

1. General description

Planar passivated Silicon Controlled Rectifier with ultra-sensitive gate in a SOT54 (TO-92) plastic package.

2. Features and benefits

- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Ultra sensitive gate

3. Applications

- Electronic ballasts
- Safety shut down and protection circuits
- Sensing circuits
- Smoke detectors
- Switched Mode Power Supplies

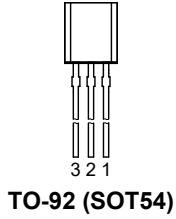

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage		-	-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 67\text{ }^{\circ}\text{C}$; Fig. 1	-	-	0.51	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 67\text{ }^{\circ}\text{C}$; Fig. 2 ; Fig. 3	-	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	8	A
		half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	-	-	9	A
T_j	junction temperature		-	-	125	$^{\circ}\text{C}$
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	0.5	-	7	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 13 ; Fig. 14	75	-	-	$\text{V}/\mu\text{s}$

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 <p>TO-92 (SOT54)</p>	
2	G	gate		
3	K	cathode		

6. Ordering information

Table 3. Ordering information

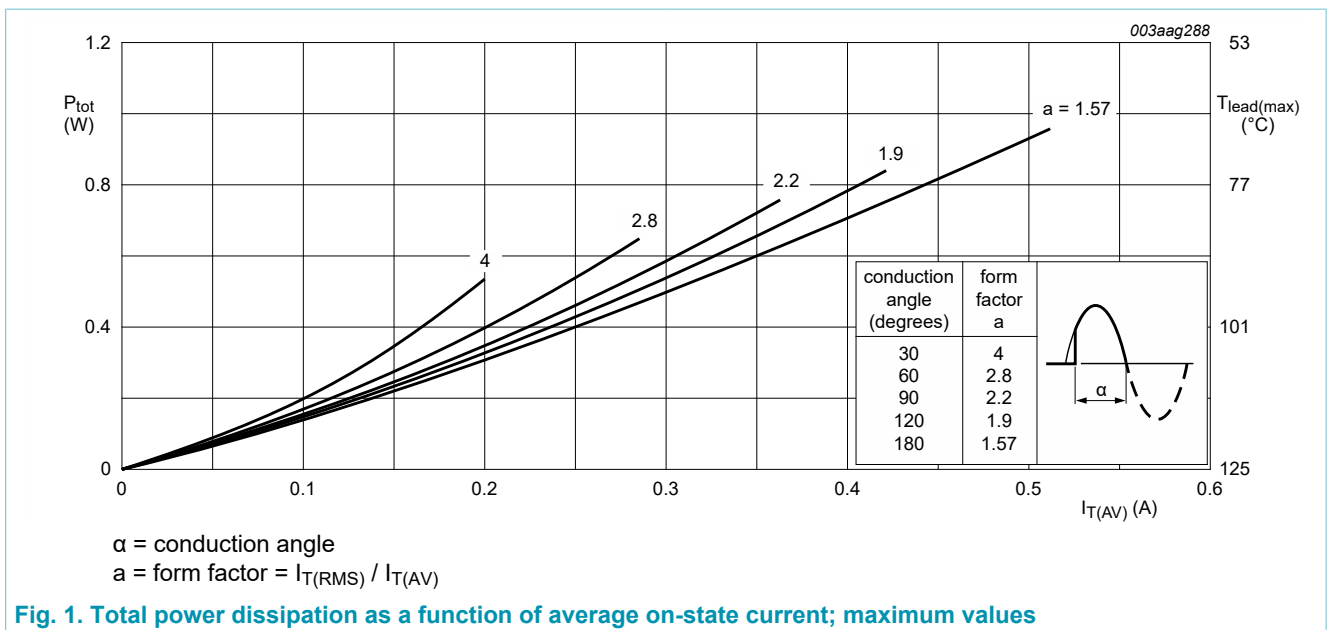
Type number	Package		
	Name	Description	Version
N0118GA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

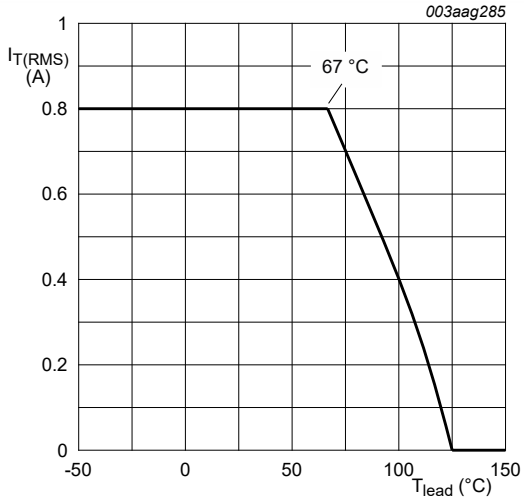
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

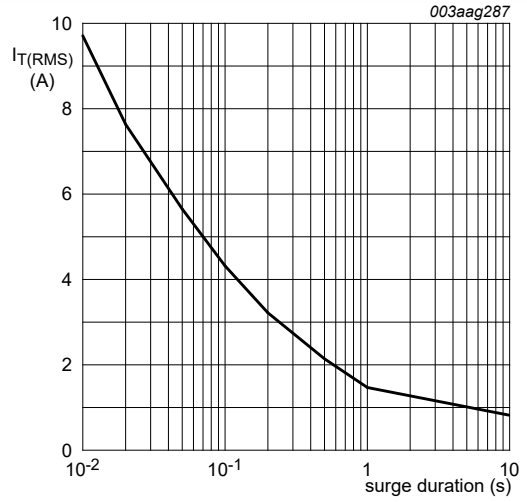
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
V_{RRM}	repetitive peak reverse voltage		-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 67\text{ }^{\circ}\text{C}$; Fig. 1	-	0.51	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 67\text{ }^{\circ}\text{C}$; Fig. 2; Fig. 3	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4; Fig. 5	-	8	A
		half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	0.32	A^2s
di_T/dt	rate of rise of on-state current	$I_T = 0.8\text{ A}$; $I_G = 10\text{ mA}$; $di_G/dt = 0.1\text{ A}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$





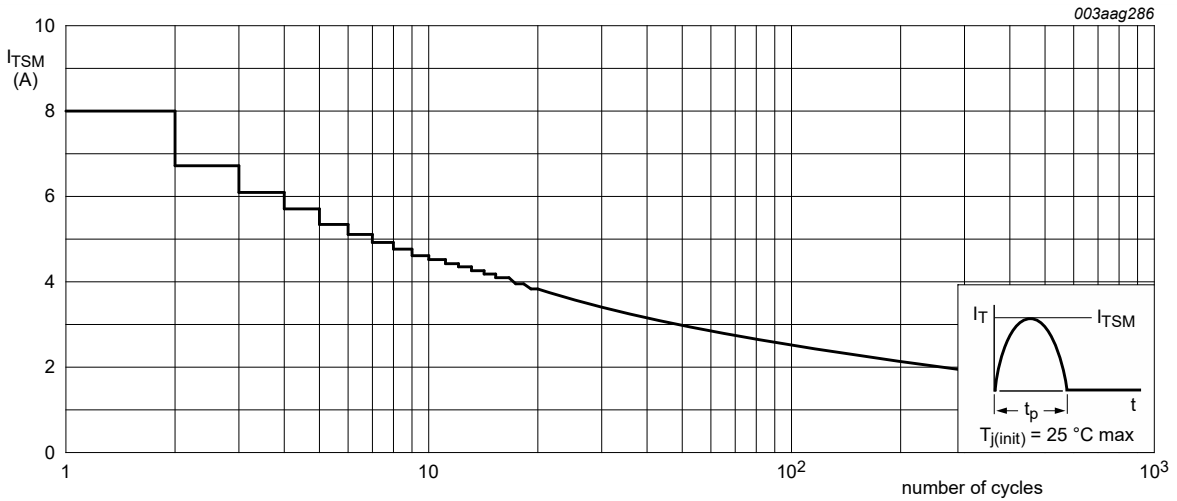
(1) $T_{lead} = 67\text{ °C}$

Fig. 2. RMS on-state current as a function of lead temperature; maximum values



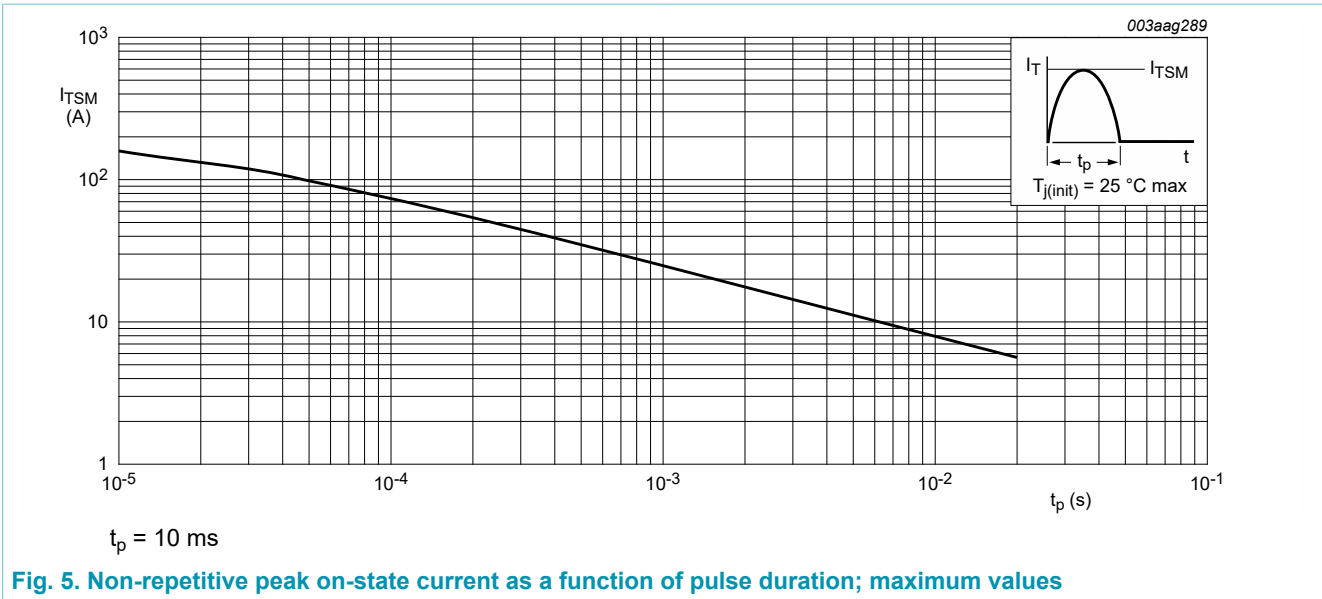
$f = 50\text{ Hz}$; $T_{lead} = 67\text{ °C}$

Fig. 3. RMS on-state current as a function of surge duration; maximum values



$f = 50\text{ Hz}$

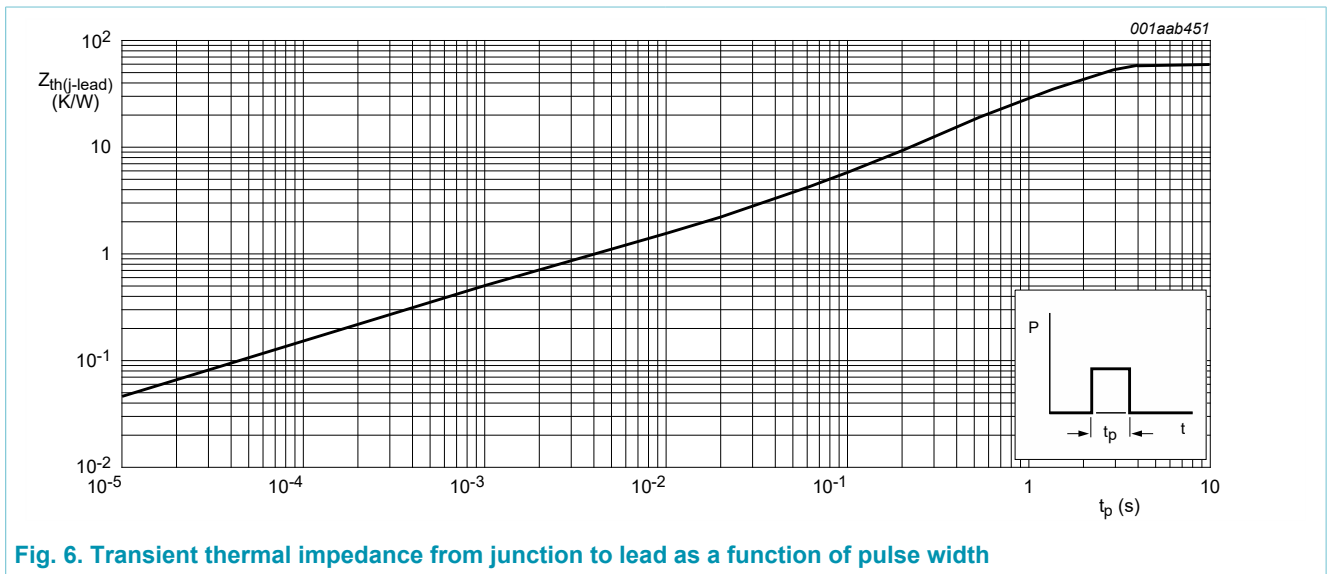
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

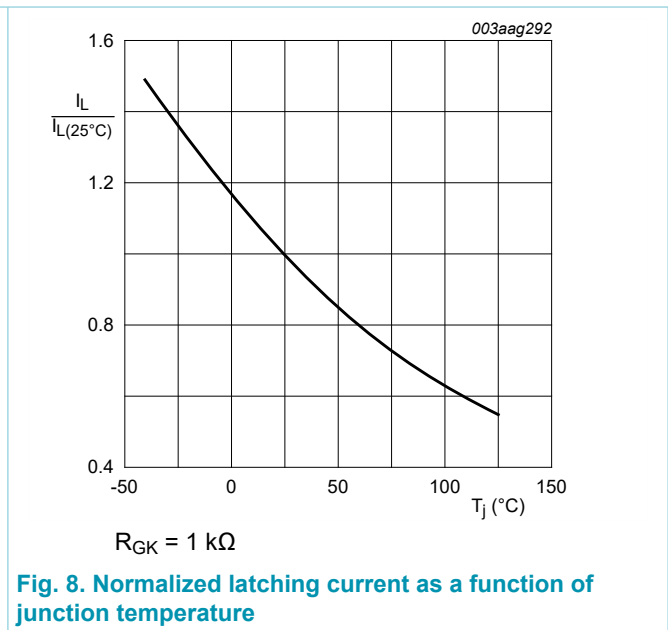
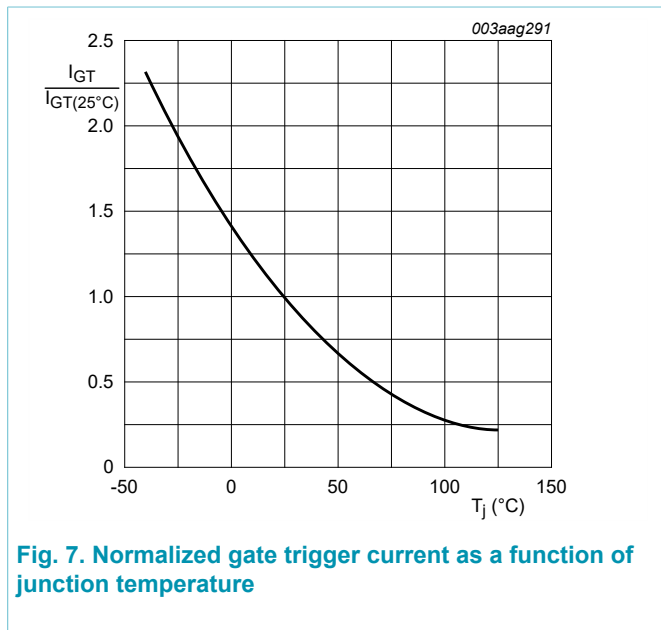
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	Fig. 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	0.5	-	7	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	6	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 ; Fig. 10	-	-	5	mA
V_T	on-state voltage	$I_T = 1.6\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	1.4	1.95	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12	-	-	0.8	V
I_D	off-state current	$V_D = 400\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	-	10	μA
		$V_D = 600\text{ V}$; $R_{GK(ext)}} = 1\text{ k}\Omega$; $T_j = 125\text{ }^\circ\text{C}$	-	-	100	μA
I_R	reverse current	$V_R = 600\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; $R_{GK(ext)}} = 1\text{ k}\Omega$	-	-	10	μA
		$V_R = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK(ext)}} = 1\text{ k}\Omega$	-	-	100	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 13 ; Fig. 14	75	-	-	V/ μs



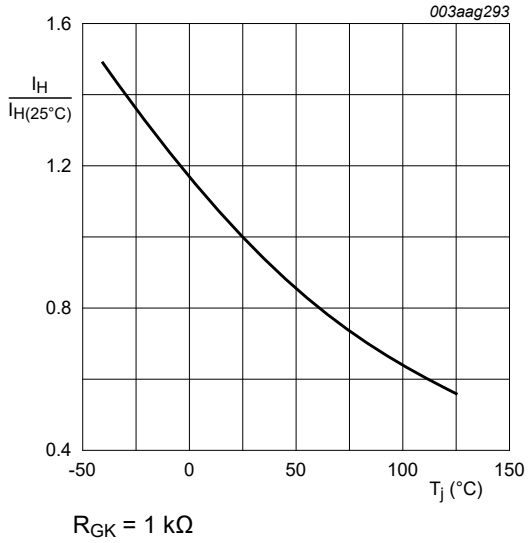


Fig. 9. Normalized holding current as a function of junction temperature

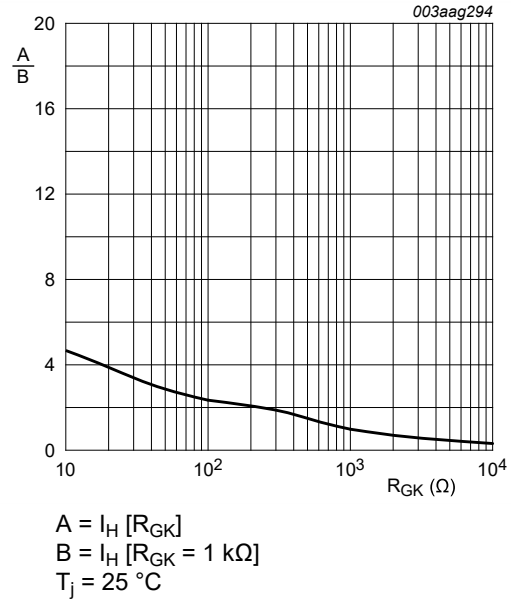
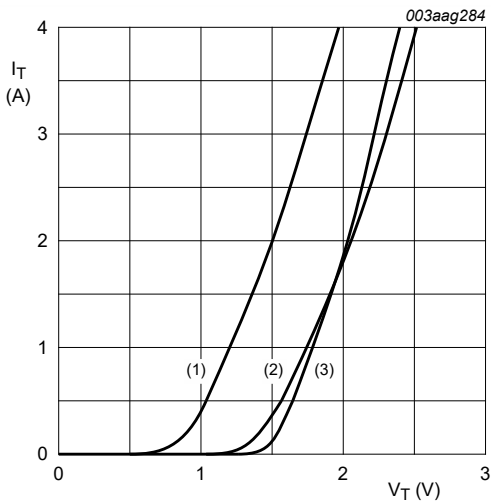


Fig. 10. Normalized holding current as a function of gate-cathode resistance (typical values)



$V_o = 1.383 \text{ V}; R_s = 0.4 \text{ } \Omega$
 (1) $T_j = 125 \text{ } ^\circ\text{C}$; typical values
 (2) $T_j = 125 \text{ } ^\circ\text{C}$; maximum values
 (3) $T_j = 25 \text{ } ^\circ\text{C}$; maximum values

Fig. 11. On-state current as a function of on-state voltage

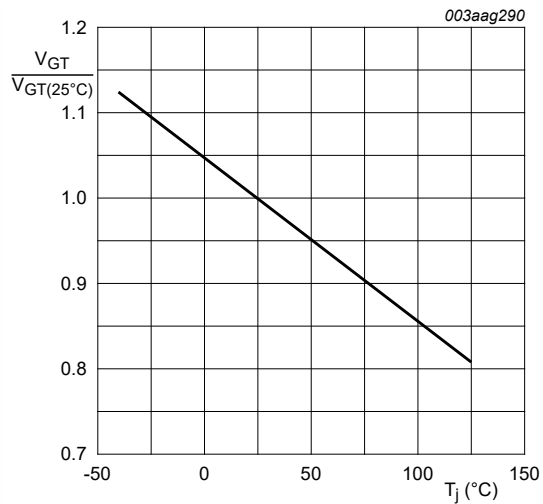
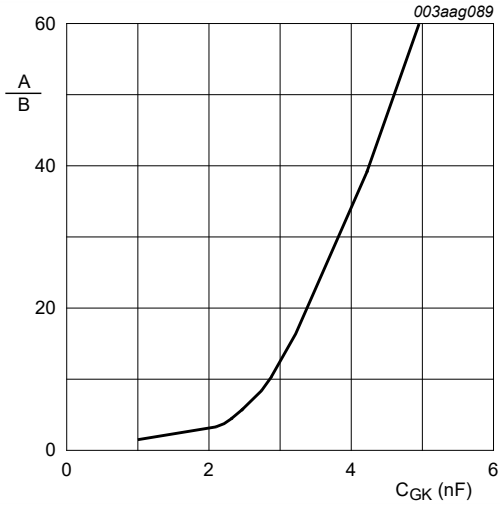
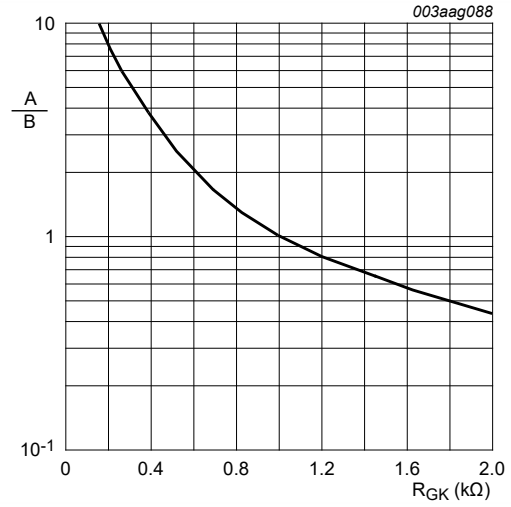


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



A = dV / dt [CGK]
 B = dV / dt [RGK = 1 kΩ]
 Tj = 125 °C;
 RGK = 1 kΩ; VDM = 402 V

Fig. 13. Normalized dV/dt immunity as a function of gate-cathode capacitance (typical values)



A = dV / dt [CGK]
 B = dV / dt [RGK = 1 kΩ]
 Tj = 125 °C;
 RGK = 1 kΩ; VDM = 402 V

Fig. 14. Normalized dV/dt immunity as a function of gate-cathode resistance (typical values)

10. Package outline

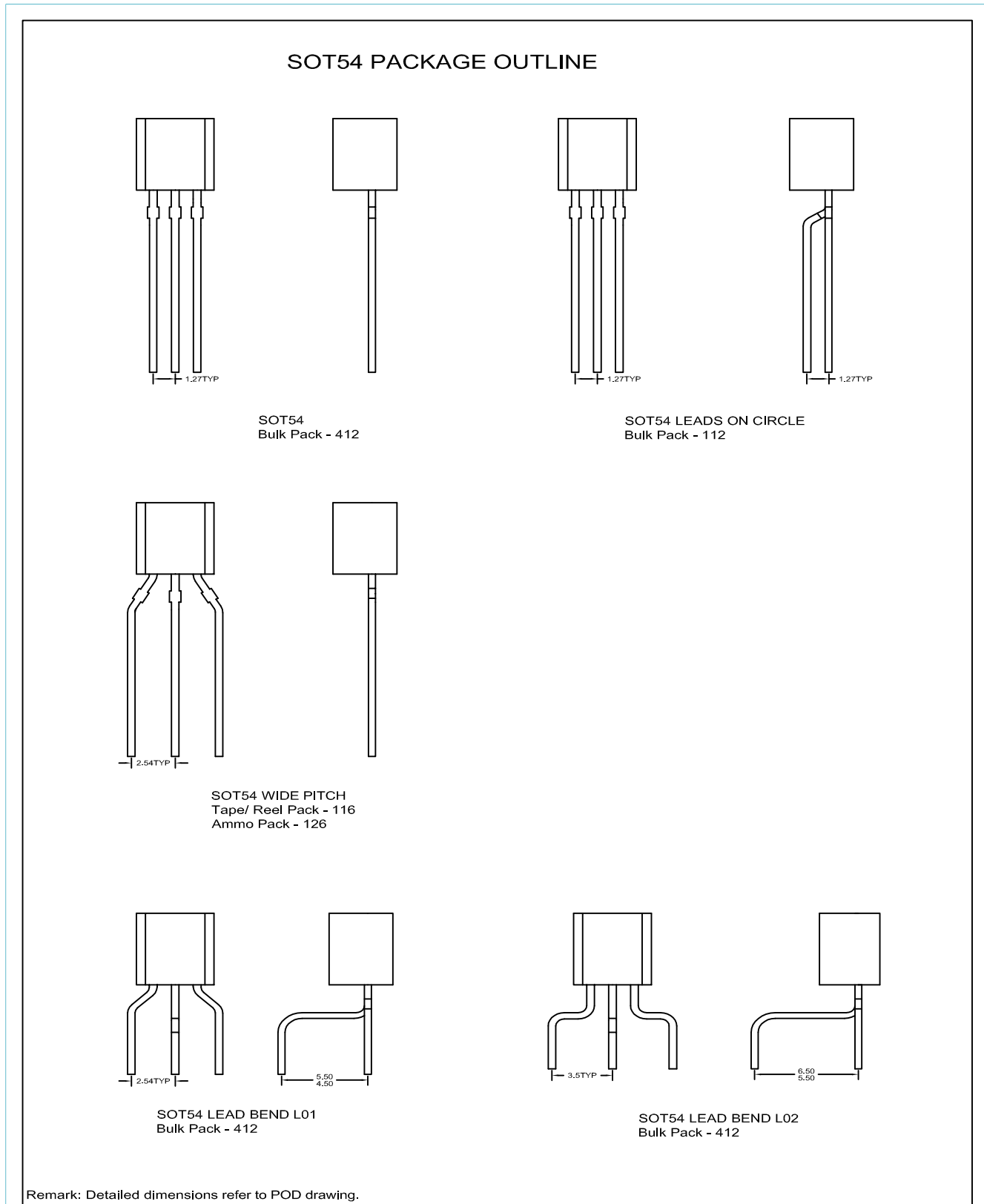


Fig. 15. Package outline TO-92 (SOT54)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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