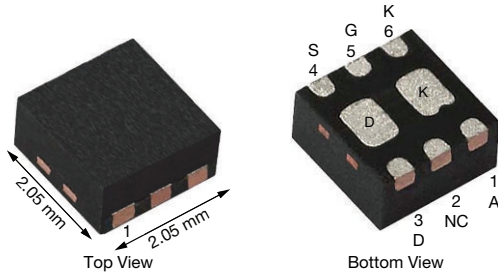


P-Channel 20 V (D-S) MOSFET with Schottky Diode

PowerPAK® SC-70-6L Dual with Schottky Diode



Marking code: HD

PRODUCT SUMMARY	
MOSFET	
V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.116
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5$ V	0.155
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8$ V	0.205
Q_g typ. (nC)	4.9
I_D (A) ^a	-4.5
SCHOTTKY	
V_{KA} (V)	20
V_F (V) at 1 A	0.45
I_F (A) ^a	2
Configuration	Dual plus integrated Schottky

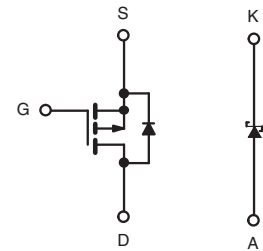
FEATURES

- LITTLE FOOT® plus Schottky power MOSFET
- New thermally enhanced PowerPAK® SC-70 package
 - Small footprint area
 - Low on-resistance
 - Thin 0.75 mm profile
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Cellular charger switch
- Asynchronous DC/DC for portable devices
- Load switch for portable devices



P-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK SC-70
Lead (Pb)-free and halogen-free	SiA811ADJ-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage (MOSFET)	V_{DS}	-20	V		
Reverse voltage (Schottky)	V_{KA}	20			
Gate-source voltage (MOSFET)	V_{GS}	± 8			
Continuous drain current ($T_J = 150$ °C) (MOSFET)	I_D	$T_C = 25$ °C	-4.5 ^a	A	
		$T_C = 70$ °C	-4.5 ^a		
		$T_A = 25$ °C	-3.2 ^{b, c}		
		$T_A = 70$ °C	-2.6 ^{b, c}		
Pulsed drain current (MOSFET)	I_{DM}	-8	W		
Continuous source-drain diode current (MOSFET diode conduction)	I_S	$T_C = 25$ °C			-4.5 ^a
		$T_A = 25$ °C			-1.5 ^{b, c}
Average forward current (Schottky)	I_F	2 ^b			W
Pulsed forward current (Schottky)	I_{FM}	5			
Maximum power dissipation (MOSFET)	P_D	$T_C = 25$ °C	6.5		
		$T_C = 70$ °C	4.2		
		$T_A = 25$ °C	1.8 ^{b, c}		
		$T_A = 70$ °C	1.1 ^{b, c}		
Maximum power dissipation (Schottky)	P_D	$T_C = 25$ °C	6.8		
		$T_C = 70$ °C	4.3		
		$T_A = 25$ °C	1.6 ^{b, c}		
		$T_A = 70$ °C	1 ^{b, c}		
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C		
Soldering recommendations (peak temperature) ^{d, e}		260			



THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient (MOSFET) ^{b, f}	$t \leq 5$ s	R_{thJA}	55	70	°C/W	
Maximum junction-to-case (drain) (MOSFET)	Steady state	R_{thJC}	15	19		
Maximum junction-to-ambient (Schottky) ^{b, f}	$t \leq 5$ s	R_{thJA}	62	76		
Maximum junction-to-case (drain) (Schottky)	Steady state	R_{thJC}	15	18.5		

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 110 °C/W

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = -250$ μ A	-20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = -250$ μ A	-	-19	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	2.4	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250$ μ A	-0.4	-	-1	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -20$ V, $V_{GS} = 0$ V	-	-	-1	μ A
		$V_{DS} = -20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	-	-	-10	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \leq 5$ V, $V_{GS} = -4.5$ V	-8	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -2.8$ A	-	0.096	0.116	Ω
		$V_{GS} = -2.5$ V, $I_D = -2.3$ A	-	0.126	0.155	
		$V_{GS} = -1.8$ V, $I_D = -0.54$ A	-	0.165	0.205	
Forward transconductance ^a	g_{fs}	$V_{DS} = -10$ V, $I_D = -2.8$ A	-	7	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = -10$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	345	-	pF
Output capacitance	C_{oss}		-	65	-	
Reverse transfer capacitance	C_{rss}		-	50	-	
Total gate charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -8$ V, $I_D = -3.5$ A	-	8.4	13	nC
		$V_{DS} = -10$ V, $V_{GS} = -4.5$ V, $I_D = -3.5$ A	-	4.9	7.4	
Gate-source charge	Q_{gs}		-	0.75	-	
Gate-drain charge	Q_{gd}		-	1.2	-	
Gate resistance	R_g	$f = 1$ MHz	-	6	-	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 2.85$ Ω $I_D \cong -3.5$ A, $V_{GEN} = -4.5$ V, $R_g = 1$ Ω	-	15	25	ns
Rise time	t_r		-	45	70	
Turn-off delay time	$t_{d(off)}$		-	20	30	
Fall time	t_f		-	10	15	
Turn-on delay time	$t_{d(on)}$		-	5	10	
Rise time	t_r	$V_{DD} = -10$ V, $R_L = 2.85$ Ω $I_D \cong -3.5$ A, $V_{GEN} = -8$ V, $R_g = 1$ Ω	-	10	15	
Turn-off delay time	$t_{d(off)}$	-	20	30		
Fall time	t_f	-	10	15		



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	-4.5	A
Pulse diode forward current	I_{SM}		-	-	-8	
Body diode voltage	V_{SD}	$I_S = -1\text{ A}, V_{GS} = 0\text{ V}$	-	-0.8	-1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = -4.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	30	60	ns
Body diode reverse recovery charge	Q_{rr}		-	20	40	nC
Reverse recovery fall time	t_a		-	15	-	ns
Reverse recovery rise time	t_b		-	15	-	

Notes

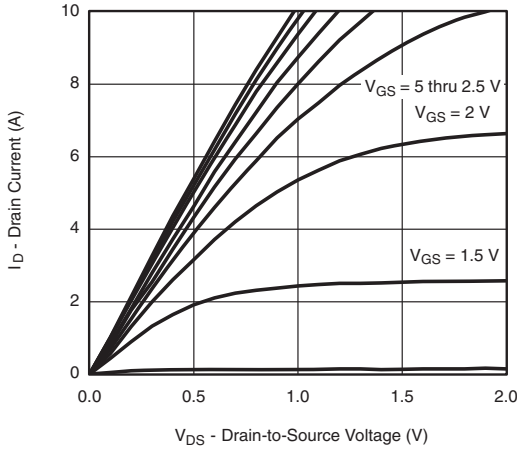
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 b. Guaranteed by design, not subject to production testing

SCHOTTKY SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Forward voltage drop	V_F	$I_F = 1\text{ A}$	-	0.41	0.45	V
		$I_F = 1\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	0.36	0.41	
Maximum reverse leakage current	I_{rm}	$V_r = 5\text{ V}$	-	0.015	0.080	mA
		$V_r = 5\text{ V}, T_J = 85\text{ }^\circ\text{C}$	-	0.5	5	
		$V_r = 20\text{ V}$	-	0.02	0.10	
		$V_r = 20\text{ V}, T_J = 85\text{ }^\circ\text{C}$	-	0.7	7	
Junction capacitance	C_T	$V_r = 20\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	5	50	pF
		$V_r = 10\text{ V}$	-	60	-	

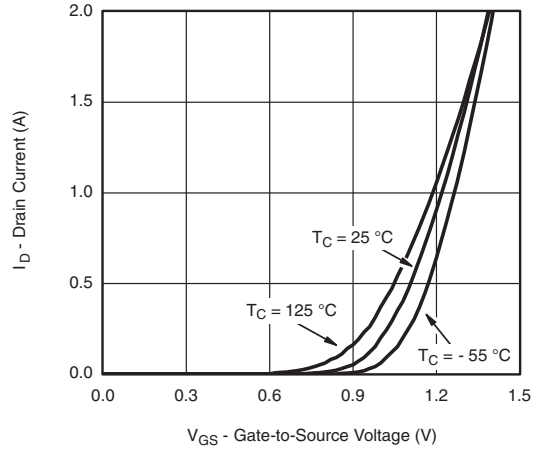
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



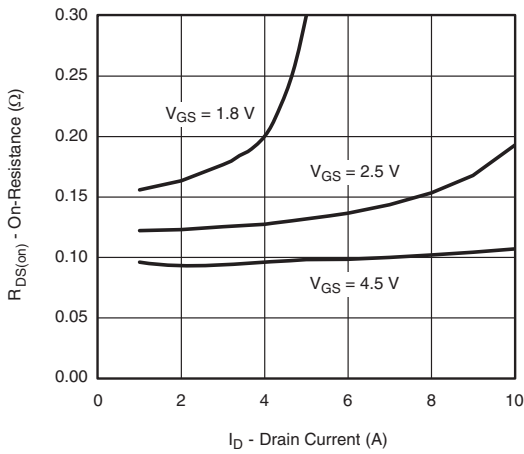
MOSFET TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



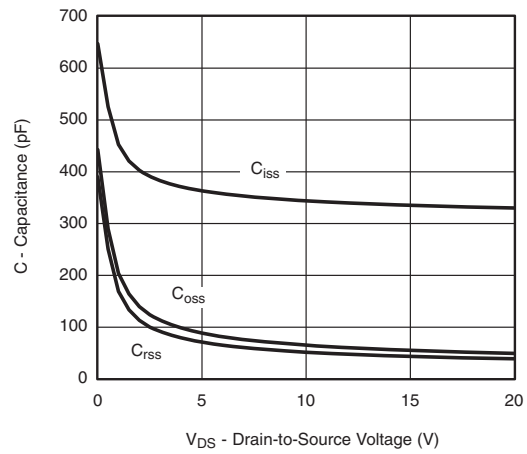
Output Characteristics



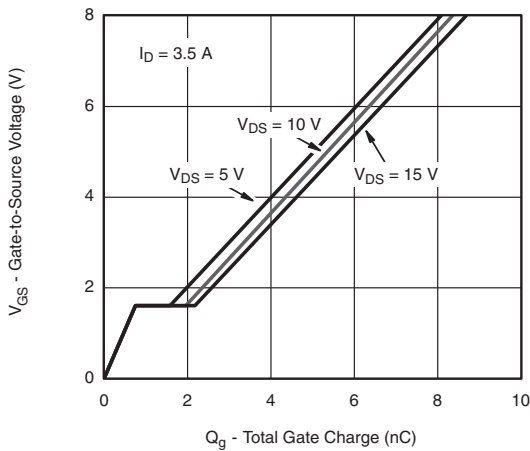
Transfer Characteristics



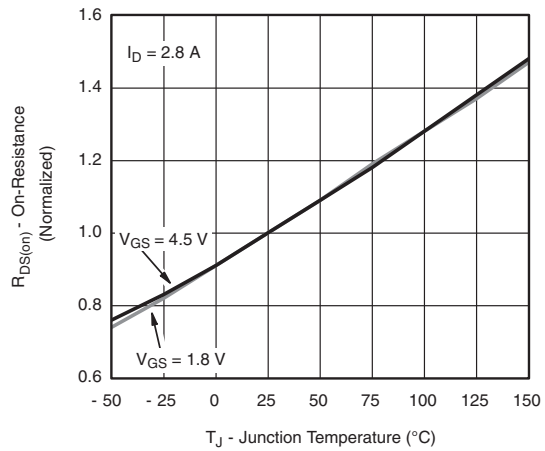
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



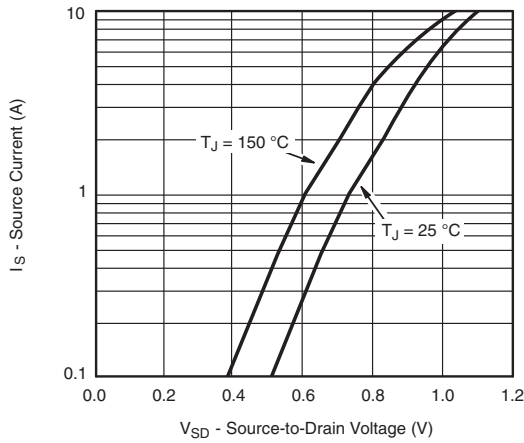
Gate Charge



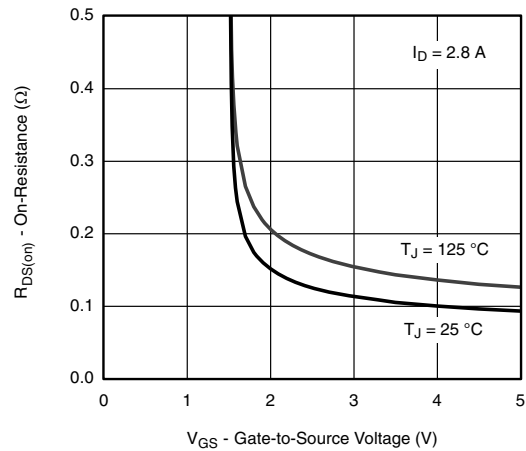
On-Resistance vs. Junction Temperature



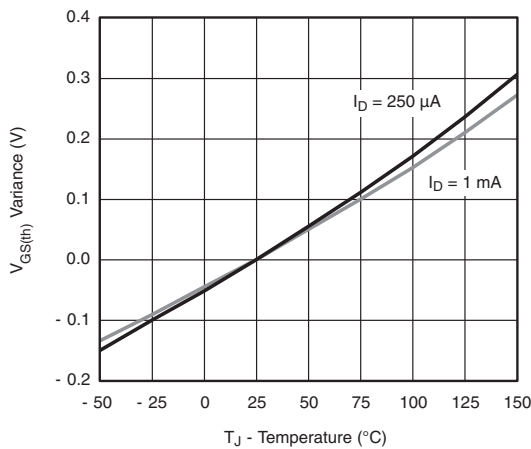
MOSFET TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



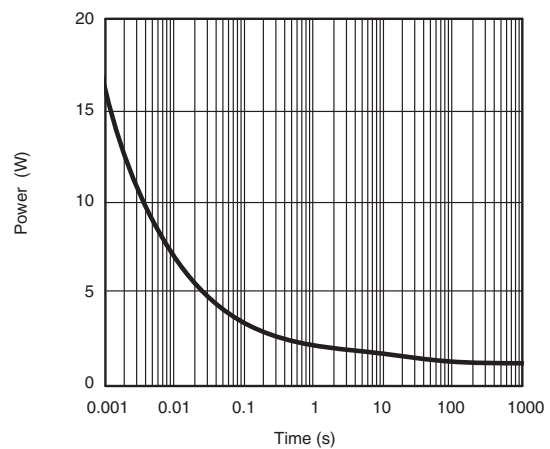
Source-Drain Diode Forward Voltage



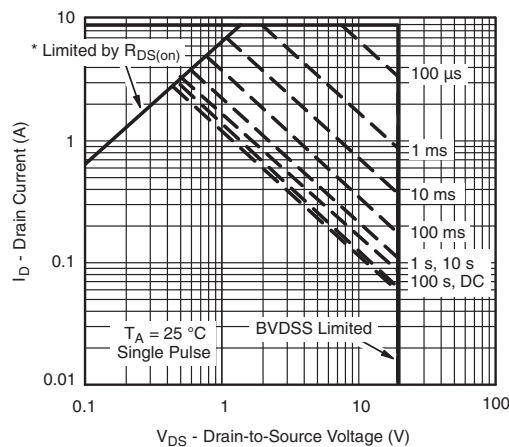
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



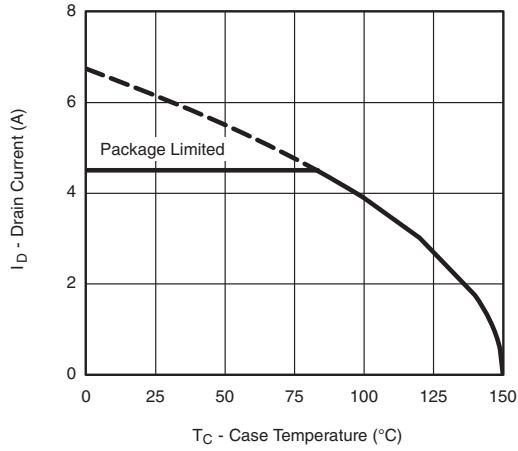
Single Pulse Power, Junction-to-Ambient



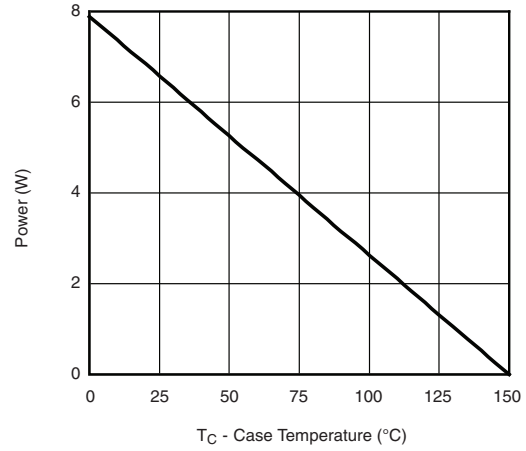
Safe Operating Area, Junction-to-Case



MOSFET TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Current Derating ^a



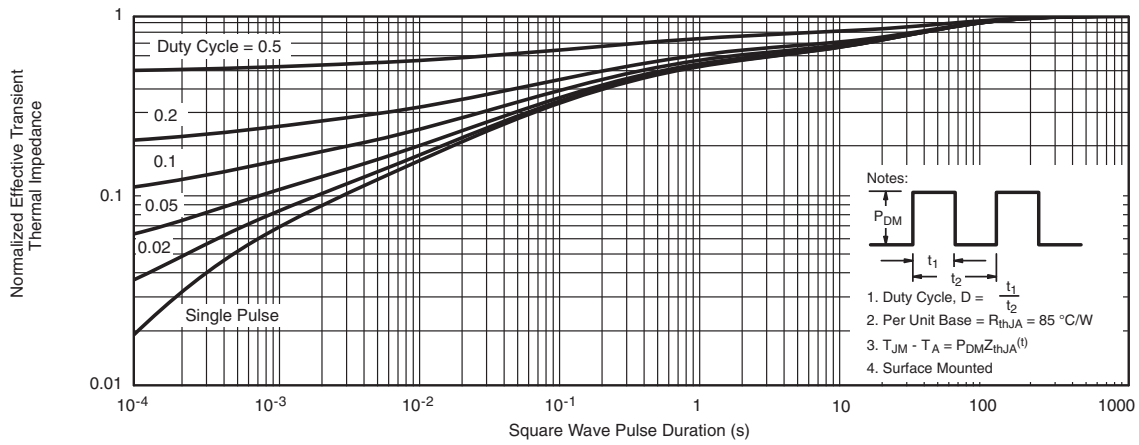
Power Derating

Note

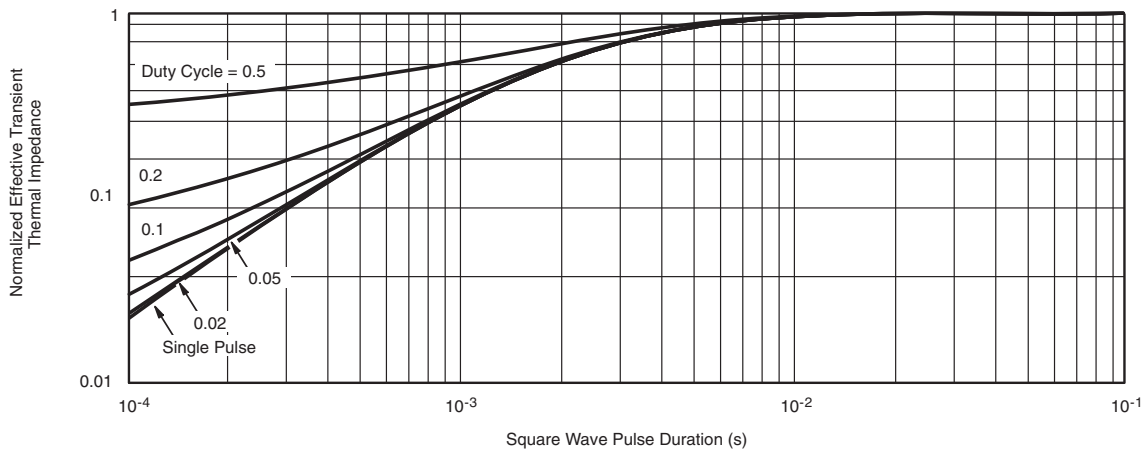
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



MOSFET TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



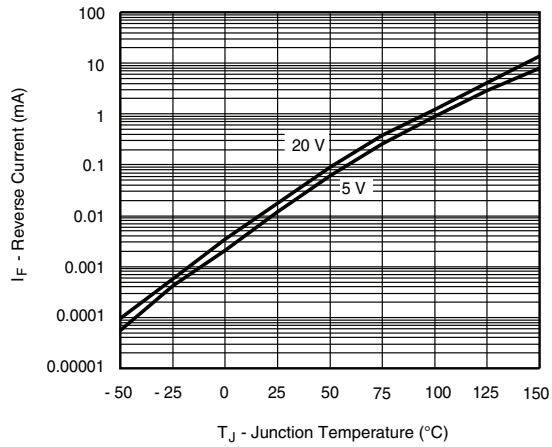
Normalized Thermal Transient Impedance, Junction-to-Ambient



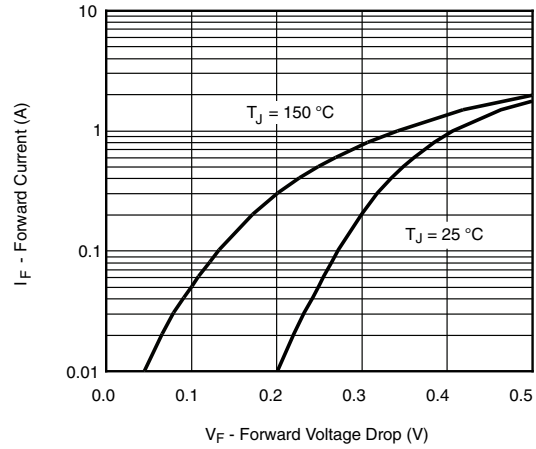
Normalized Thermal Transient Impedance, Junction-to-Case



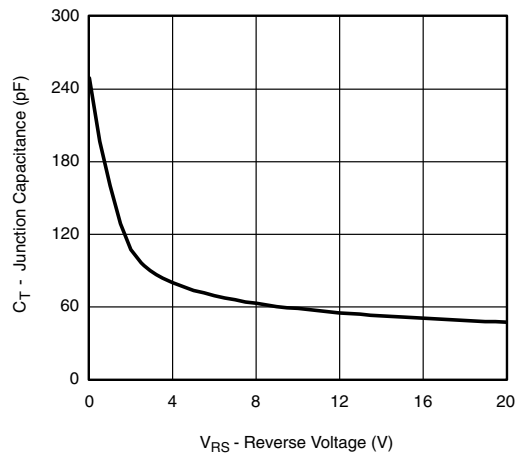
SCHOTTKY TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Reverse Current vs. Junction Temperature



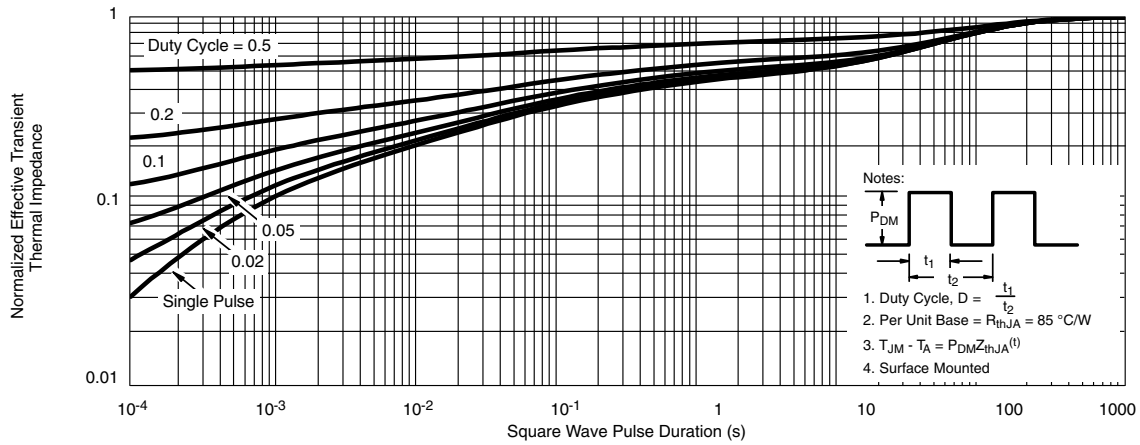
Forward Voltage Drop



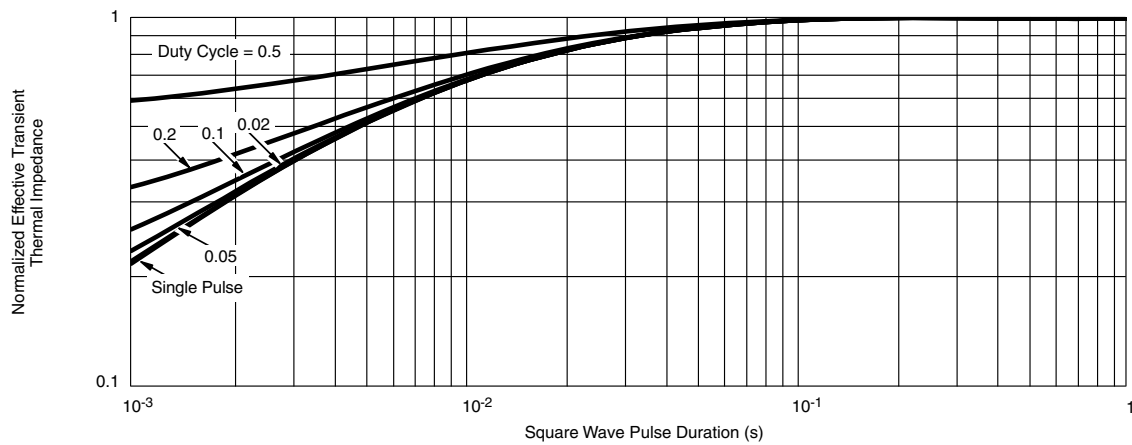
Capacitance



SCHOTTKY TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

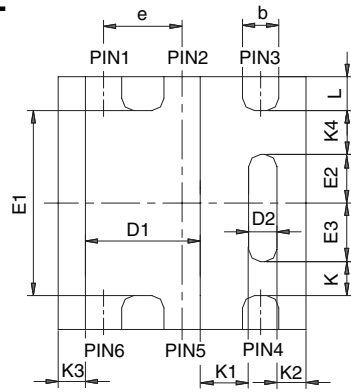


Normalized Thermal Transient Impedance, Junction-to-Case

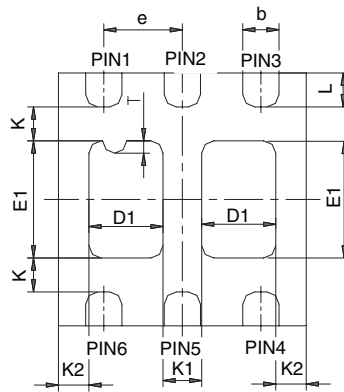
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68955.



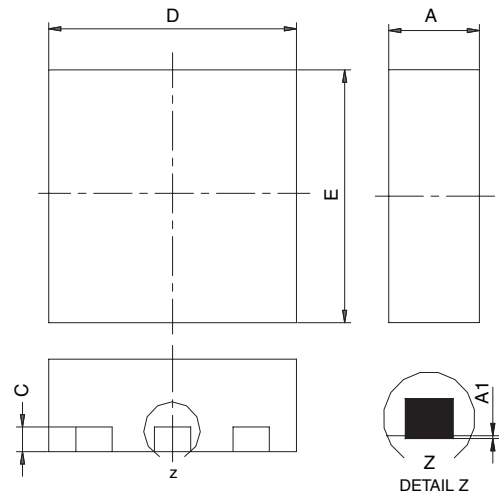
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL

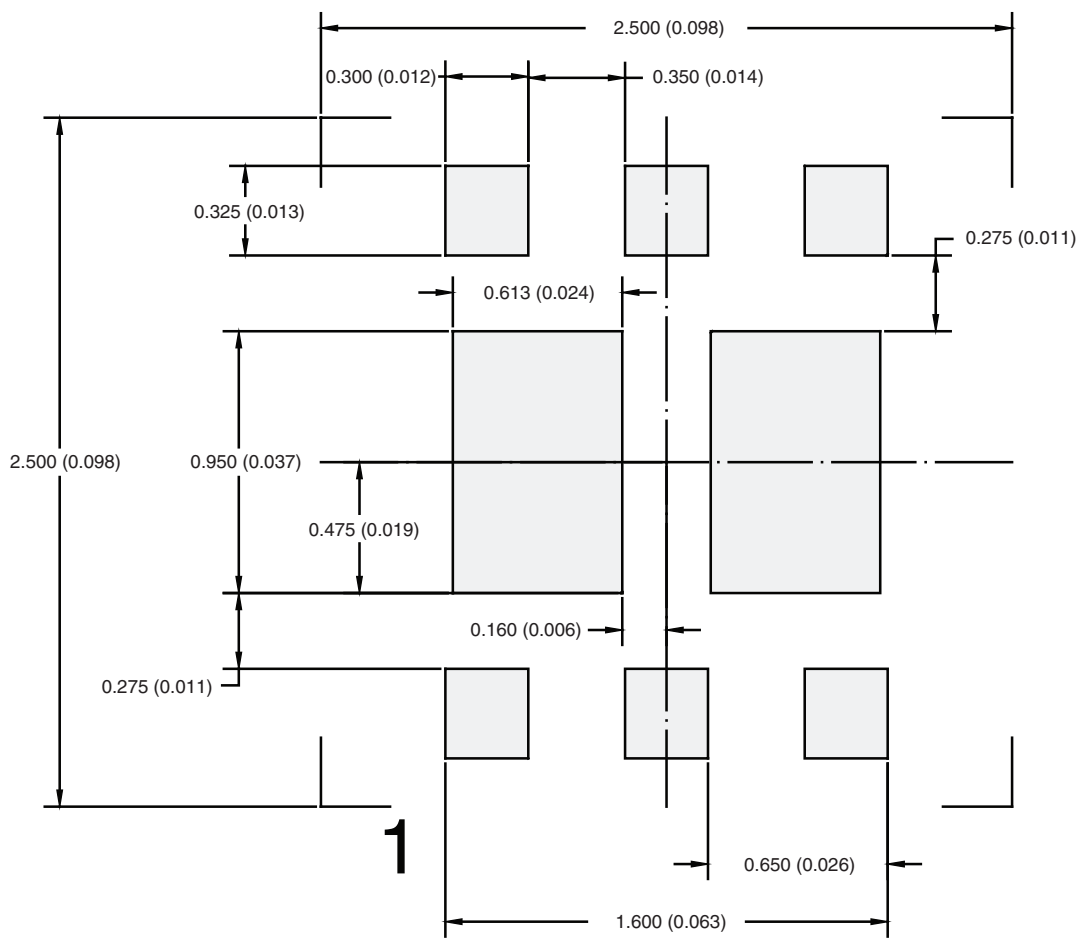


- Notes:
 1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07
 DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)

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APPLICATION NOTE



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