



Dual P-Channel 30-V (D-S) MOSFET

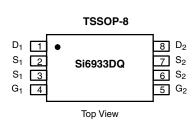
PRODUCT SUMMARY			
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	
- 30	0.045 at V _{GS} = - 10 V	± 3.5	
	0.085 at V _{GS} = - 4.5 V	± 2.5	

FEATURES

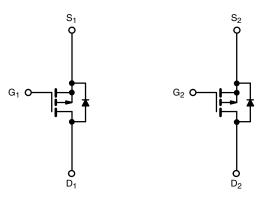
- Halogen-free
- TrenchFET[®] Power MOSFETs



RoHSCOMPLIANT



Ordering Information: Si6933DQ-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	- 30	V	
Gate-Source Voltage		V _{GS}	± 20	\neg \lor $ $	
Continuous Drain Current /T 150 °C\8	T _A = 25 °C	- I _D	± 3.5		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		± 2.8	_	
Pulsed Drain Current		I _{DM}	± 20	Α	
Continuous Source Current (Diode Conduction) ^a		I _S	- 1.25		
Mariana Daniar Dissis Aliand	T _A = 25 °C	P _D	1.0	W	
Maximum Power Dissipation ^a	T _A = 70 °C	' D	0.64		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W	

Notes:

a. Surface Mounted on FR4 board, $t \leq 10 \ s.$

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm.

Si6933DQ

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit		
Static								
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	- 1.0			V		
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA		
Zara Cata Valtaga Drain Current		$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	μΑ		
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			- 25			
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 15			Α		
	D	$V_{GS} = -10 \text{ V}, I_D = 3.5 \text{ A}$		0.035	0.045	0		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = 2.5 \text{ A}$		0.062	0.085	Ω		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 3.5 A		7.2		S		
Diode Forward Voltage ^a	V_{SD}	I _S = - 1.25 A, V _{GS} = 0 V		- 0.77	- 1.2	V		
Dynamic ^b								
Total Gate Charge	Q_g			17	30			
Gate-Source Charge	Q_{gs}	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 3.5 A		4.4		nC		
Gate-Drain Charge	Q_{gd}			3.1				
Turn-On Delay Time	t _{d(on)}			13	20			
Rise Time	t _r	V_{DD} = - 15 V, R_L = 15 Ω		10	20			
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ - 1 A, $V_{GEN}=$ - 10 V, $R_G=6~\Omega$		33	60	ns		
Fall Time	t _f			10	20			
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 1.25 A, dI/dt = 100 A/μs		30	60			

Notes:

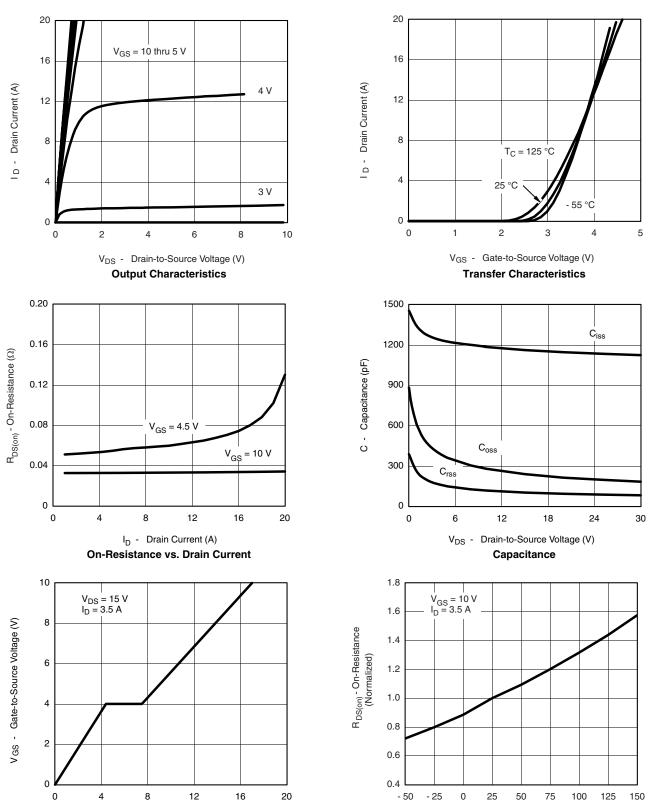
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

b. Guaranteed by design, not subject to production testing.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Total Gate Charge (nC)

Gate Charge

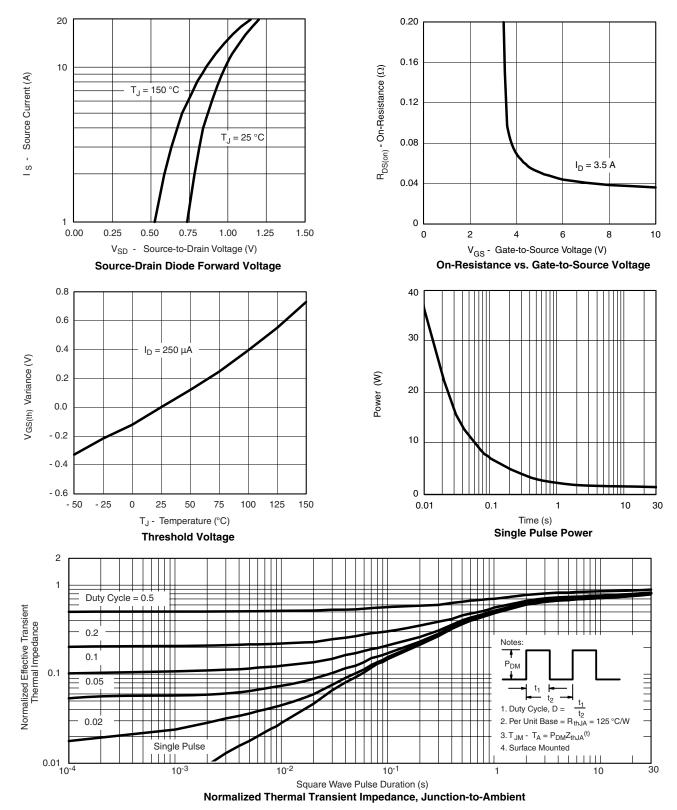
T_J - Junction Temperature (°C)

On-Resistance vs. Junction Temperature

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70640.



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