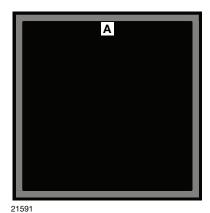


Vishay Semiconductors

Silicon PIN Photodiode



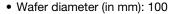
DESCRIPTION

T1610P is a high speed and high sensitive PIN photodiode chip with 7.7 mm² sensitive area. It is sensitive to visible light much like the human eye and has peak sensitivity at 560 nm. Anode is the bond pad on top, cathode is the backside contact.

FEATURES

- Package type: chip
- · Package form: single chip





• Radiant sensitive area (in mm²): 7.7

· High photo sensitivity

· High radiant sensitivity

· Suitable for visible light

Fast response times

• Angle of half sensitivity: $\varphi = \pm 60^{\circ}$

· Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



HALOGEN

FREE GREEN

APPLICATIONS

- · Ambient light sensor
- · Backlight dimmer

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY					
COMPONENT	I _{ra} (μΑ)	φ (deg)	λ _{0.5} (nm)		
T1610P	2.9	± 60	390 to 800		

Note

Test conditions see table "Basic Characteristics"

ORDERING INFORMATION					
ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM		
T1610P-SD-F	Wafer sawn on foil with disco frame	MOQ: 3500 pcs	Chip		

· MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T _{amb} = 25 °C, unless otherwise specified)					
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT	
Reverse voltage		V _R	16	V	
Junction temperature		T _j	100	°C	
Operating temperature range		T _{amb}	-40 to +100	°C	
Storage temperature range		T _{stg1}	-40 to +100	°C	
Storage temperature range on foil		T _{stg2}	-40 to +50	°C	

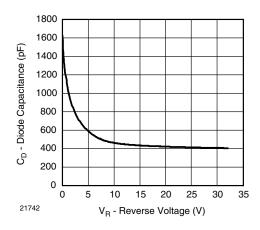
ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishav.com/doc?91000

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BASIC CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Breakdown voltage	I _R = 100 μA, E = 0	V _(BR)	16			V
Reverse dark current	V _R = 10 V, E = 0	I _{ro}		2	5	nA
Diode capacitance	V _R = 3 V, f = 1 MHz, E = 0	C _D		730		pF
Reverse light current	$E_V = 100 \text{ lx}$, CIE illuminant A, $V_R = 5 \text{ V}$	I _{ra}		2.9		μΑ
Angle of half sensitivity		φ		± 60		deg
Wavelength of peak sensitivity		λ_{p}		560		nm
Range of spectral bandwidth		λ _{0.5}		390 to 800		nm
Rise time	$V_R = 5 \text{ V}, R_L = 50 \Omega, \lambda = 515 \text{ nm}$	t _r		100		ns
Fall time	$V_R = 5 \text{ V}, R_L = 50 \Omega, \lambda = 515 \text{ nm}$	t _f		100		ns

Note

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)





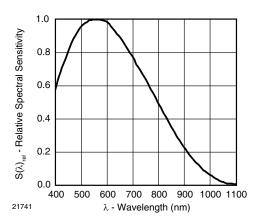


Fig. 2 - Relative Spectral Sensitivity vs. Wavelength

MECHANICAL DIMENSIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Length of chip edge (x-direction)	L _x		2.97		mm
Length of chip edge (y-direction)	L _y		2.97		mm
Sensitive area	As		7.7		mm ²
Die height	Н		0.28		mm
Bond pad anode	x * v		0.125 x 0.11		mm ²

ADDITIONAL INFORMATION				
Frontside metallization, anode	AlSi			
Backside metallization, cathode	NiV-Ag			
Dicing	Sawing			
Die bonding technology	Epoxy bonding			

Note

All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870.
The visual inspection shall be made in accordance with the "specification of visual inspection as referenced". The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification.
The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

[•] The measurements are based on samples of die which are mounted on a TO-header without resin coating



Vishay Semiconductors

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.



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