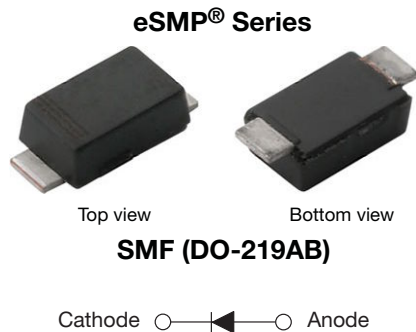


## Hyperfast Rectifier, 1 A FRED Pt<sup>®</sup>



### DESIGN SUPPORT TOOLS

[click logo to get started](#)

**3D**  
Models  
Available

### FEATURES

- Hyperfast recovery time, reduced  $Q_{rr}$ , and soft recovery
- 175 °C maximum operating junction temperature
- Specified for output and snubber operation
- Low forward voltage drop
- Low leakage current
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- Wave and reflow solderable
- AEC-Q101 qualified, meets JESD 201 class 2 whisker test
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### DESCRIPTION / APPLICATIONS

State of the art hyperfast recovery rectifiers specifically designed with optimized performance of forward voltage drop and hyperfast recovery time.

The planar structure and the platinum doped life time control guarantee the best overall performance, ruggedness, and reliability characteristics.

These devices are intended for use in snubber, boost, lighting, piezo-injection, as high frequency rectifiers, and freewheeling diodes.

Their extremely optimized stored charge and low recovery current minimize the switching losses and reduce power dissipation in the switching element.

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	1 A
$V_R$	100 V
$V_F$ at $I_F$ (typ. 125 °C)	0.74 V
$t_{rr}$	25 ns
$T_J$ max.	175 °C
Package	SMF (DO-219AB)
Circuit configuration	Single

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	$V_{RRM}$		100	V
Average rectified forward current	$I_{F(AV)}$	$T_C = 160$ °C <sup>(1)</sup>	1	A
Non-repetitive peak surge current	$I_{FSM}$	$T_J = 25$ °C	35	
Operating junction and storage temperature range	$T_J, T_{Stg}$		-65 to +175	°C

#### Note

<sup>(1)</sup> Device on PCB with 8 mm x 16 mm soldering lands

ELECTRICAL SPECIFICATIONS ( $T_J = 25$ °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Breakdown voltage, blocking voltage	$V_{BR}, V_R$	$I_R = 100$ $\mu$ A	100	-	-	V
Reverse leakage current	$I_R$	$V_R = V_R$ rated	-	-	2	$\mu$ A
		$T_J = 125$ °C, $V_R = V_R$ rated	-	0.5	8	
Junction capacitance	$C_T$	$V_R = 100$ V	-	5	-	pF

<b>DYNAMIC RECOVERY CHARACTERISTICS</b> ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse recovery time	$t_{rr}$	$I_F = 1\text{ A}$ , $dI_F/dt = 50\text{ A}/\mu\text{s}$ , $V_R = 30\text{ V}$	-	24	-	ns
		$I_F = 0.5\text{ A}$ , $I_R = 1\text{ A}$ , $I_{rr} = 0.25\text{ A}$	-	-	25	
		$T_J = 25\text{ }^\circ\text{C}$	-	16	-	
		$T_J = 125\text{ }^\circ\text{C}$	-	23	-	
Peak recovery current	$I_{RRM}$	$T_J = 25\text{ }^\circ\text{C}$	-	1.6	-	A
		$T_J = 125\text{ }^\circ\text{C}$	-	2.5	-	
Reverse recovery charge	$Q_{rr}$	$T_J = 25\text{ }^\circ\text{C}$	-	13	-	nC
		$T_J = 125\text{ }^\circ\text{C}$	-	30	-	

<b>THERMAL - MECHANICAL SPECIFICATIONS</b>						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	$T_J, T_{Stg}$		-65	-	+175	$^\circ\text{C}$
Thermal resistance, junction to case	$R_{thJC}$	Device mounted on PCB with 8 mm x 16 mm soldering lands	-	-	17	$^\circ\text{C}/\text{W}$
Thermal resistance, junction to ambient	$R_{thJA}$	Device mounted on PCB with 2 mm x 3.5 mm soldering lands	-	-	140	$^\circ\text{C}/\text{W}$
Approximate weight			0.015			g
			0.0005			oz.
Marking device		Case style SMF (DO-219AB)	MAH			

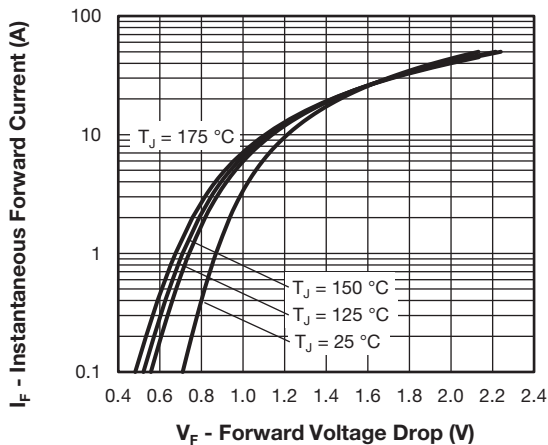


Fig. 1 - Typical Forward Voltage Drop Characteristics

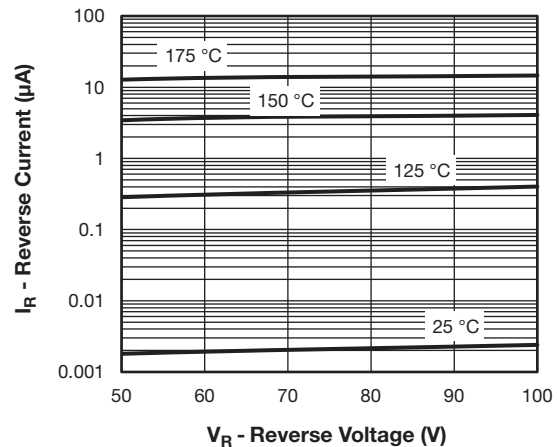


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

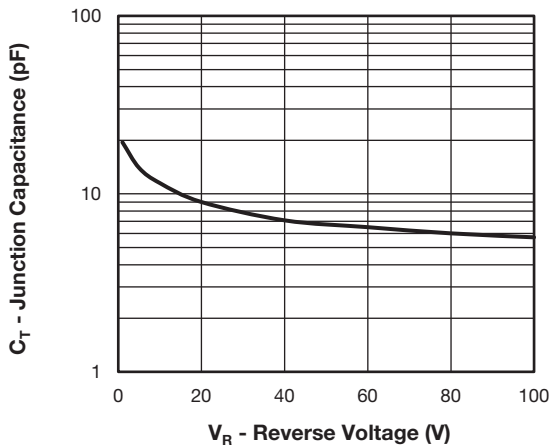


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

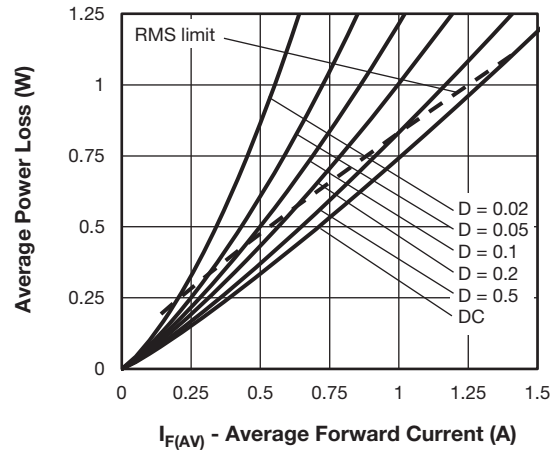


Fig. 5 - Forward Power Loss Characteristics

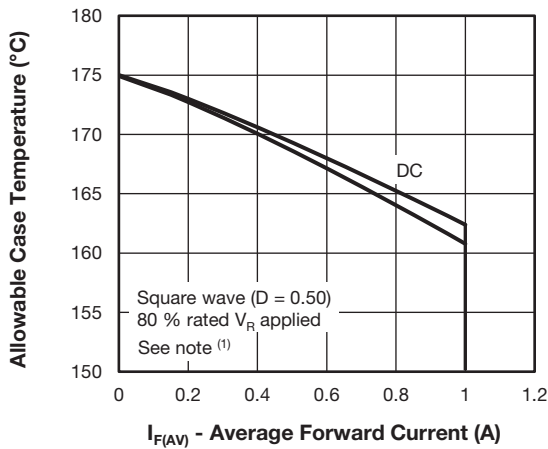


Fig. 4 - Maximum Allowable Case Temperature vs. Average Forward Current

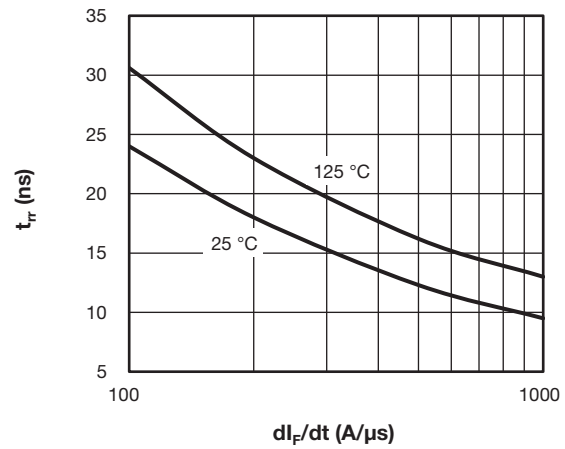


Fig. 6 - Typical Reverse Recovery Time vs.  $di_F/dt$

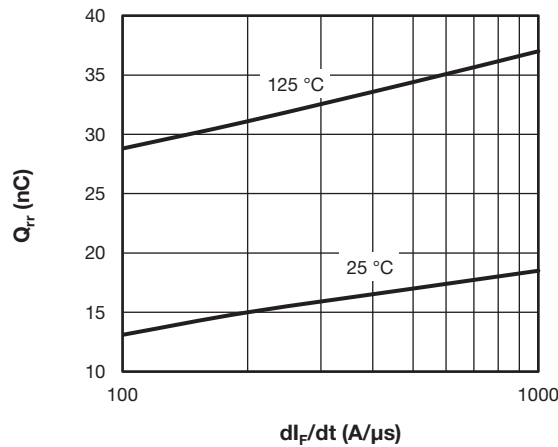
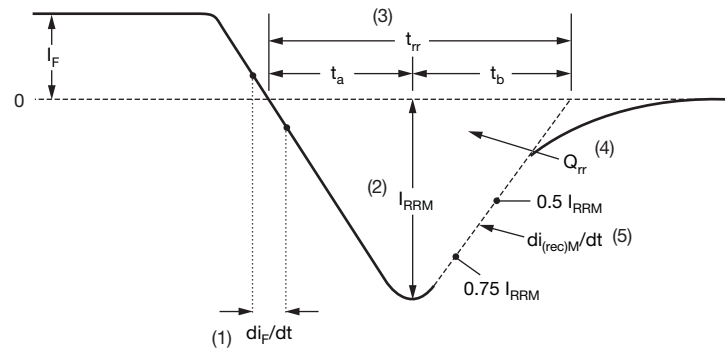


Fig. 7 - Typical Stored Charge vs.  $di_F/dt$

**Note**

- (1) Formula used:  $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$ ;  
 $P_d$  = forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 5);  
 $P_{dREV}$  = inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at  $V_{R1}$  = rated  $V_R$



- (1)  $di_F/dt$  - rate of change of current through zero crossing
- (2)  $I_{RRM}$  - peak reverse recovery current
- (3)  $t_{rr}$  - reverse recovery time measured from zero crossing point of negative going  $I_F$  to point where a line passing through  $0.75 I_{RRM}$  and  $0.50 I_{RRM}$  extrapolated to zero current.
- (4)  $Q_{rr}$  - area under curve defined by  $t_{rr}$  and  $I_{RRM}$
- $$Q_{rr} = \frac{t_{rr} \times I_{RRM}}{2}$$
- (5)  $di_{(rec)M}/dt$  - peak rate of change of current during  $t_b$  portion of  $t_{rr}$

Fig. 8 - Reverse Recovery Waveform and Definitions

**ORDERING INFORMATION TABLE**

Device code	<b>VS-</b>	<b>1</b>	<b>E</b>	<b>F</b>	<b>H</b>	<b>01</b>	<b>H</b>	<b>M3</b>
	1	2	3	4	5	6	7	8

- 1** - Vishay Semiconductors product
- 2** - Current rating (1 = 1 A)
- 3** - Circuit configuration:  
E = single diode
- 4** - F = SMF package
- 5** - Process type,  
H = hyperfast recovery
- 6** - Voltage code (01 = 100 V)
- 7** - H = AEC-Q101 qualified
- 8** - M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free

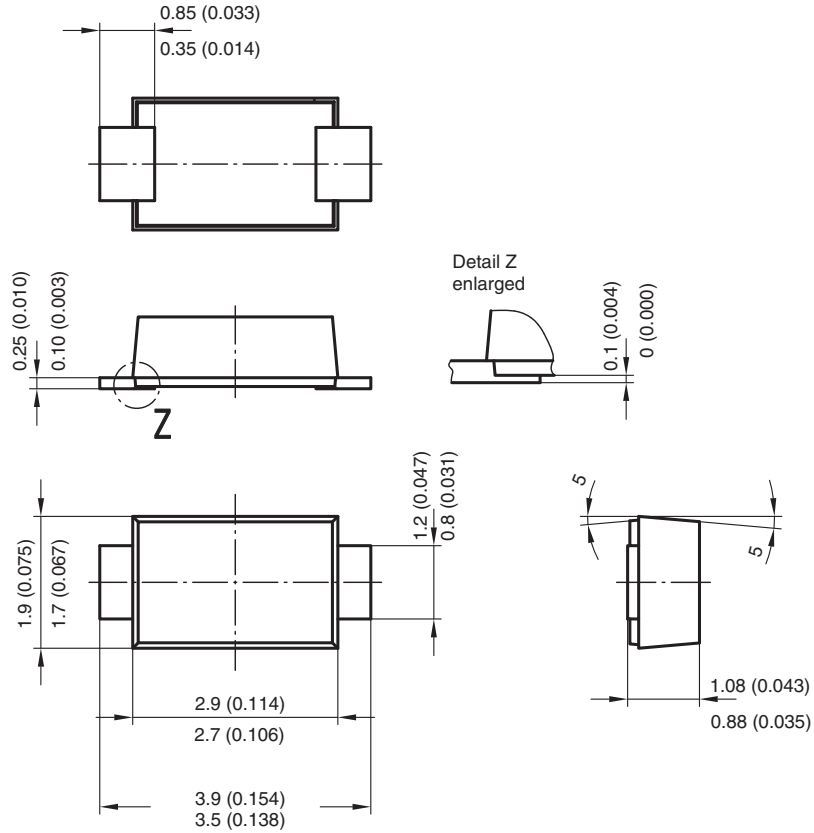
<b>ORDERING INFORMATION (Example)</b>			
PREFERRED P/N	QUANTITY PER REEL	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-1EFH01HM3/I	10 000	10 000	13" diameter plastic tape and reel

<b>LINKS TO RELATED DOCUMENTS</b>	
Dimensions	<a href="http://www.vishay.com/doc?95572">www.vishay.com/doc?95572</a>
Part marking information	<a href="http://www.vishay.com/doc?95618">www.vishay.com/doc?95618</a>
Packaging information	<a href="http://www.vishay.com/doc?95577">www.vishay.com/doc?95577</a>
SPIICE model	<a href="http://www.vishay.com/doc?96012">www.vishay.com/doc?96012</a>

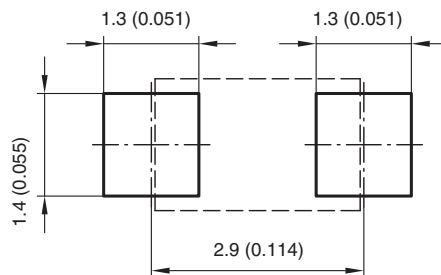


## SMF (DO-219AB)

**DIMENSIONS** in millimeters (inches)



Foot print recommendation:



Created - Date: 15. February 2005  
Rev. 3 - Date: 13. March 2007  
Document no.:S8-V-3915.01-001 (4)  
17247



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