# FlipKY®, Chip Scale Package Schottky Barrier Rectifier, 0.5 A

FlipKY®

## FEATURES

- Ultra low $V_F$ to footprint area
- Very low profile (< 0.6 mm)
- Low thermal resistance
- Supplied tested and on tape and reel
- Compliant to RoHS Directive 2002/95/EC

Pb-free

e3

RoHS COMPLIANT

## APPLICATIONS

- Reverse polarity protection
- Current steering
- Freewheeling
- Flyback
- Oring

| PRODUCT SUMMARY | |
|---|---|
| $I_{F(AV)}$ | 0.5 A |
| $V_R$ | 30 V |
| $V_F$ at $I_F$ | 0.33 V |
| $I_{RM}$ max. at 25 °C | 50 µA |
| $I_{RM}$ max. at 125 °C | 15 mA |
| $T_J$ max. | 150 °C |
| $E_{AS}$ | 5 mJ |

## DESCRIPTION

Vishay's FlipKY® product family utilizes wafer level chip scale packaging to deliver Schottky diodes with the lowest $V_F$ to PCB footprint area in industry. The three pad 0.9 mm x 1.2 mm devices can deliver up to 0.5 A and occupy only 1.08 $mm^2$ of board space. The anode and cathode connections are made through solder bump pads on one side of the silicon enabling designers to strategically place the diodes on the PCB. This design not only minimizes board space but also reduces thermal resistance and inductance, which can improve overall circuit efficiency.

Typical applications include hand-held, portable equipment such as cell phones, MP3 players, bluetooth, GPS, PDAs, and portable hard disk drives where space savings and performance are crucial.

| MAJOR RATINGS AND CHARACTERISTICS | | | |
|---|---|---|---|
| SYMBOL | CHARACTERISTICS | MAX. | UNITS |
| $V_{RRM}$ | | 30 | V |
| $I_{F(AV)}$ | Rectangular waveform | 0.5 | A |
| $I_{FSM}$ | | 190 | |
| $V_F$ | 0.5 $A_{pk}$, $T_J$ = 125 °C | 0.33 | V |
| $T_J$ | | - 55 to 150 | °C |

| VOLTAGE RATINGS | | | |
|---|---|---|---|
| PARAMETER | SYMBOL | VS-FCSP0530TR | UNITS |
| Maximum DC reverse voltage | $V_R$ | 30 | V |
| Maximum working peak reverse voltage | $V_{RWM}$ | | |

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | TEST CONDITIONS | | VALUES | UNITS |
|---|---|---|---|---|---|
| Maximum average forward current | $I_{F(AV)}$ | 50 % duty cycle at $T_{PCB}$ = 133 °C, rectangular waveform | | 0.5 | A |
| Maximum peak one cycle non-repetitive surge current at 25 °C | $I_{FSM}$ | 5 µs sine or 3 µs rect. pulse | Following any rated load condition and with rated $V_{RRM}$ applied | 190 | |
| | | 10 ms sine or 6 ms rect. pulse | | 10 | |
| Non-repetitive avalanche energy | $E_{AS}$ | $T_J$ = 25 °C, $I_{AS}$ = 2.0 A, L = 5.0 mH | | 5 | mJ |
| Repetitive avalanche current | $I_{AR}$ | Current decaying linearly to zero in 1 µs<br>Frequency limited by $T_J$ maximum $V_A$ = 1.5 x $V_R$ typical | | 0.5 | A |

## ELECTRICAL SPECIFICATIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Maximum forward voltage drop See fig. 1 | $V_{FM}$ (1) | 0.5 A | $T_J$ = 25 °C | 0.40 | 0.44 | V |
| | | 1 A | | 0.45 | 0.49 | |
| | | 0.5 A | $T_J$ = 125 °C | 0.29 | 0.33 | |
| | | 1 A | | 0.36 | 0.39 | |
| Maximum reverse leakage current See fig. 2 | $I_{RM}$ (1) | $T_J$ = 25 °C | $V_R$ = Rated $V_R$ | 10 | 50 | µA |
| | | $T_J$ = 125 °C | | 5 | 15 | mA |
| Maximum junction capacitance | $C_T$ | $V_R$ = 5 $V_{DC}$ (test signal range 100 kHz to 1 MHz), 25 °C | | - | 90 | pF |
| Maximum voltage rate of change | dV/dt | Rated $V_R$ | | - | 10 000 | V/µs |

**Note**

(1) Pulse width < 300 µs, duty cycle < 2 %

## THERMAL - MECHANICAL SPECIFICATIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | VALUES | UNITS |
|---|---|---|---|---|
| Maximum junction and storage temperature range | $T_J$ (1), $T_{Stg}$ | | - 55 to 150 | °C |
| Typical thermal resistance, junction to PCB | $R_{thJL}$ (2) | DC operation | 35 | °C/W |
| Typical thermal resistance, junction to ambient | $R_{thJA}$ | | 150 | |

**Notes**

(1) $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$ thermal runaway condition for a diode on its own heatsink

(2) Mounted on minimum footprint PCB

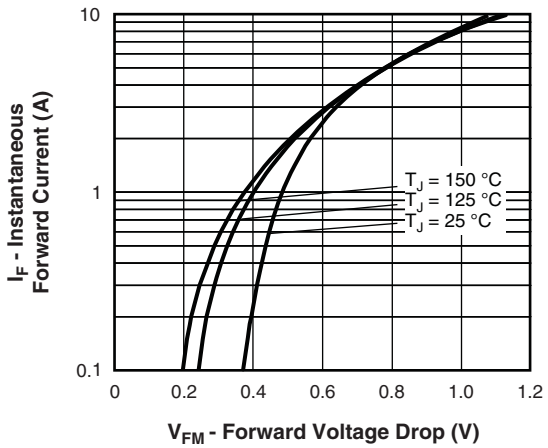



Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

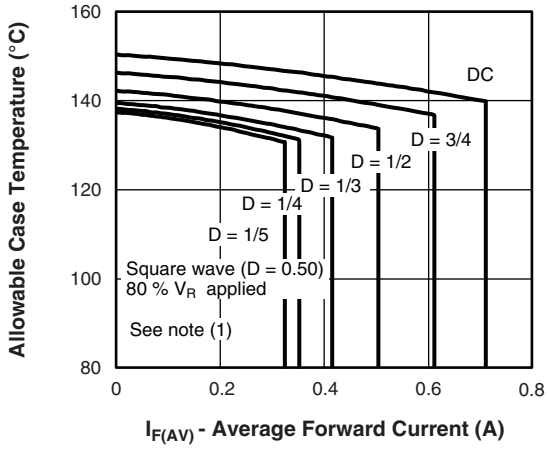



Fig. 4 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

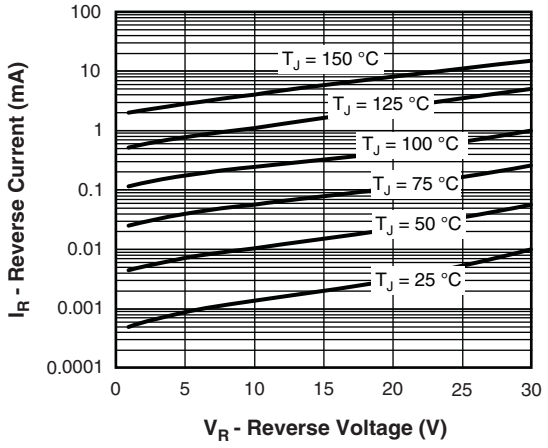



Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

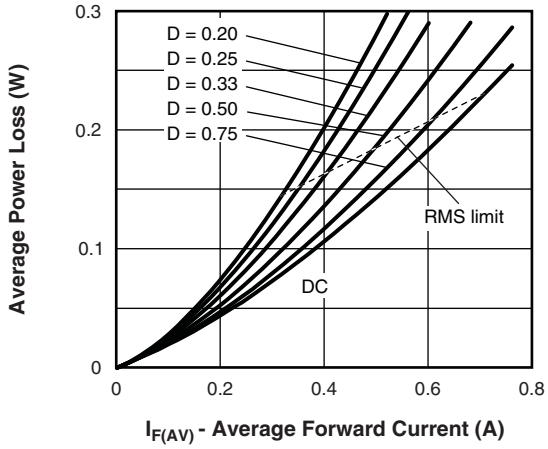



Fig. 5 - Forward Power Loss Characteristics (Per Leg)

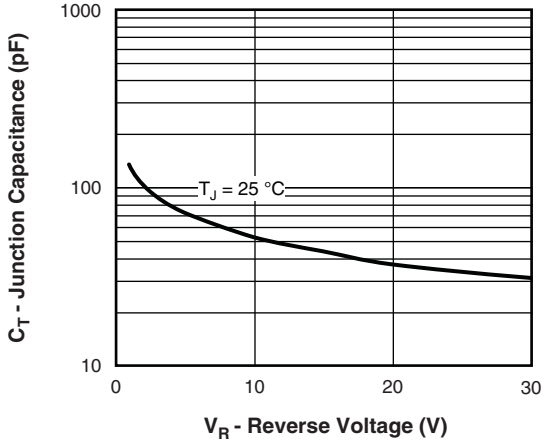



Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

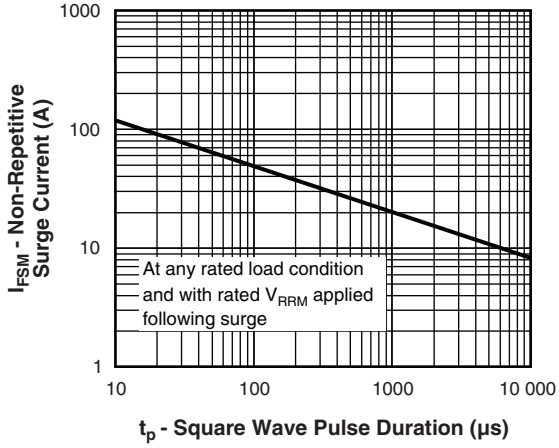



Fig. 6 - Maximum Non-Repetitive Surge Current (Per Leg)

**Note**

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$;
Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}$/D) (see fig. 6); $Pd_{REV}$ = Inverse power loss = $V_{R1} \times I_R$ (1 - D); $I_R$ at 80 % $V_R$ applied

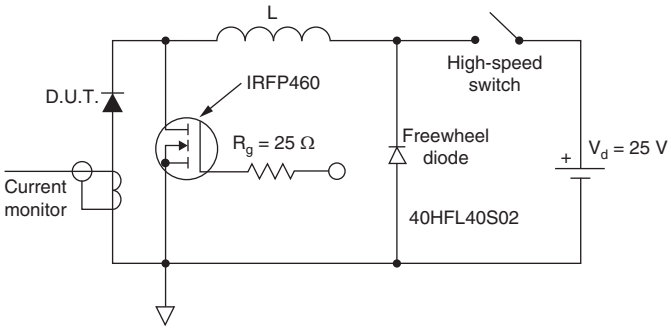
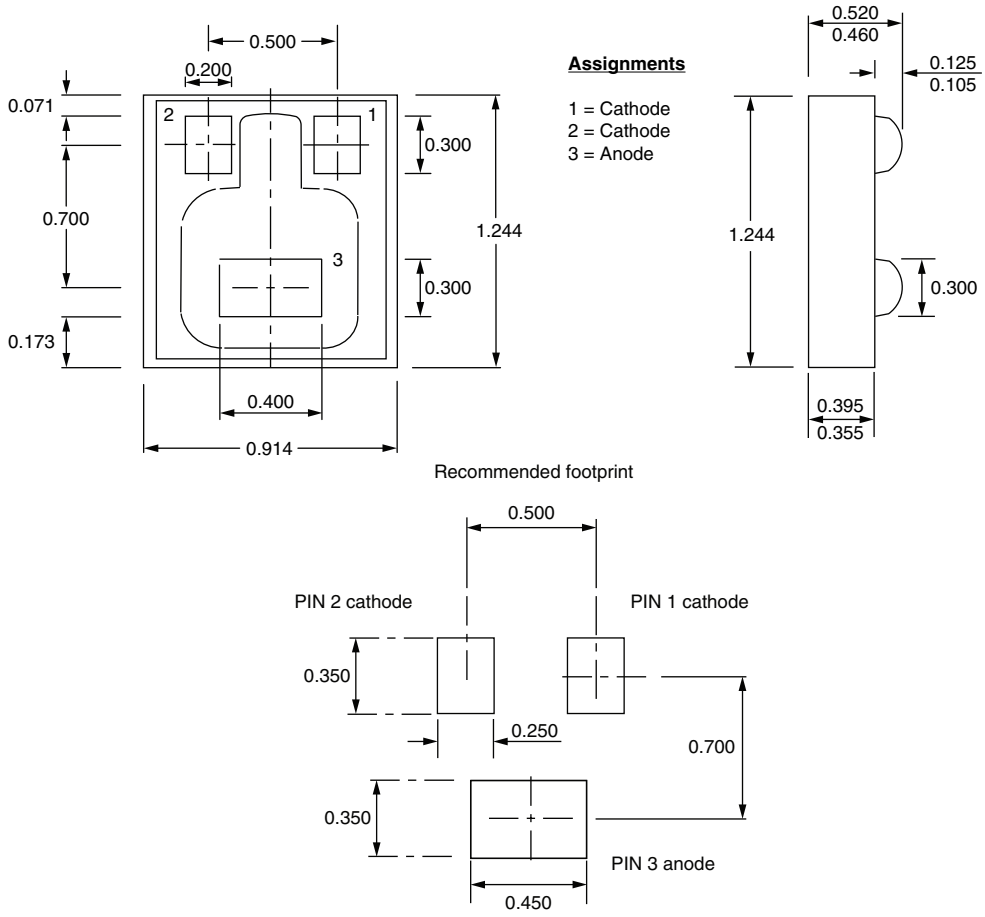



Fig. 7 - Unclamped Inductive Test Circuit

| LINKS TO RELATED DOCUMENTS | |
|---|---|
| Dimensions | www.vishay.com/doc?95049 |
| Part marking information | www.vishay.com/doc?95060 |
| Packaging information | www.vishay.com/doc?95062 |

# FlipKY® 0.5 A/0.75 A

**DIMENSIONS** in millimeters




**Notes**

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Controlling dimension: millimeter

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