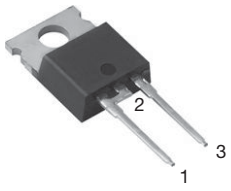
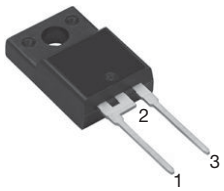
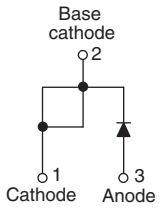
Hyperfast Rectifier, 15 A FRED Pt®



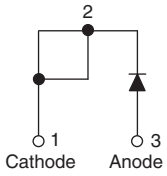
TO-220AC



TO-220 FullPAK



VS-15ETX06PbF
VS-15ETX06-N3



VS-15ETX06FPPbF
VS-15ETX06FP-N3

FEATURES

- Hyperfast recovery time
- Low forward voltage drop
- 175 °C operating junction temperature
- Benchmark ultralow forward voltage drop
- Low leakage current
- Fully isolated package (V_{INS} = 2500 V_{RMS})
- UL E78996 approved
- Designed and qualified according to JEDEC®-JESD 47
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
e3
RoHS COMPLIANT
HALOGEN FREE Available

DESCRIPTION / APPLICATIONS

State of the art hyperfast recovery rectifiers designed with optimized performance of forward voltage drop, hyperfast recovery time, and soft recovery.
The planar structure and the platinum doped life time control guarantee the best overall performance, ruggedness and reliability characteristics.
These devices are intended for use in PFC boost stage in the AC/DC section of SMPS, inverters or as freewheeling diodes.
Their extremely optimized stored charge and low recovery current minimize the switching losses and reduce over dissipation in the switching element and snubbers.

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	15 A
V_R	600 V
V_F at I_F	1.5 V
t_{rr} typ.	18 ns
T_J max.	175 °C
Package	TO-220AC, TO-220FullPAK
Circuit configuration	Single

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM}		600	V
Average rectified forward current	$I_{F(AV)}$	T_C = 133 °C	15	A
		T_C = 62 °C (FullPAK)		
Non-repetitive peak surge current	I_{FSM}	T_J = 25 °C	170	
Peak repetitive forward current	I_{FM}		30	
Operating junction and storage temperatures	T_J, T_{Stg}		-65 to +175	°C

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Breakdown voltage, blocking voltage	V_{BR}, V_R	I_R = 100 µA	600	-	-	V
Forward voltage	V_F	I_F = 15 A	-	2.3	3.2	
		I_F = 15 A, T_J = 150 °C	-	1.5	1.8	
Reverse leakage current	I_R	V_R = V_R rated	-	0.1	50	µA
		T_J = 150 °C, V_R = V_R rated	-	40	300	
Junction capacitance	C_T	V_R = 600 V	-	20	-	pF
Series inductance	L_S	Measured lead to lead 5 mm from package body	-	8.0	-	nH

For technical questions within your region: DiodesAmericas@vishay.com, DiodesAsia@vishay.com, DiodesEurope@vishay.com

DYNAMIC RECOVERY CHARACTERISTICS (T_C = 25 °C unless otherwise specified)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNITS**
Reverse recovery time	t_{rr}	I_F = 1 A, dI_F/dt = 100 A/µs, V_R = 30 V		-	18	22	ns
		I_F = 15 A, dI_F/dt = 100 A/µs, V_R = 30 V		-	20	32	
		T_J = 25 °C	I_F = 15 A dI_F/dt = 200 A/µs V_R = 390 V	-	22	-	
		T_J = 125 °C		-	52	-	
Peak recovery current	I_{RRM}	T_J = 25 °C		-	2.4	-	A
		T_J = 125 °C		-	5.1	-	
Reverse recovery charge	Q_{rr}	T_J = 25 °C		-	25	-	C
		T_J = 125 °C		-	150	-	
Reverse recovery time	t_{rr}	T_J = 125 °C	I_F = 15 A dI_F/dt = 800 A/µs V_R = 390 V	-	37	-	ns
Peak recovery current	I_{RRM}			-	16	-	A
Reverse recovery charge	Q_{rr}			-	350	-	nC

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Maximum junction and storage temperature range	T_J, T_{Stg}		-65	-	175	°C
Thermal resistance, junction to case	R_{thJC}		-	1.0	1.3	°C/W
(FULL-PAK)			-	3.0	3.5	
Thermal resistance, junction to ambient per leg	R_{thJA}	Typical socket mount	-	-	70	
Thermal resistance, case to heatsink	R_{thCS}	Mounting surface, flat, smooth and greased	-	0.5	-	
Weight			-	2.0	-	g
			-	0.07	-	oz.
Mounting torque			6.0 (5.0)	-	12 (10)	kgf · cm (lbf · in)
Marking device		Case style TO-220AC	15ETX06			
		Case style TO-220 FullPAK	15ETX06FP			

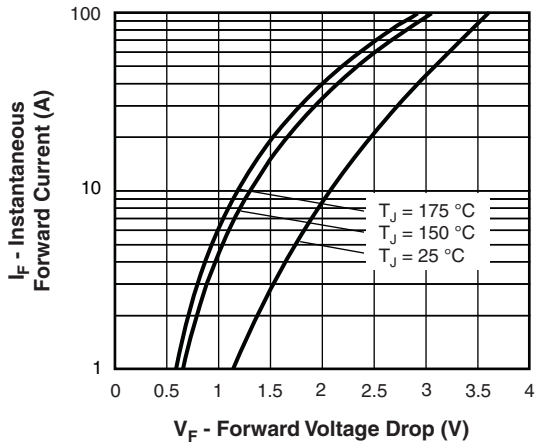


Fig. 1 - Typical Forward Voltage Drop Characteristics

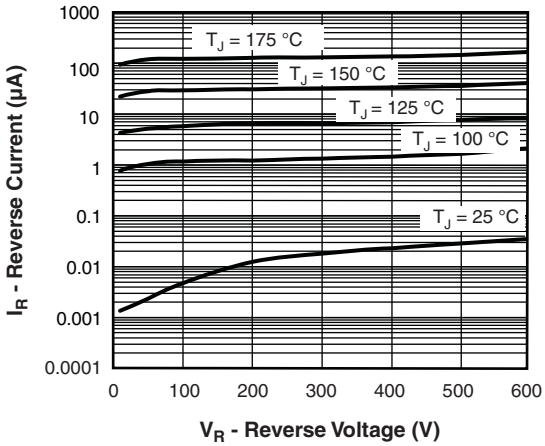


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

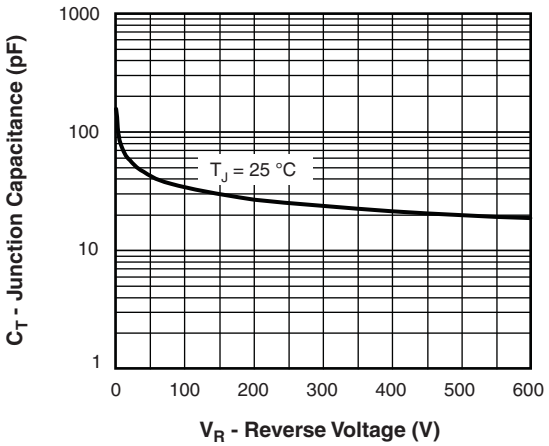


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

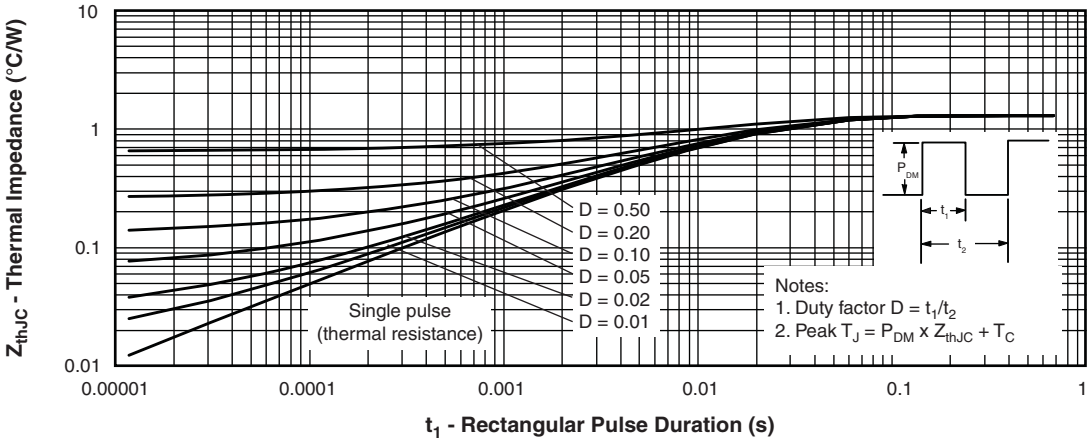


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

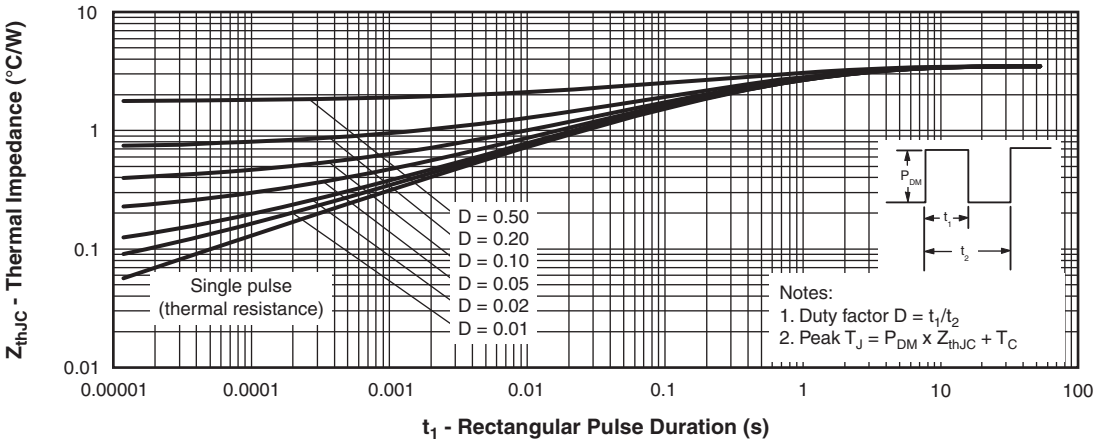


Fig. 5 - Maximum Thermal Impedance Z_{thJC} Characteristics (FullPAK)

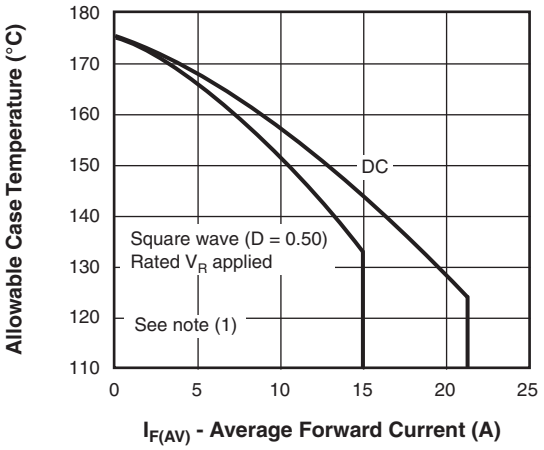


Fig. 6 - Maximum Allowable Case Temperature vs. Average Forward Current

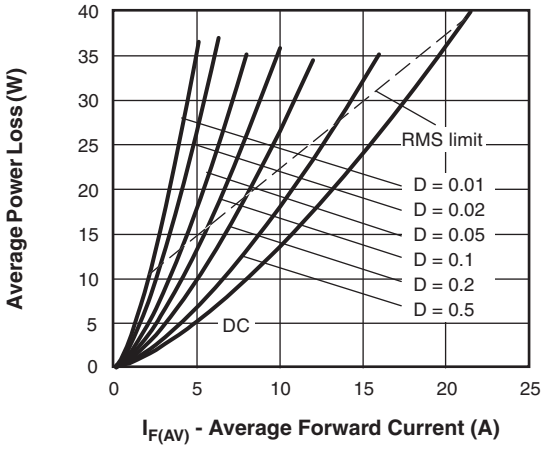


Fig. 8 - Forward Power Loss Characteristics

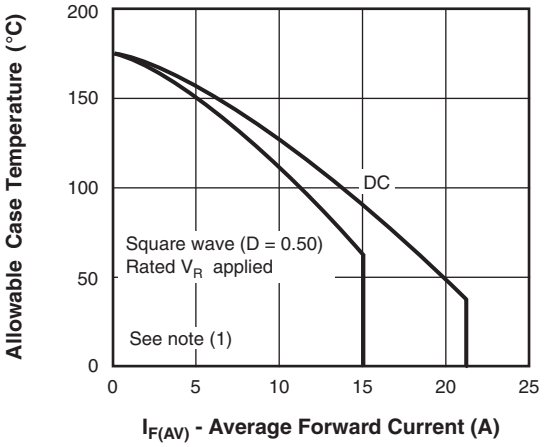


Fig. 7 - Maximum Allowable Case Temperature vs. Average Forward Current (FullPAK)

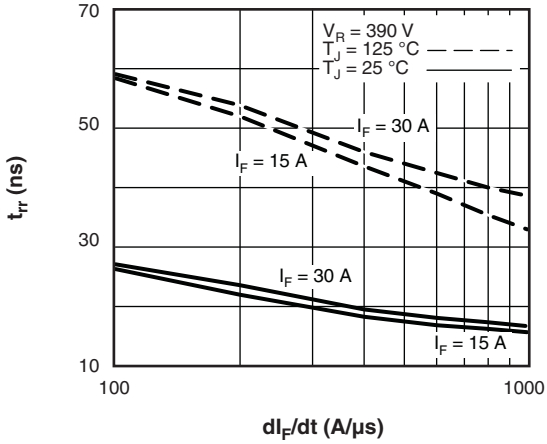


Fig. 9 - Typical Reverse Recovery Time vs. dI_F/dt

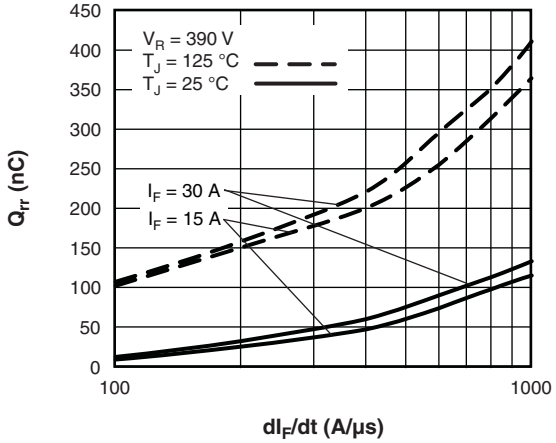


Fig. 10 - Typical Stored Charge vs. dI_F/dt

Note

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$;
Pd = forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}$/D) (see fig. 8);
Pd_{REV} = inverse power loss = $V_{R1} \times I_R$ (1 - D); I_R at V_{R1} = rated V_R

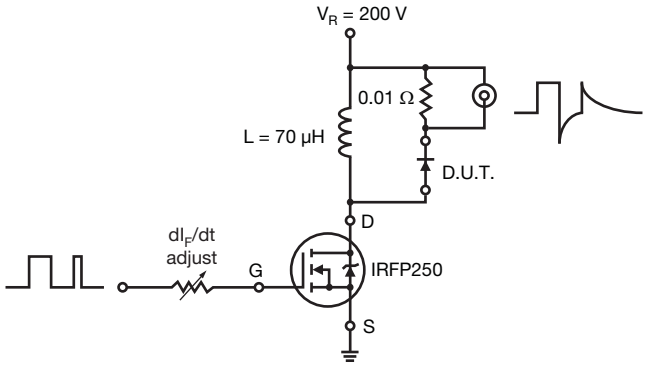
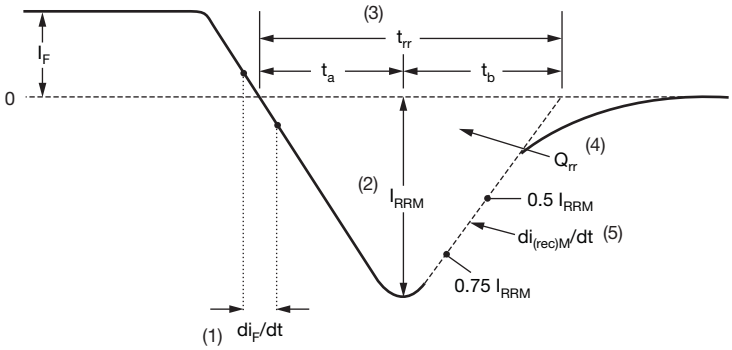


Fig. 11 - Reverse Recovery Parameter Test Circuit



(1) di_F/dt - rate of change of current through zero crossing

(2) I_{RRM} - peak reverse recovery current

(3) t_{rr} - reverse recovery time measured from zero crossing point of negative going I_F to point where a line passing through 0.75 I_{RRM} and 0.50 I_{RRM} extrapolated to zero current.

(4) Q_{rr} - area under curve defined by t_{rr} and I_{RRM}

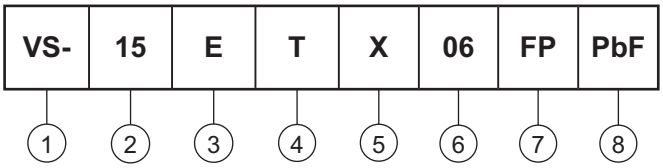
$$Q_{rr} = \frac{t_{rr} \times I_{RRM}}{2}$$

(5) $di_{(rec)M}/dt$ - peak rate of change of current during t_b portion of t_{rr}

Fig. 12 - Reverse Recovery Waveform and Definitions

ORDERING INFORMATION TABLE

Device code

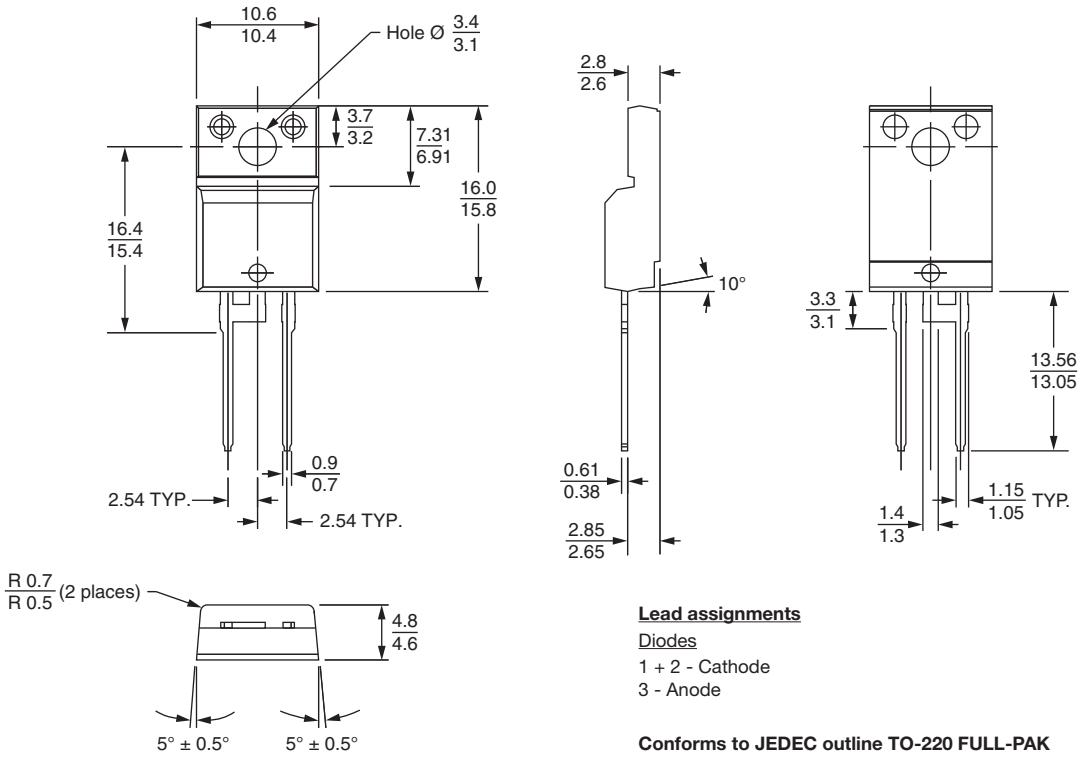


1 - Vishay Semiconductors product
2 - Current rating (15 = 15 A)
3 - E = single diode
4 - T = TO-220, D^2PAK
5 - X = hyperfast recovery
6 - Voltage rating (06 = 600 V)
7 - • None = TO-220AC
• FP = TO-220 FullPAK
8 - Environmental digit:
PbF = lead (Pb)-free and RoHS-compliant
-N3 = halogen-free, RoHS-compliant, and totally lead (Pb)-free

ORDERING INFORMATION (Example)			
PREFERRED P/N	**QUANTITY PER T/R**	**MINIMUM ORDER QUANTITY**	**PACKAGING DESCRIPTION**
VS-15ETX06PbF	50	1000	Antistatic plastic tube
VS-15ETX06-N3	50	1000	Antistatic plastic tube
VS-15ETX06FPPbF	50	1000	Antistatic plastic tube
VS-15ETX06FP-N3	50	1000	Antistatic plastic tube

LINKS TO RELATED DOCUMENTS		
Dimensions	TO-220AC	www.vishay.com/doc?95221
	TO-220FP	www.vishay.com/doc?95005
Part marking information	TO-220ACPbF	www.vishay.com/doc?95224
	TO-220AC-N3	www.vishay.com/doc?95068
	TO-220AFPPbF	www.vishay.com/doc?95009
	TO-220FP-N3	www.vishay.com/doc?95440
SPICE model	TO-220AC	www.vishay.com/doc?96377
	TO-220FP	www.vishay.com/doc?96385

DIMENSIONS in millimeters



Lead assignments

Diodes

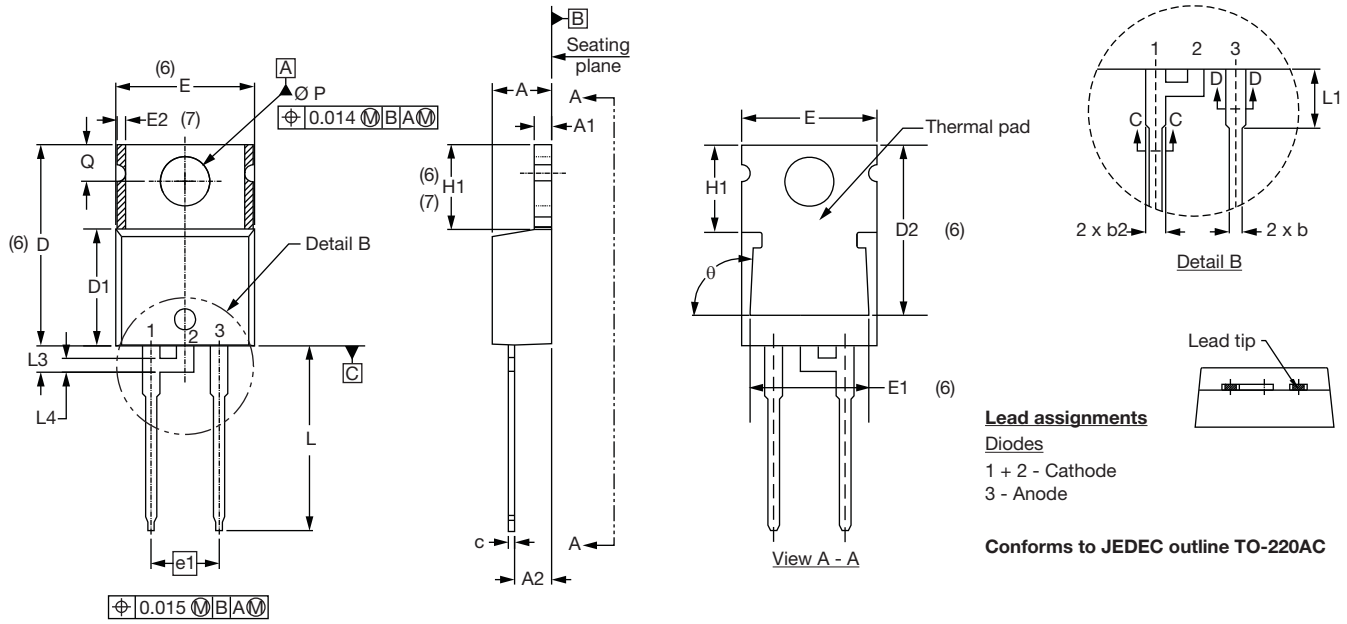
1 + 2 - Cathode

3 - Anode

Conforms to JEDEC outline TO-220 FULL-PAK

TO-220AC

DIMENSIONS in millimeters and inches



Lead assignments

Diodes

1 + 2 - Cathode

3 - Anode

Conforms to JEDEC outline TO-220AC

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
c	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
E	10.11	10.51	0.398	0.414	3, 6

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
e	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
L3	1.78	2.13	0.070	0.084	
L4	0.76	1.27	0.030	0.050	2
Ø P	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° to 93°		90° to 93°		

Notes

(1) Dimensioning and tolerancing as per ASME Y14.5M-1994
(2) Lead dimension and finish uncontrolled in L1
(3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
(4) Dimension b1, b3 and c1 apply to base metal only
(5) Controlling dimension: inches
(6) Thermal pad contour optional within dimensions E, H1, D2 and E1
(7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
(8) Outline conforms to JEDEC TO-220, D2 (minimum) where dimensions are derived from the actual package outline

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