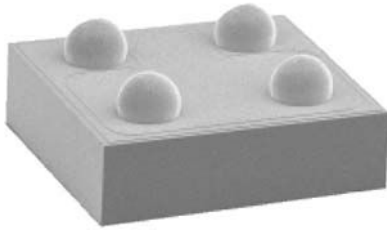




# FlipKY®, 1 A Chip Scale Package Schottky Barrier Rectifier



FlipKY®

### FEATURES

- Super low profile (0.6 mm)
- One-fifth footprint of SMA
- Ultralow  $V_F$  per footprint area
- Low leakage
- Low thermal resistance
- Available tested on tape and reel
- Compliant to RoHS Directive 2002/95/EC



RoHS  
COMPLIANT

### APPLICATIONS

- Reverse polarity protection
- Current steering
- Freewheeling
- Flyback
- Oring

### DESCRIPTION

Vishay's FlipKY® product family utilizes wafer level chip scale packaging to deliver Schottky diodes with the lowest  $V_F$  to PCB footprint area in industry. The four bump 1.5 mm x 1.5 mm devices can deliver up to 1 A and occupy only 2.3 mm<sup>2</sup> of board space. The anode and cathode connections are made through solder bump pads on one side of the silicon enabling designers to strategically place the diodes on the PCB. This design not only minimizes board space but also reduces thermal resistance and inductance, which can improve overall circuit efficiency.

Typical applications include hand-held, portable equipment such as cell phones, MP3 players, bluetooth, GPS, PDAs, and portable hard disk drives where space savings and performance are crucial.

PRODUCT SUMMARY	
$I_{F(AV)}$	1 A
$V_R$	40 V
$V_F$ at $I_F$	0.42 V
$I_{RM}$ max. at 25 °C	15 $\mu$ A
$I_{RM}$ max. at 125 °C	4 mA
$T_J$ max.	150 °C
$E_{AS}$	10 mJ

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	MAX.	UNITS
$V_{RRM}$		40	V
$I_{F(AV)}$	Rectangular waveform	1	A
$I_{FSM}$		250	
$V_F$	1 Apk, $T_J = 125$ °C	0.42	V
$T_J$		- 55 to 150	°C

VOLTAGE RATINGS			
PARAMETER	SYMBOL	VS-FCSP1H40LTR	UNITS
Maximum DC reverse voltage	$V_R$	40	V
Maximum working peak reverse voltage	$V_{RWM}$		



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	$I_{F(AV)}$	50 % duty cycle at $T_{PCB} = 117\text{ °C}$ , rectangular waveform		1.0	A
Maximum peak one cycle non-repetitive surge current at 25 °C	$I_{FSM}$	5 $\mu$ s sine or 3 $\mu$ s rect. pulse	Following any rated load condition and with rated $V_{RRM}$ applied	250	
		10 ms sine or 6 ms rect. pulse		21	
Non-repetitive avalanche energy	$E_{AS}$	$T_J = 25\text{ °C}$ , $I_{AS} = 2.0\text{ A}$ , $L = 5.0\text{ mH}$		10	mJ
Repetitive avalanche current	$I_{AR}$	Current decaying linearly to zero in 1 $\mu$ s Frequency limited by $T_J$ maximum $V_A = 1.5 \times V_R$ typical		2.0	A

ELECTRICAL SPECIFICATIONS ( $T_J = 25\text{ °C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum forward voltage drop See fig. 1	$V_{FM}^{(1)}$	1 A	$T_J = 25\text{ °C}$	0.48	0.52	V
		2 A		0.54	0.59	
		1 A	$T_J = 125\text{ °C}$	0.38	0.42	
		2 A		0.48	0.52	
Maximum reverse leakage current See fig. 2	$I_{RM}^{(1)}$	$T_J = 25\text{ °C}$	$V_R = \text{Rated } V_R$	3	15	$\mu$ A
			$V_R = 20\text{ V}$	0.5	1	
			$V_R = 10\text{ V}$	0.2	0.5	
			$V_R = 5\text{ V}$	0.15	0.3	
		$T_J = 125\text{ °C}$	$V_R = \text{Rated } V_R$	2.5	4	mA
			$V_R = 20\text{ V}$	0.9	2	
			$V_R = 10\text{ V}$	0.6	1.5	
			$V_R = 5\text{ V}$	0.5	1	
Maximum junction capacitance	$C_T$	$V_R = 5\text{ V}_{DC}$ (test signal range 100 kHz to 1 MHz), 25 °C		-	160	pF
Maximum voltage rate of charge	dV/dt	Rated $V_R$		-	10 000	V/ $\mu$ s

**Note**

(1) Pulse width < 300  $\mu$ s, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum junction and storage temperature range	$T_J^{(1)}$ , $T_{Stg}$			- 55 to 150	°C
Typical thermal resistance, junction to PCB	$R_{thJL}^{(2)}$	DC operation		40	°C/W
Maximum thermal resistance, junction to ambient	$R_{thJA}$			62	

**Notes**

(1)  $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$  thermal runaway condition for a diode on its own heatsink

(2) Mounted 1" square PCB

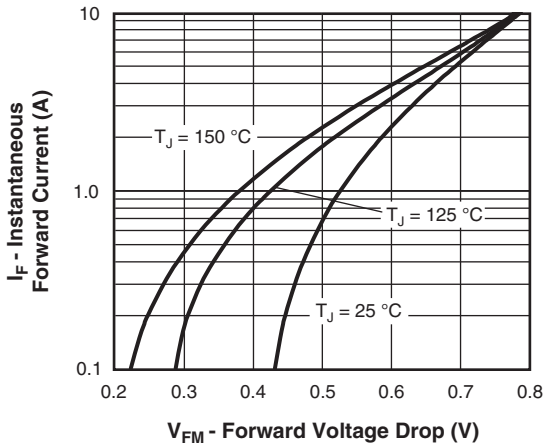


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

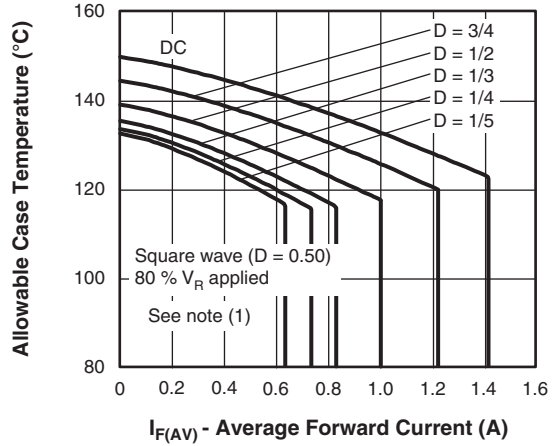


Fig. 4 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

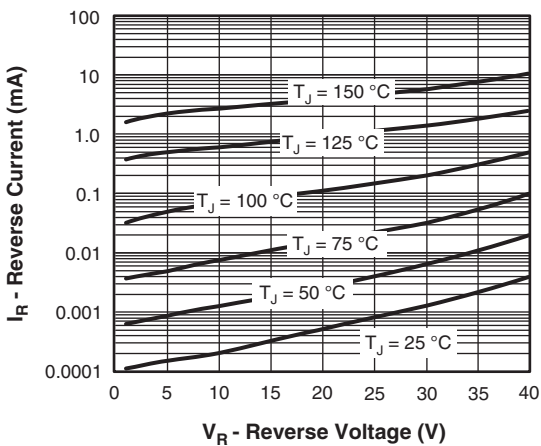


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

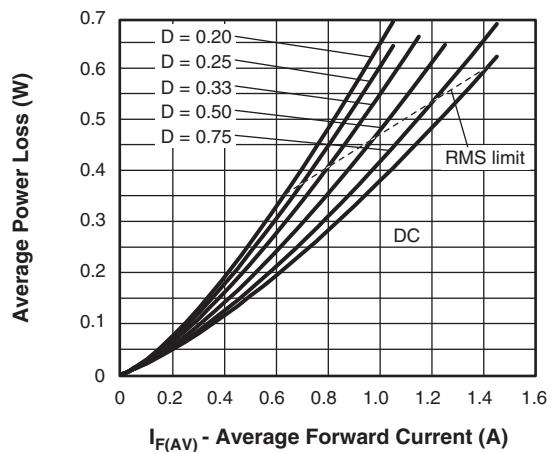


Fig. 5 - Forward Power Loss Characteristics (Per Leg)

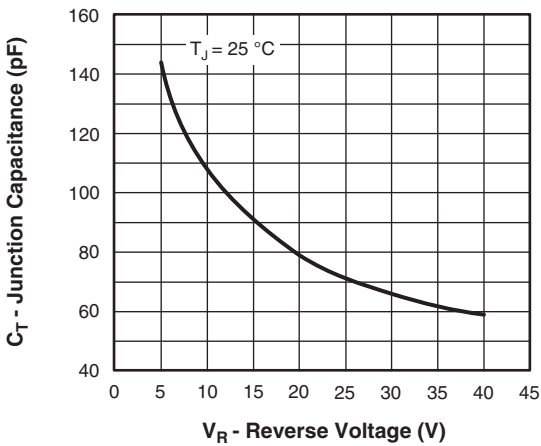


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

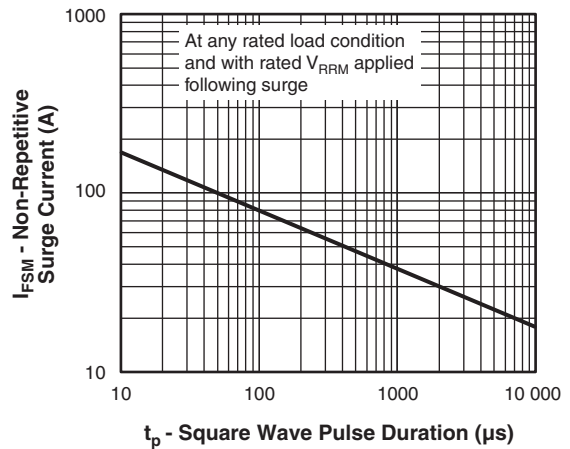


Fig. 6 - Maximum Non-Repetitive Surge Current (Per Leg)

**Note**

- (1) Formula used:  $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$ ;  
 $P_d$  = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);  $P_{dREV}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at 80 %  $V_R$  applied

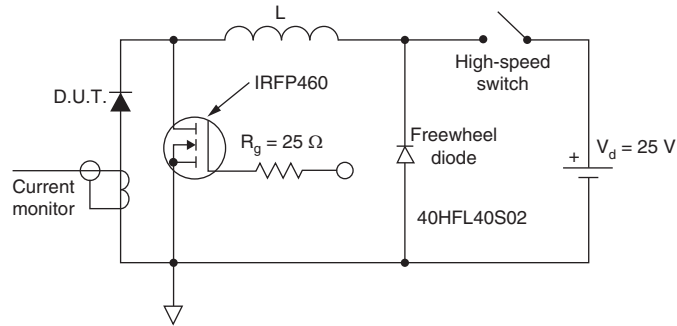


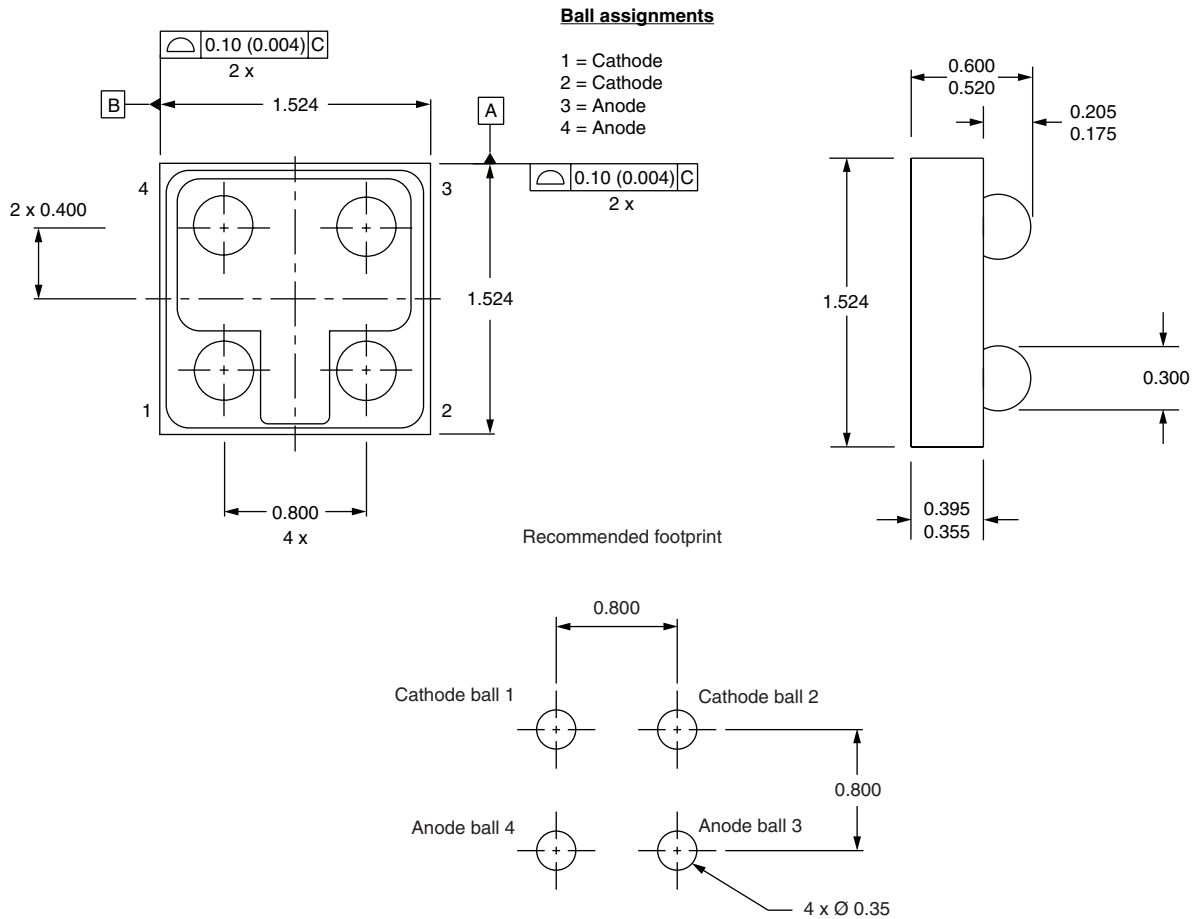
Fig. 7 - Unclamped Inductive Test Circuit

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95282">www.vishay.com/doc?95282</a>
Part marking information	<a href="http://www.vishay.com/doc?95281">www.vishay.com/doc?95281</a>
Packaging information	<a href="http://www.vishay.com/doc?95062">www.vishay.com/doc?95062</a>
SPICE model	<a href="http://www.vishay.com/doc?95421">www.vishay.com/doc?95421</a>



## FlipKY<sup>®</sup> 1 A/1.5 A (Large Bump Pad Design)

**DIMENSIONS** in millimeters



### Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Controlling dimension: millimeter



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