Cool-Power®
ZVS Switching Regulators
PI358x-00

30 – 60V_{IN} Cool-Power ZVS Buck Regulator

Product Description

The PI358x-00 is a family of high input voltage, wide-input-range DC-DC ZVS Buck regulators integrating controller and power switches within a high-density GQFN (UTAC's Grid-array QFN) package.

The integration of a high-performance Zero-Voltage Switching (ZVS) topology, within the PI358x-00 series, increases point-of-load performance providing best-in-class power efficiency.

Device	Output Voltage		I_{OUT} Max
	Set	Range	
PI3583-00-QFYZ	3.3V	2.2 – 4.0V	10A
PI3585-00-QFYZ	5.0V	3.8 – 6.5V	10A
PI3586-00-QFYZ	12.0V	6.5 – 14V	9A

Features & Benefits

- High-Efficiency HV ZVS Buck Topology
- Wide input voltage range of 30 – 60V
- Power up into pre-biased load < 6V
- Parallel capable with single-wire current sharing
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- Differential amplifier for output remote sensing
- User adjustable soft start & tracking
- –20 to 120°C operating range (T_{INT})

Applications

- HV to PoL Buck Regulator Applications
- Computing, Communications, Industrial, Automotive Equipment

Package Information

- 37-Pin GQFN

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Order Information

Product	Nominal Output	Rated I_{OUT}	Package	Transport Media
PI3583-00-QFYZ	3.3V	10A	7 x 8mm GQFN	TRAY
PI3585-00-QFYZ	5.0V	10A	7 x 8mm GQFN	TRAY
PI3586-00-QFYZ	12.0V	9A	7 x 8mm GQFN	TRAY

Thermal, Storage and Handling Information

Name	Rating
Storage Temperature	–65 to 150°C
Internal Operating Temperature	–20 to 120°C
Soldering Temperature for 30 seconds	260°C
MSL Rating	MSL3
ESD Rating, JESD22-A114F, JS-002-2014	500V HBM; 200V CDM, respectively

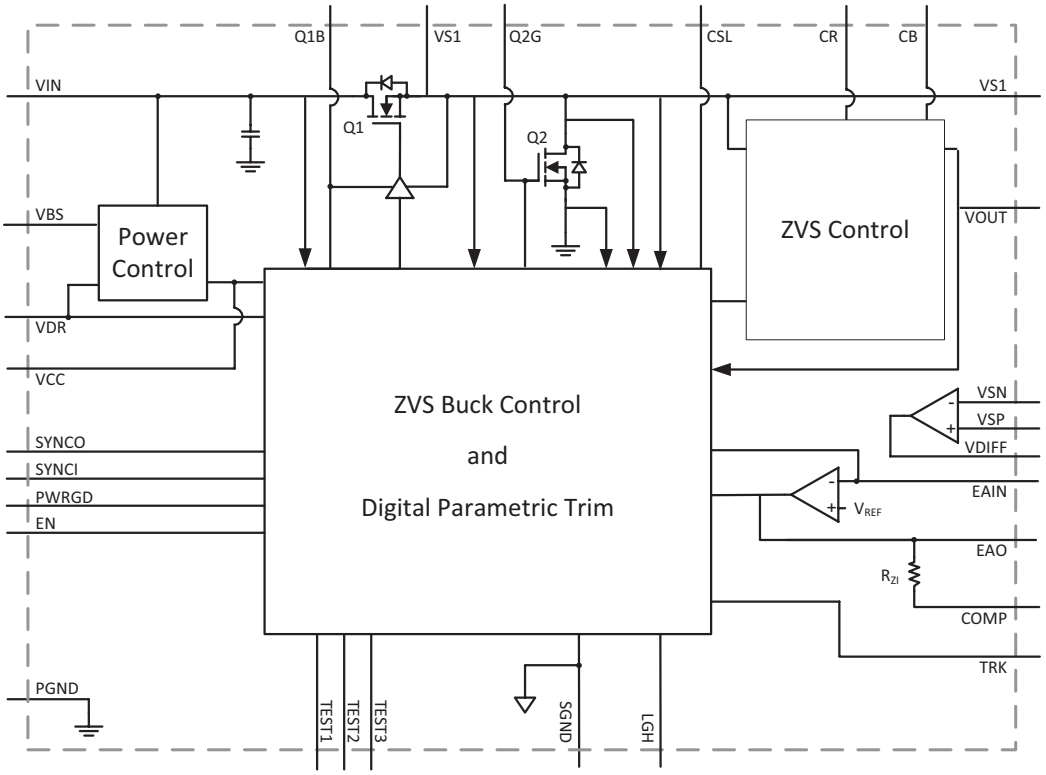
Absolute Maximum Ratings [a]

Name	Rating
V_{IN}	–0.7 to 75V
VS1	–6 [b] to 75V
V_{OUT}	–0.5 to 25V
CR	–0.7 to 25V
CB	–0.3 to 5.5V with respect to CR
Q1B	–0.3 to 5.5V with respect to VS1
VBS	–0.7 to 75V
Q2G	–0.5 to 5.5V
SGND	±100mA
TRK	–0.3 to 5.5V, ±30mA
VDR, VCC, SYNCI, SYNCO, PWRGD, EN, CC, CSL, COMP, EAO, EAIN, VDIFF, VSN, VSP, TESTx	–0.3 to 5.5V, ±5mA

[a] Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltages are referenced to PGND unless otherwise noted.

[b] Peak during switching transient.

Functional Block Diagram

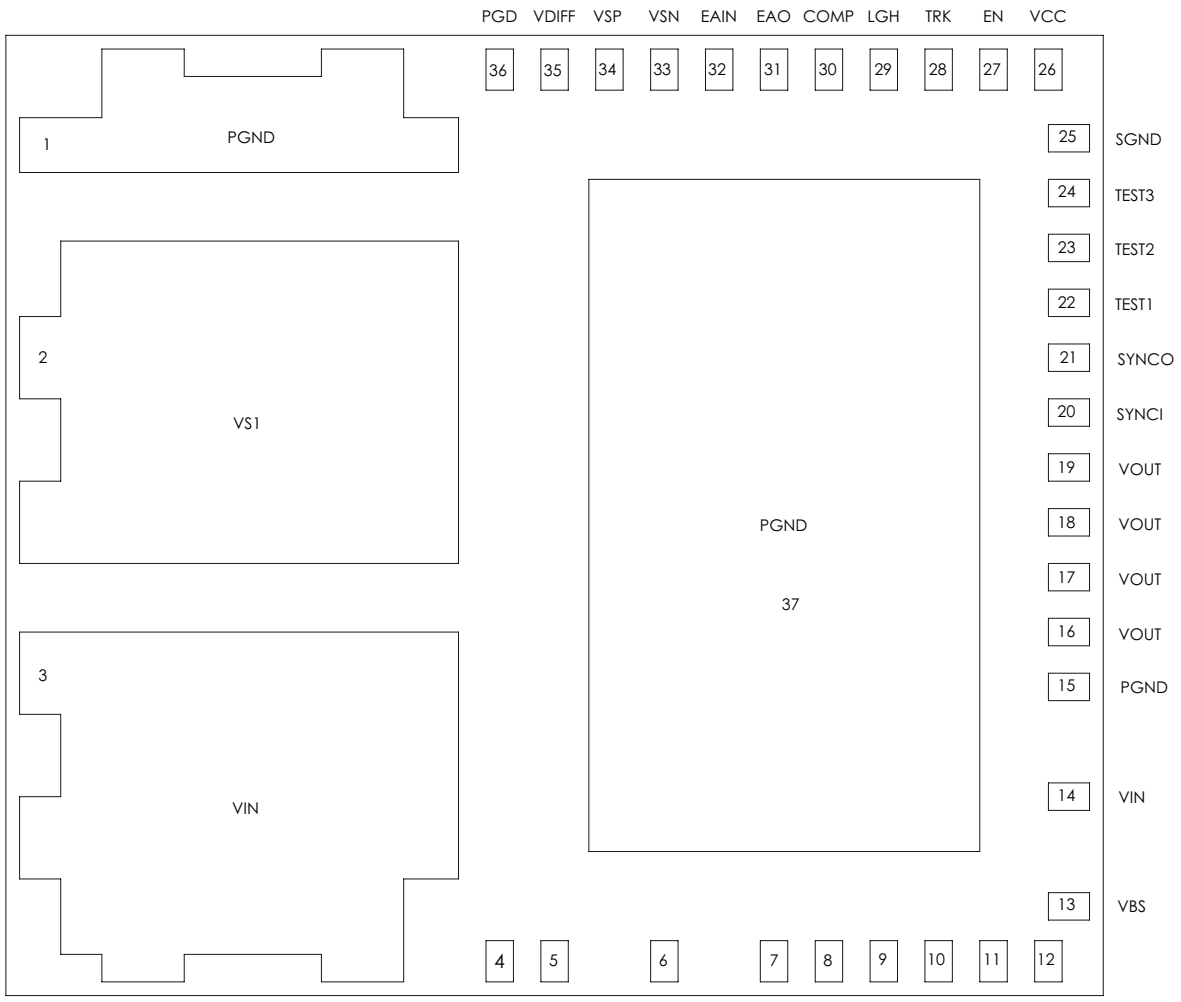


Simplified block diagram

Pin Description

Name	Location	I/O	Description
PGND	1, 15, 37	Power	**Power Ground:** VIN and VOUT power returns
VS1	2	Power	**Switching Node:** and ZVS sense for power switches. Requires a schottky diode clamp with a low inductance connection in parallel with an RC snubber for 1nF and 0.3Ω. Refer to Table 1 for the recommended components.
VIN	3	Power	**Input Voltage:** for the power stage.
	14	Power	**Input Voltage:** and sense for UVLO, OVLO and feed forward ramp.
CR	4	Power	ZVS control function node. Requires a 40V schottky diode clamp to PGND. Refer to Table 1 for the recommended component.
CB	5	Power	ZVS control function node. Decouple with a 0.047µF capacitor between CB and CR. Refer to Table 1 for the recommended component.
Q1B	6	Power	Q1 driver boost pin. Decouple with a 0.22µF capacitor in series with a 1.3Ω resistor between Q1B and VS1. Refer to Table 1 for the recommended components.
CSL	7	Power	ZVS control function node. Connect to PGND.
Q2G	8	Power	Q2 gate drive. Leave open.
VDR	9	I/O	**Gate Driver VCC:** 5.1V gate driver bias supply. May be used as a bias supply for low power external loads. See Application Description for important considerations.
N/C	10-12	I/O	No Internal connection.
VBS	13	Power	Switching node for gate driver bias supply.
VOUT	16-19	Power	**Output Voltage:** Internal Clamp connection and sense for power switches and feed-forward ramp.
SYNCI	20	I	**Synchronization Input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use. The PI358x-00 family is not optimized for external synchronization functionality.
SYNCO	21	O	**Synchronization Output:** Outputs a high signal at the start of each clock cycle for the longer of ½ of the minimum period or the on time of the high-side power MOSFET.
TEST1	22	I/O	**Factory Test:** Use only with factory guidance. Connect to SGND for proper operation.
TEST2	23	I/O	**Factory Test:** Use only with factory guidance. Connect to SGND for proper operation.
TEST3	24	I/O	**Factory Test:** Use only with factory guidance. Leave open.
SGND	25	I/O	**Signal Ground:** Internal logic ground for EAO, EAIN, TRK, SYNCI, SYNCO communication returns. SGND and PGND are not connected inside the package. SGND should be connected to the large PGND island (controller paddle, pin 37) directly under the PI358x package. Sensitive analog nodes should be connected to the SGND side of the connection.
VCC	26	I/O	**Control Circuitry VCC:** Analog & digital bias. Decouple with 2.2µF to SGND.
EN	27	I/O	**Enable Input:** Regulator enable control. Asserted high or left floating – regulator enabled; Asserted low – regulator output disabled.
TRK	28	I	**Soft Start and Track Input:** An external capacitor with minimum capacitance of 47nF is required to be connected between TRK pin and SGND to control the rate of rise during soft start.
LGH	29	I/O	For factory use only. Connect to SGND in application.
COMP	30	O	**Compensation Capacitor:** Connect capacitor for control loop dominant pole. See Error Amplifier section for details. A default C_{COMP} of 4.7nF is used in the example.
EAO	31	O	**Error Amplifier Output:** External connection for additional compensation and current sharing.
EAIN	32	I	**Error Amplifier Inverting Input:** Connection for the feedback divider tap.
VSN	33	I	**Independent Amplifier Inverting Input:** If unused connect in unity gain.
VSP	34	I	**Independent Amplifier Non-Inverting Input:** If unused connect to SGND.
VDIFF	35	O	**Independent Amplifier Output:** Active only when module is enabled.
PWRGD	36	O	**Power Good:** High impedance when regulator is operating and VOUT is in regulation. Otherwise pulls to SGND.

Package Pinout



PI358x

TOP THROUGH VIEW OF PRODUCT

GQFN PACKAGE

PI358x-00 Common Electrical Characteristics

Specifications apply for –20°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted. [c]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Amp						
Open Loop Gain		[d]	96	120	140	dB
Small Signal Gain-Bandwidth		[d]	5	7	12	MHz
Input Offset Error				0.5	1	mV
Common-Mode Input Range			–0.1		2.5	V
Differential-Mode Input Range					2	V
Input Bias Current			–1		1	µA
Sink/Source Current			–1		1	mA
Maximum V_{OUT}		I_{VDIFF} = –1mA	4.85			V
Minimum V_{OUT}		I_{VDIFF} = –1mA			20	mV
Capacitive Load Range for Stability		[j]	0		50	pF
Slew Rate				11		V/µs
PWRGD						
V_{OUT} Rising Threshold	$V_{PG\_HI\%}$		78	84	90	% V_{OUT_DC}
V_{OUT} Falling Threshold	$V_{PG\_LO\%}$		75	81	87	% V_{OUT_DC}
PWRGD Output Low	V_{PG_SAT}	Sink = 4mA			0.4	V

[c] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI358x evaluation board with 3 x 3in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[d] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[e] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[f] Refer to Output Ripple plots.
[g] Refer to Load Current vs. Ambient Temperature curves.
[h] Refer to Switching Frequency vs. Load current curves.
[i] Contact factory applications for array derating and layout best practices to minimize sharing errors.
[j] Informational only.

PI358x-00 Common Electrical Characteristics (Cont.)

Specifications apply for –20°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted. [c]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VDR						
Voltage Set Point	V_{VDR}	V_{IN_DC} > 10V	4.9	5.05	5.2	V
External Loading	I_{VDR}	See Application Description for details	0		2	mA
External Inductor Between VDR and VBS	L_{VBS}	External required components for VDR, recommended to be an Inductor. Refer to Table 1 for the recommended component.		10		µH
External Capacitor Between VDR and PGND	C_{VDR}	External required components for VDR, recommended to be a capacitor. Refer to Table 1 for the recommended component.		2.2		µF
Enable						
High Threshold	V_{EN_HI}		0.9	1.0	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Pull-Up Voltage Level for Source Current	V_{EN_PU}			2		V
Pull-Up Current	$I_{EN\_PU\_POS}$			50		µA
Reliability						
MTBF		MIL-HDBK-217, 25°C, Ground Benign: GB		22.7		MHrs
		Telcordia SR-332, 25°C, Ground Benign: GB		191		MHrs

[c] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI358x evaluation board with 3 x 3in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
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[f] Refer to Output Ripple plots.
[g] Refer to Load Current vs. Ambient Temperature curves.
[h] Refer to Switching Frequency vs. Load current curves.
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[j] Informational only.

PI3583-00 ($3.3V_{OUT}$) Electrical Characteristics

Specifications apply for –20°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted. [c]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		30	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_{CASE} = 25°C, full load		0.77		A
Input Current at Output Short (Fault Condition Duty Cycle)	I_{IN_Short}	Short at terminals		3		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.65		mA
Input Quiescent Current	I_{Q_VIN}	Enabled, no load, T_{CASE} = 25°C		1.8		mA
Input Voltage Slew Rate	V_{IN_SR}	[j]			1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[d]	0.975	0.990	1.005	V
Output Voltage Trim Range	V_{OUT_DC}	[d] [e]	2.2	3.3	4.0	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	@ 25°C, 30V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	@ 25°C, 10% to 100% load		0.10		%
Output Voltage Ripple	V_{OUT_AC}	Full load, C_{OUT} = 6 x 100µF, 20MHz BW [f]		53		mV_{P-P}
Output Current	I_{OUT_DC}	[g]	0		10	A
Current Limit	I_{OUT_CL}	Typical current limit based on nominal 420nH inductor.		11.5		A
Maximum Array Size	$N_{PARALLEL}$	[d]			3	Modules
Output Current, Array of 2	$I_{OUT\_DC\_ARRAY2}$	Total array capability, [d] see applications section for details	0		[i]	A
Output Current, Array of 3	$I_{OUT\_DC\_ARRAY3}$	Total array capability, [d] see applications section for details	0		[i]	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}			27.0	29.1	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		1.66	2.08	2.50	V
Input UVLO Response Time				1.25		µs
Input OVLO Stop Threshold	V_{OVLO_STOP}	[d]		64.3		V
Input OVLO Start Hysteresis	V_{OVLO_HYS}	Hysteresis active when OVLO present for at least t_{FR_DLY} [d]		1.17		V
Input OVLO Start Threshold	V_{OVLO_START}	[d]	60.5			V
Input OVLO Response Time	t_f			1.25		µs
Output Overvoltage Protection, Relative	V_{OVP_REL}	Above set V_{OUT}		20		%
Output Overvoltage Protection, Absolute	V_{OVP_ABS}		4.8	5.3		V

[c] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI358x evaluation board with 3 x 3in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[d] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[e] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[f] Refer to Output Ripple plots.
[g] Refer to Load Current vs. Ambient Temperature curves.
[h] Refer to Switching Frequency vs. Load current curves.
[i] Contact factory applications for array derating and layout best practices to minimize sharing errors.
[j] Informational only.

PI3583-00 ($3.3V_{OUT}$) Electrical Characteristics (Cont.)

Specifications apply for –20°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted. [c]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_s	[h] While in DCM operating mode only, SYNCI grounded	470	500	530	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Synchronization Input (SYNCI)						
Synchronization Frequency Range	f_{SYNCI}	–50% and +10% relative to set switching frequency (f_S), while in DCM operating mode only. [e] and [h]	250		550	kHz
SYNCI Threshold	V_{SYNCI}			2.5		V
Synchronization Output (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}			40		mV
TRK to EAIN Offset	V_{EAIN_OV}		40	80	120	mV
Charge Current (Soft Start)	I_{TRK}		30	50	70	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		8.7		mA
TRK Capacitance, External	C_{TRK_EXT}		47			nF
Soft Start Time	t_{SS}	C_{TRK} = 47nF		0.94		ms
Error Amplifier Transconductance	GM_{EAO}	[d]		7.6		mS
PSM Skip Threshold	PSM_{SKIP}	[d]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[d]	1			MΩ
Internal Compensation Resistor	R_{ZI}	[d]		6		kΩ

[c] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI358x evaluation board with 3 x 3in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[d] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[e] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
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PI3583-00 ($3.3V_{OUT}$) Electrical Characteristics (Cont.)

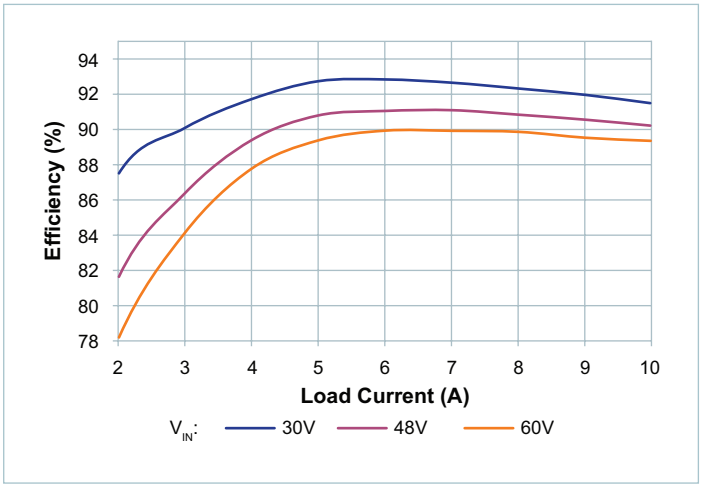


Figure 1 — *System efficiency, nominal trim, board temperature = 25°C*

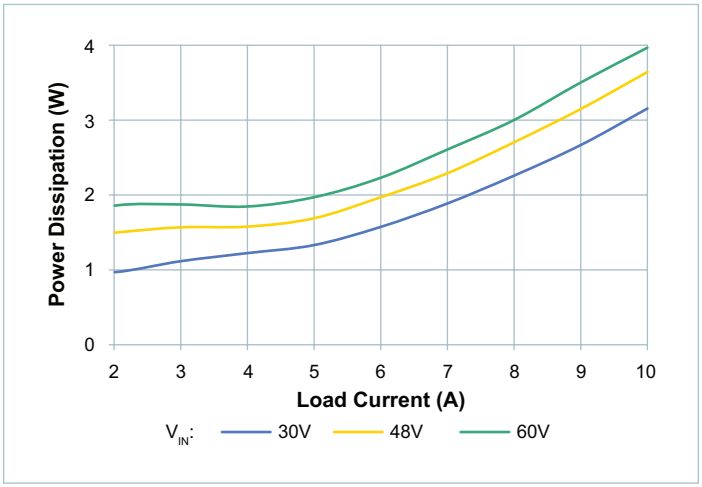


Figure 4 — *System power dissipation, nominal trim, board temperature = 25°C*

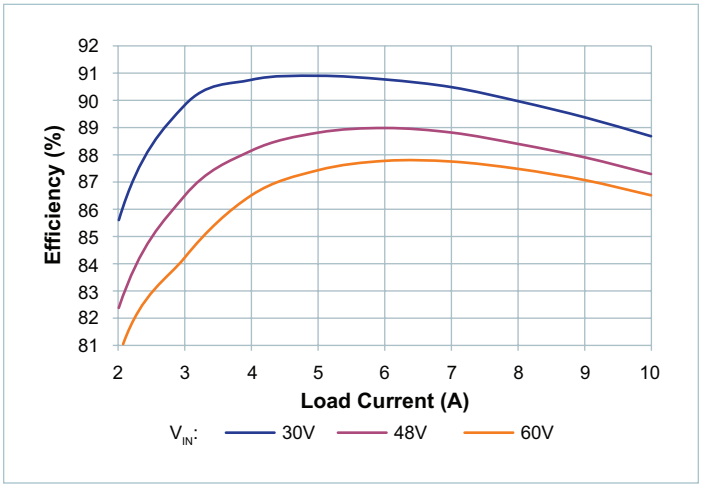


Figure 2 — *System efficiency, low trim, board temperature = 25°C*

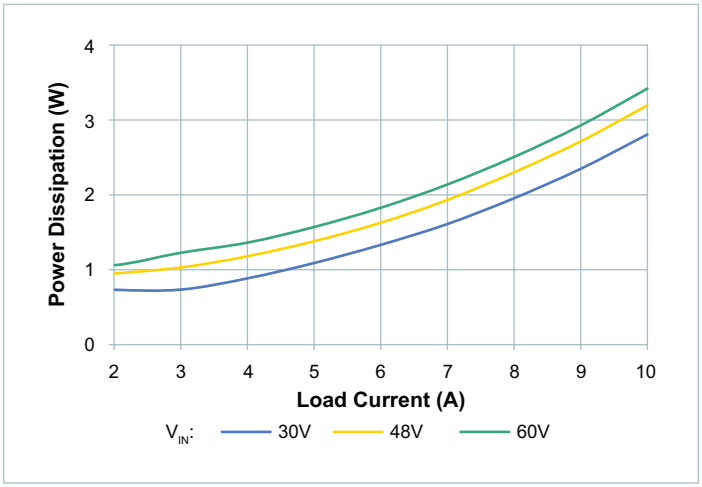


Figure 5 — *System power dissipation, low trim, board temperature = 25°C*

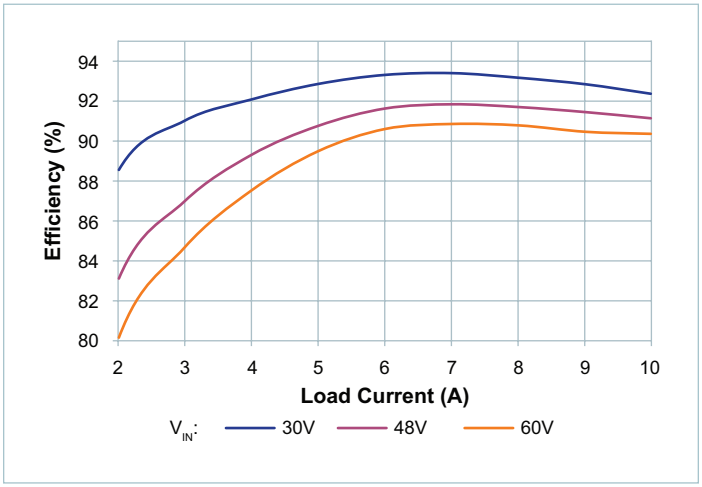


Figure 3 — *System efficiency, high trim, board temperature = 25°C*

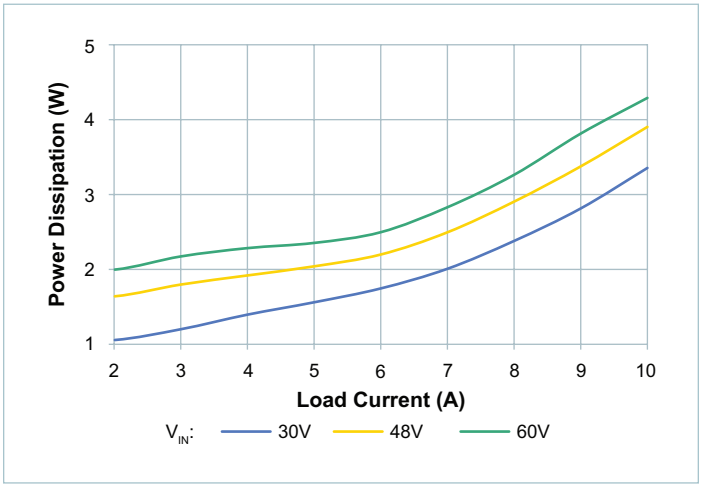


Figure 6 — *System power dissipation, high trim, board temperature = 25°C*

PI3583-00 ($3.3V_{OUT}$) Electrical Characteristics (Cont.)

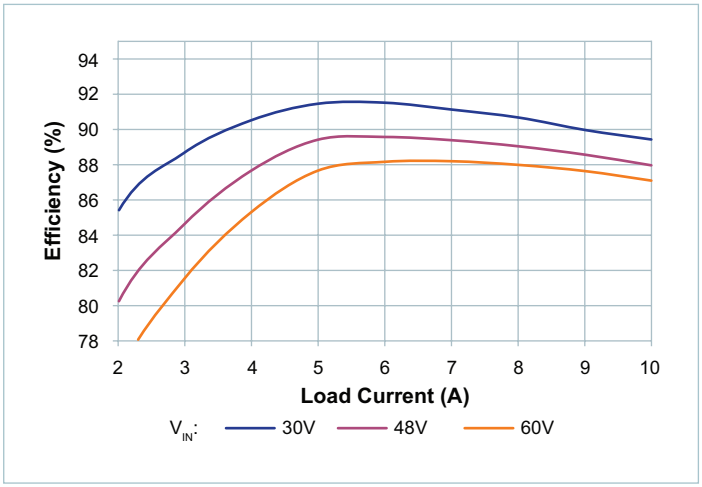


Figure 7 — *System efficiency, nominal trim, board temperature = 90°C*

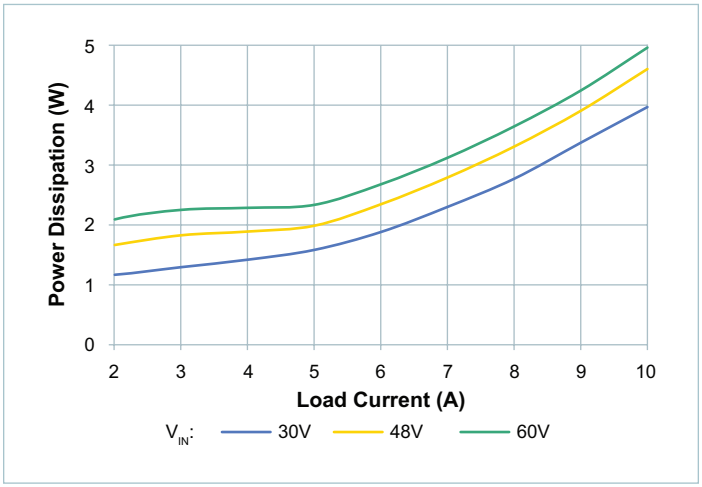


Figure 10 — *System power dissipation, nominal trim, board temperature = 90°C*

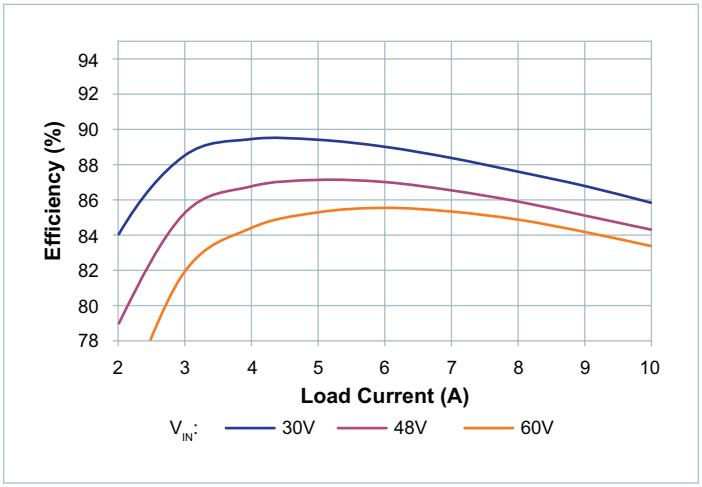


Figure 8 — *System efficiency, low Trim, board temperature = 90°C*

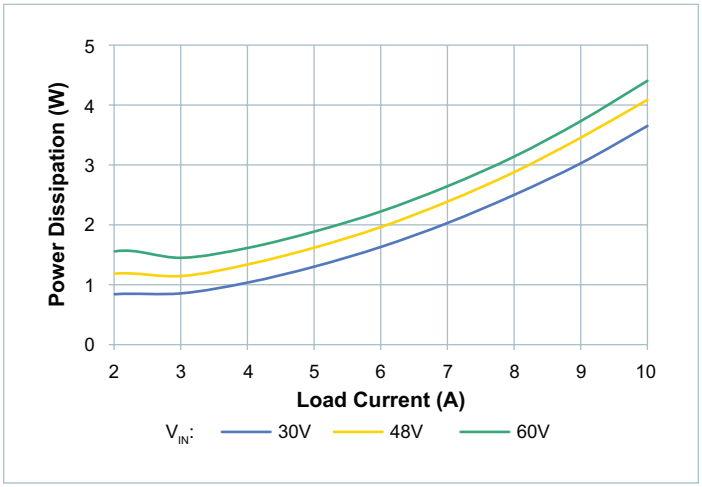


Figure 11 — *System power dissipation, low trim, board temperature = 90°C*

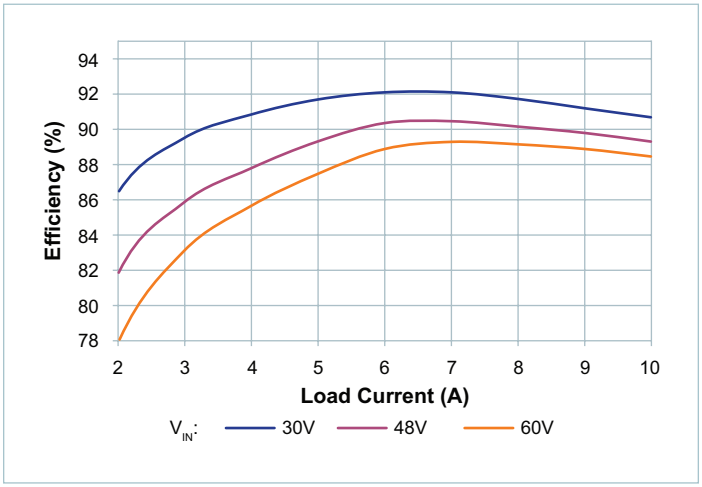


Figure 9 — *System efficiency, high trim, board temperature = 90°C*

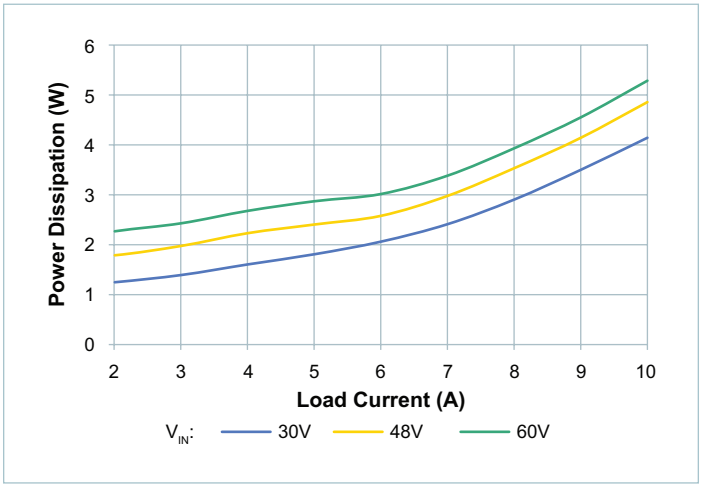


Figure 12 — *System power dissipation, high trim, board temperature = 90°C*

PI3583-00 (3.3V_{OUT}) Electrical Characteristics (Cont.)

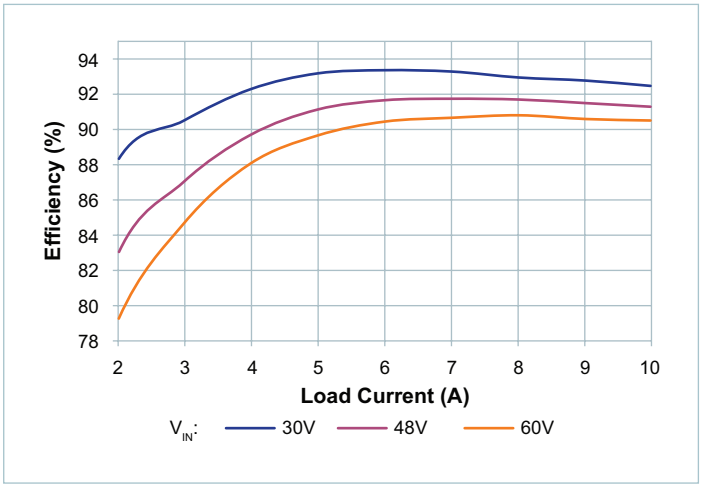


Figure 13 — *System efficiency, nominal trim, board temperature = –20°C*

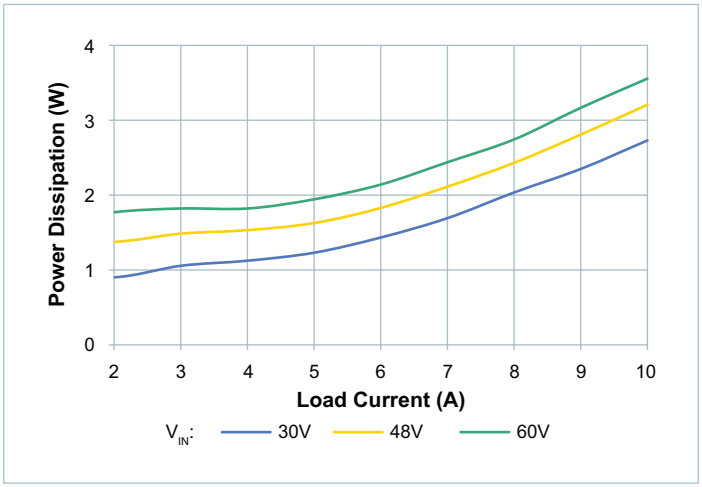


Figure 16 — *System power dissipation, nominal trim, board temperature = –20°C*

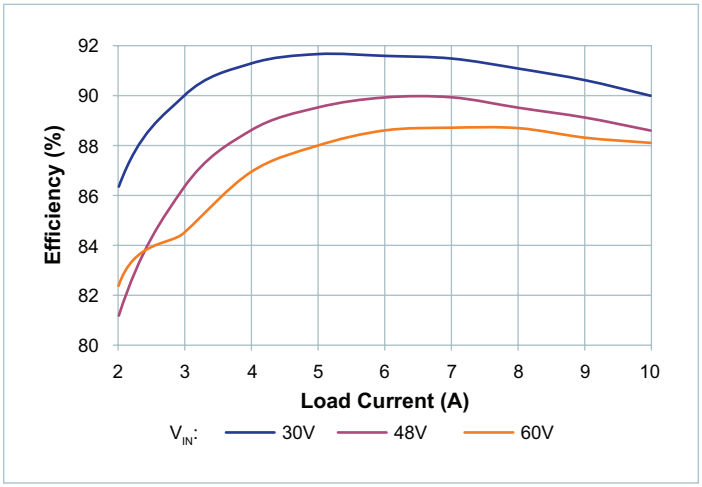


Figure 14 — *System efficiency, low trim, board temperature = –20°C*

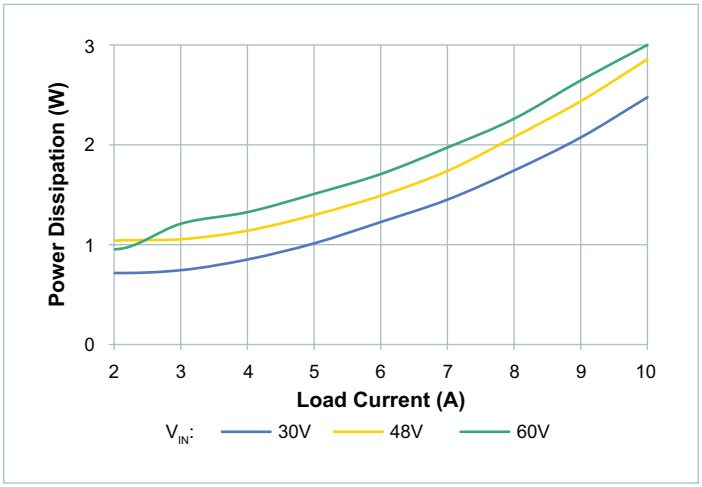


Figure 17 — *System power dissipation, low trim, board temperature = –20°C*

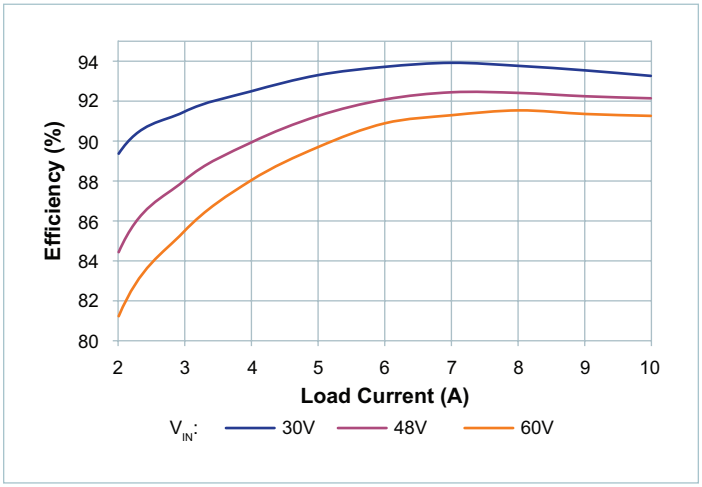


Figure 15 — *System efficiency, high trim, board temperature = –20°C*

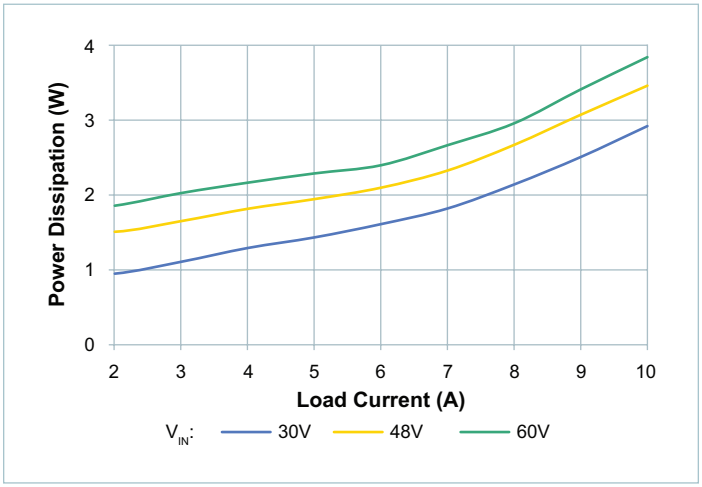


Figure 18 — *System power dissipation, high trim, board temperature = –20°C*

PI3583-00 (3.3V_{OUT}) Electrical Characteristics (Cont.)

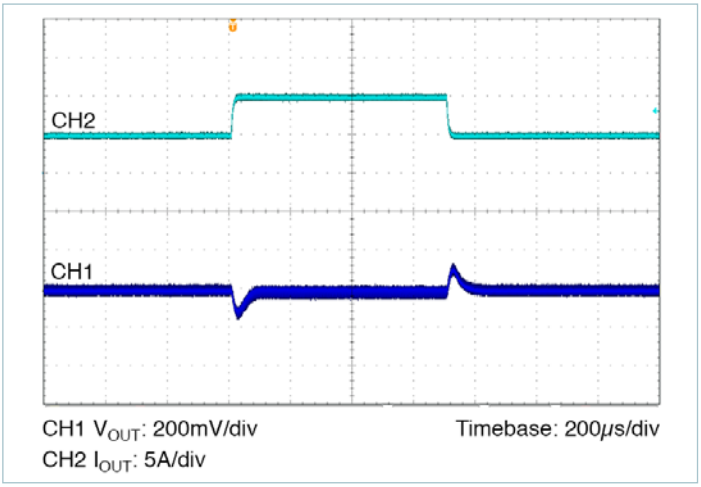


Figure 19 — *Transient response: 50% to 100% load, at 1A/µs; nominal line, nominal trim, C_{OUT} = 6 x 100µF ceramic*

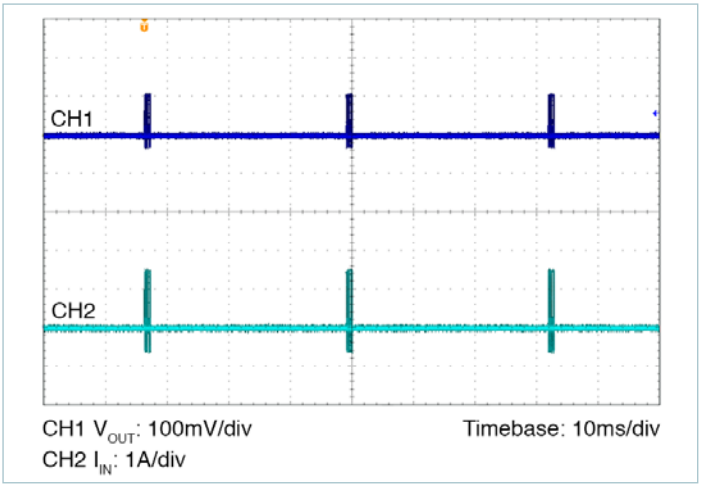


Figure 22 — *Output short circuit, nominal line*

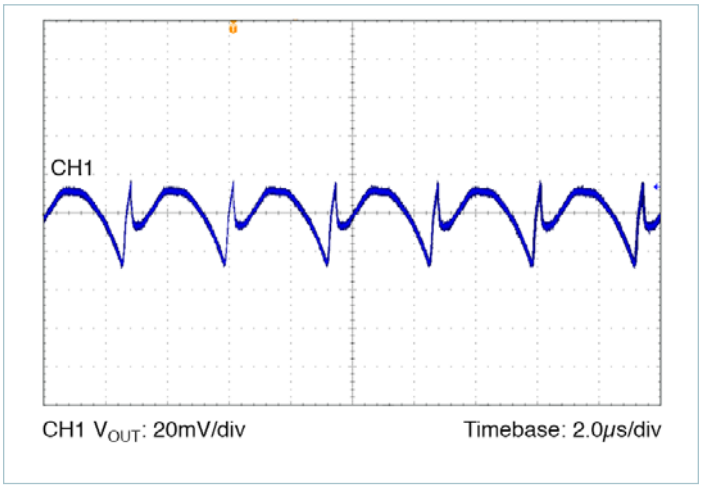


Figure 20 — *Output voltage ripple: nominal line, nominal trim, 100% load, C_{OUT} = 6 x 100µF ceramic, 20MHz BW*

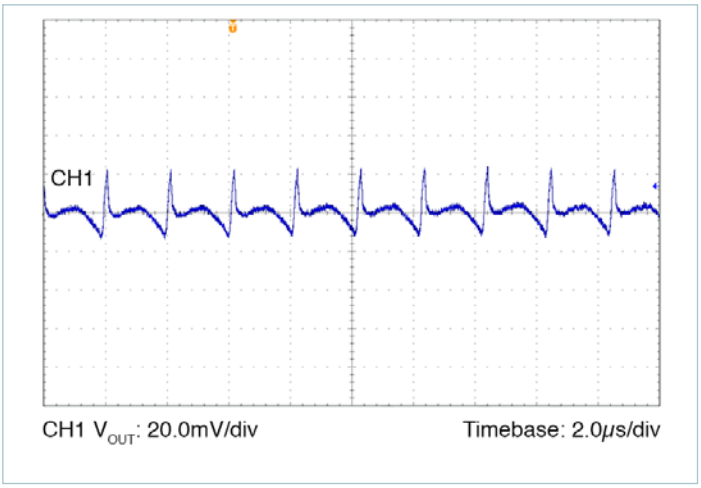


Figure 23 — *Output voltage ripple: nominal line, nominal trim, 50% load, C_{OUT} = 6 x 100µF ceramic, 20MHz BW*

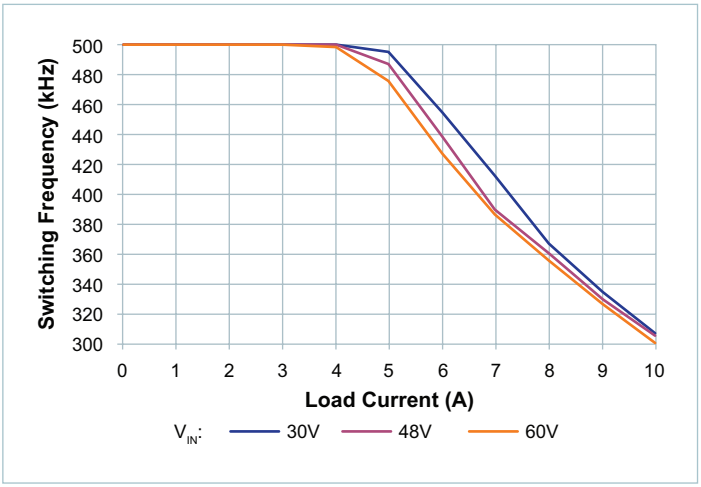


Figure 21 — *Switching frequency vs. load, nominal trim*

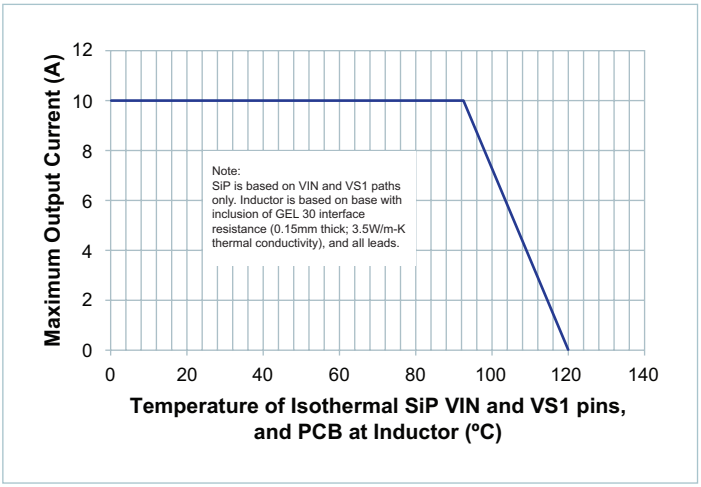


Figure 24 — *System thermal specified operating area: max I_{OUT} at nominal trim vs. temperature at locations noted*

PI3583-00 (3.3V_{OUT}) Electrical Characteristics (Cont.)

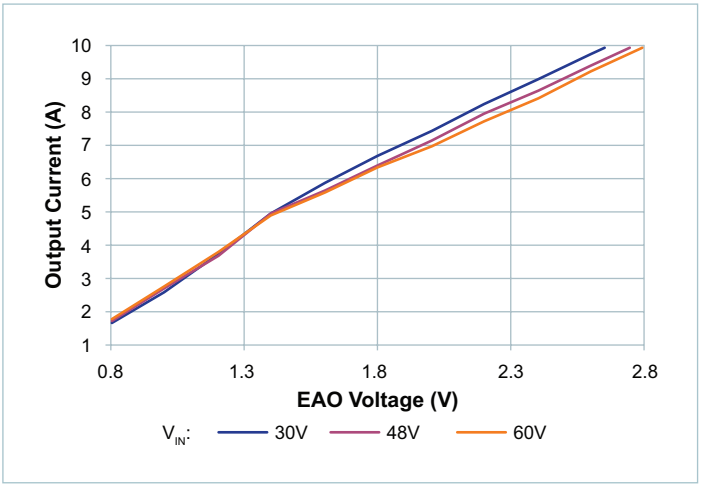


Figure 25 — *Output current vs. V_{EAO}, nominal trim*

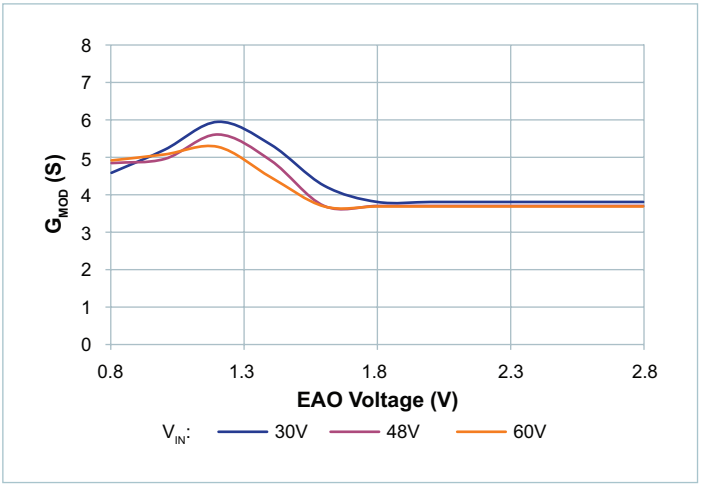


Figure 26 — *Small-signal modulator gain vs. V_{EAO}, nominal trim*

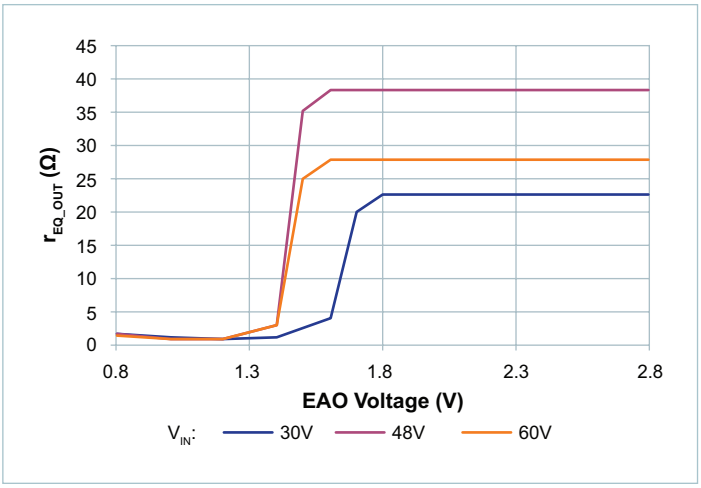


Figure 27 — *r_{EQ_OUT} vs V_{EAO}, nominal trim*

PI3585-00 ($5.0V_{OUT}$) Electrical Characteristics

Specifications apply for –20°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted. [c]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		30	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_{CASE} = 25°C, full load		1.12		A
Input Current at Output Short (Fault Condition Duty Cycle)	I_{IN_Short}	Short at terminals		1.8		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.65		mA
Input Quiescent Current	I_{Q_VIN}	Enabled, no load, T_{CASE} = 25°C		2		mA
Input Voltage Slew Rate	V_{IN_SR}	[j]			1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[d]	0.975	0.990	1.005	V
Output Voltage Trim Range	V_{OUT_DC}	[d] [e]	3.8	5.0	6.5	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	@ 25°C, 30V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	@ 25°C, 10% to 100% load		0.10		%
Output Voltage Ripple	V_{OUT_AC}	Full load, C_{OUT} = 6 x 47µF, 20MHz BW [f]		60		mV_{P-P}
Output Current	I_{OUT_DC}	[g]	0		10	A
Current Limit	I_{OUT_CL}	Typical current limit based on nominal 420nH inductor.		11.5		A
Maximum Array Size	$N_{PARALLEL}$	[d]			3	Modules
Output Current, Array of 2	$I_{OUT\_DC\_ARRAY2}$	Total array capability, [d] see applications section for details	0		[i]	A
Output Current, Array of 3	$I_{OUT\_DC\_ARRAY3}$	Total array capability, [d] see applications section for details	0		[i]	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}			27.0	29.1	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		1.66	2.08	2.50	V
Input UVLO Response Time				1.25		µs
Input OVLO Stop Threshold	V_{OVLO_STOP}	[d]		64.3		V
Input OVLO Start Hysteresis	V_{OVLO_HYS}	Hysteresis active when OVLO present for at least t_{FR_DLY} [d]		1.17		V
Input OVLO Start Threshold	V_{OVLO_START}	[d]	60.5			V
Input OVLO Response Time	t_f			1.25		µs
Output Overvoltage Protection, Relative	V_{OVP_REL}	Above set V_{OUT}		20		%
Output Overvoltage Protection, Absolute	V_{OVP_ABS}		6.7	7.5		V

[c] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI358x evaluation board with 3 x 3in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[d] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[e] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[f] Refer to Output Ripple plots.
[g] Refer to Load Current vs. Ambient Temperature curves.
[h] Refer to Switching Frequency vs. Load current curves.
[i] Contact factory applications for array derating and layout best practices to minimize sharing errors.
[j] Informational only.

PI3585-00 ($5.0V_{OUT}$) Electrical Characteristics (Cont.)

Specifications apply for –20°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted. [c]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_s	[h] While in DCM operating mode only, SYNCI grounded	564	600	636	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Synchronization Input (SYNCI)						
Synchronization Frequency Range	f_{SYNCI}	–50% and +10% relative to set switching frequency (f_S), while in DCM operating mode only. [e] and [h]	300		660	kHz
SYNCI Threshold	V_{SYNCI}			2.5		V
Synchronization Output (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}			40		mV
TRK to EAIN Offset	V_{EAIN_OV}		40	80	120	mV
Charge Current (Soft Start)	I_{TRK}		30	50	70	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		8.7		mA
TRK Capacitance, External	C_{TRK_EXT}		47			nF
Soft Start Time	t_{SS}	C_{TRK} = 47nF		0.94		ms
Error Amplifier Transconductance	GM_{EAO}	[d]		7.6		mS
PSM Skip Threshold	PSM_{SKIP}	[d]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[d]	1			MΩ
Internal Compensation Resistor	R_{ZI}	[d]		6		kΩ

[c] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI358x evaluation board with 3 x 3in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[d] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[e] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[f] Refer to Output Ripple plots.
[g] Refer to Load Current vs. Ambient Temperature curves.
[h] Refer to Switching Frequency vs. Load current curves.
[i] Contact factory applications for array derating and layout best practices to minimize sharing errors.
[j] Informational only.

PI3585-00 (5.0V$_{OUT}$) Electrical Characteristics (Cont.)

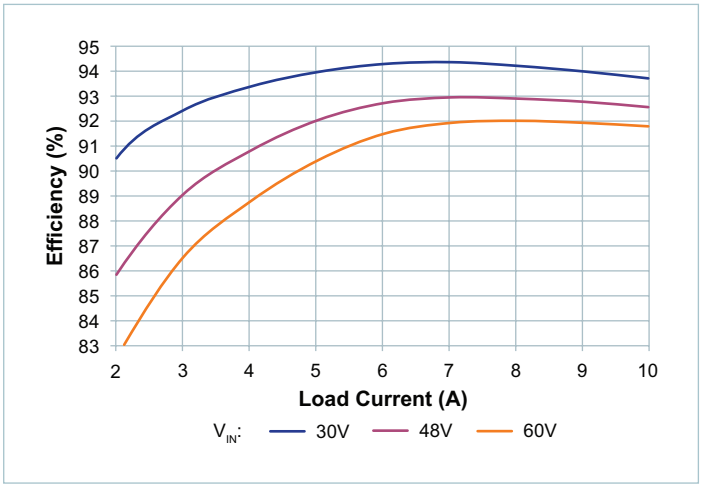


Figure 28 — *System efficiency, nominal trim, board temperature = 25°C*

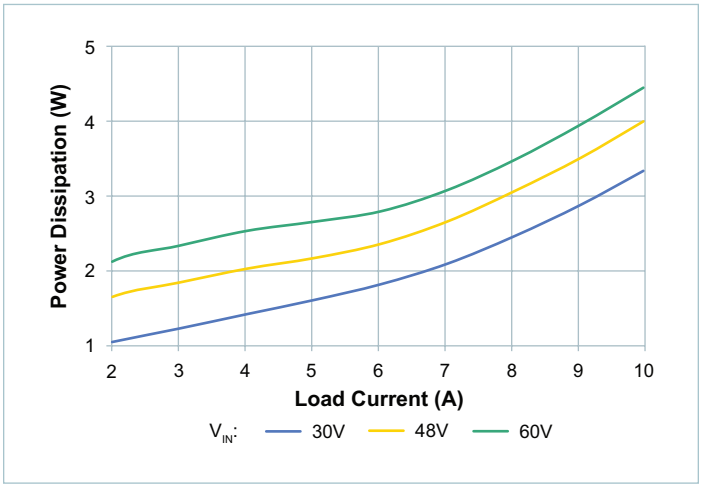


Figure 31 — *System power dissipation, nominal trim, board temperature = 25°C*

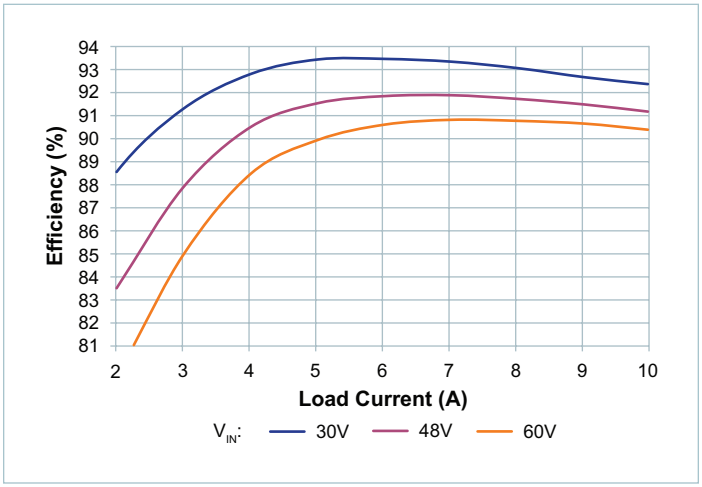


Figure 29 — *System efficiency, low trim, board temperature = 25°C*

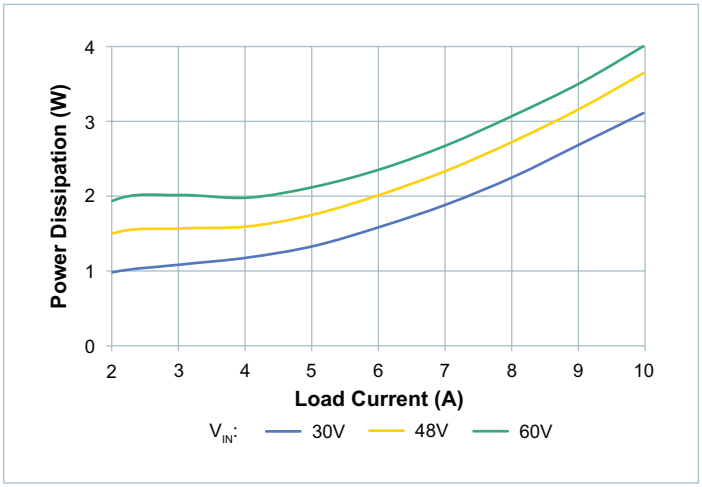


Figure 32 — *System power dissipation, low trim, board temperature = 25°C*

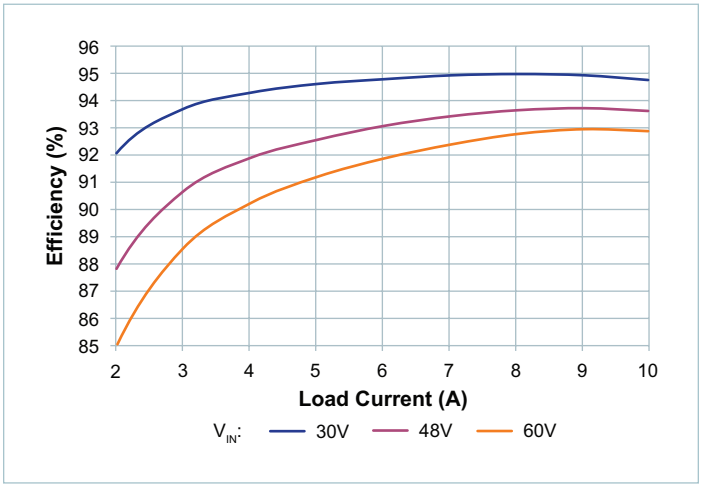


Figure 30 — *System efficiency, high trim, board temperature = 25°C*

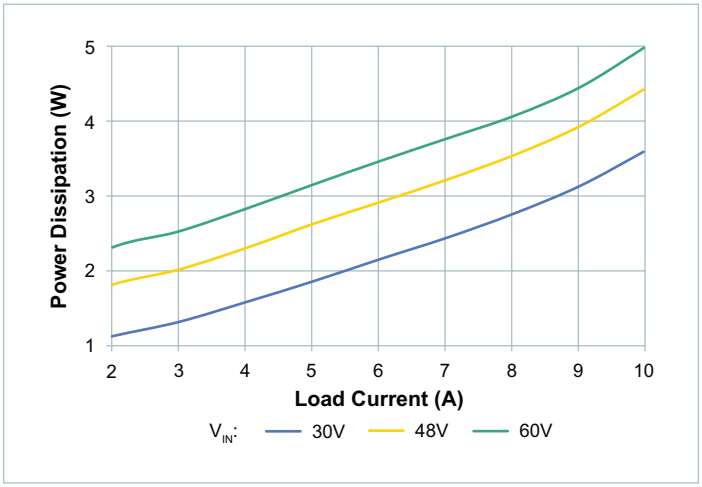


Figure 33 — *System power dissipation, high trim, board temperature = 25°C*

PI3585-00 (5.0V$_{OUT}$) Electrical Characteristics (Cont.)

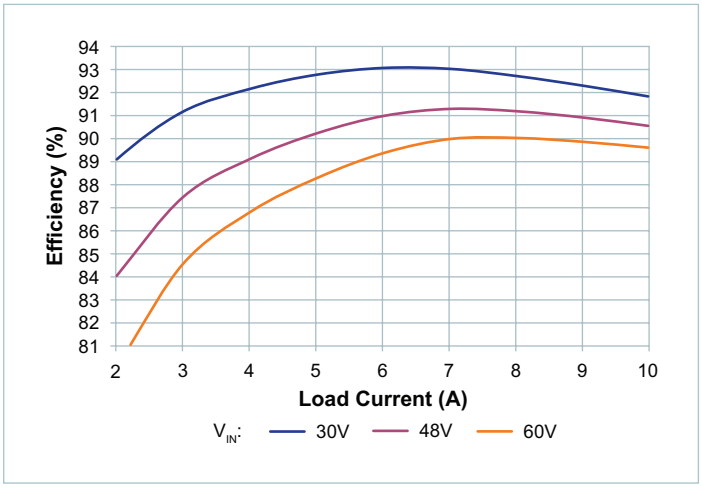


Figure 34 — *System efficiency, nominal trim, board temperature = 90°C*

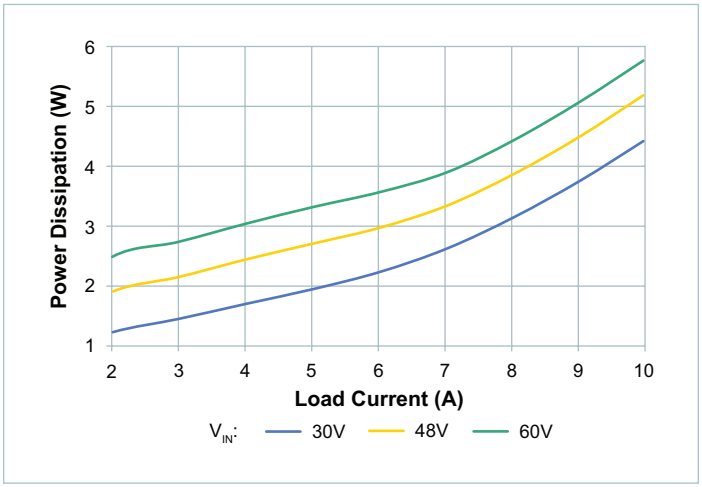


Figure 37 — *System power dissipation, nominal trim, board temperature = 90°C*

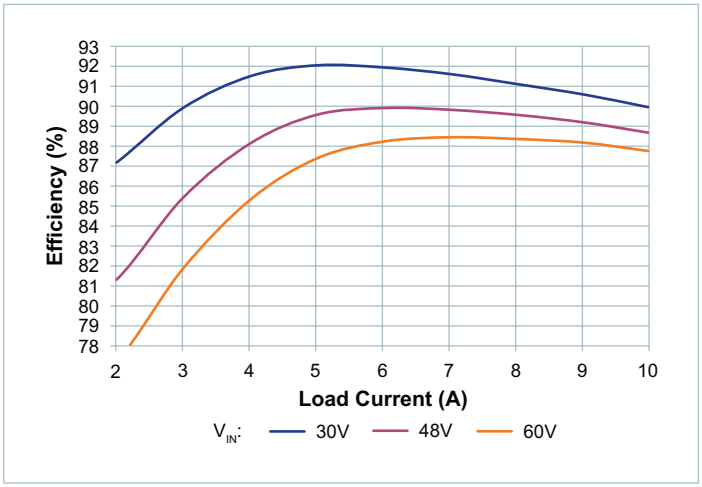


Figure 35 — *System efficiency, low Trim, board temperature = 90°C*

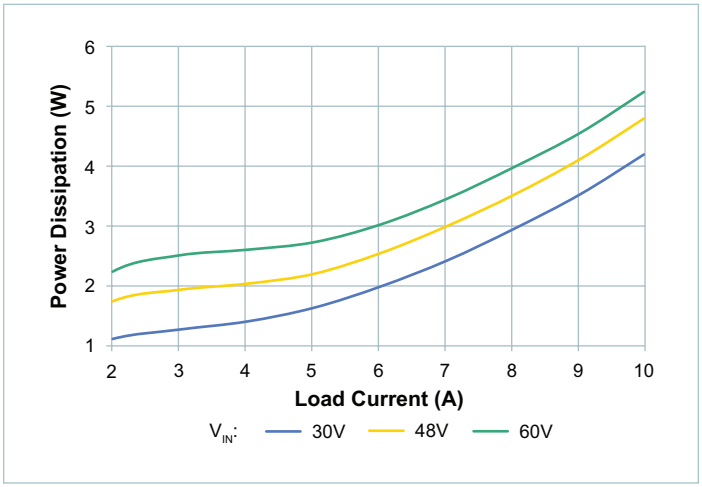


Figure 38 — *System power dissipation, low trim, board temperature = 90°C*

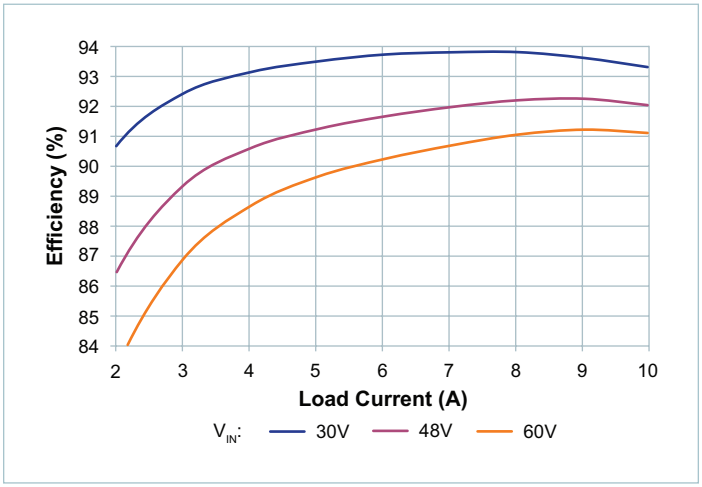


Figure 36 — *System efficiency, high trim, board temperature = 90°C*

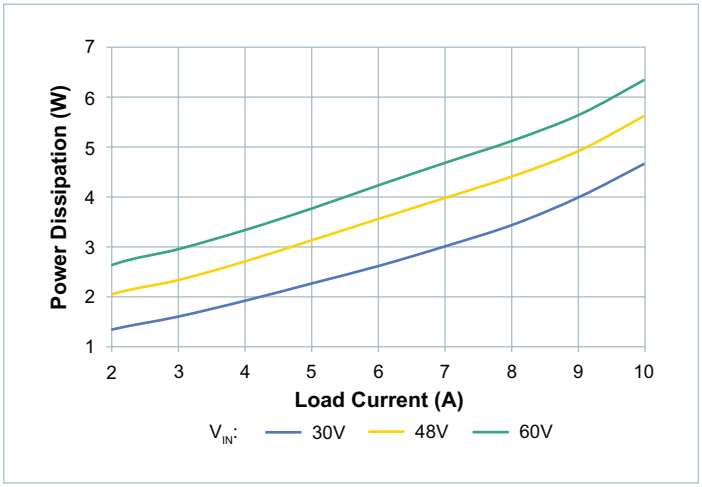


Figure 39 — *System power dissipation, high trim, board temperature = 90°C*

PI3585-00 ($5.0V_{OUT}$) Electrical Characteristics (Cont.)

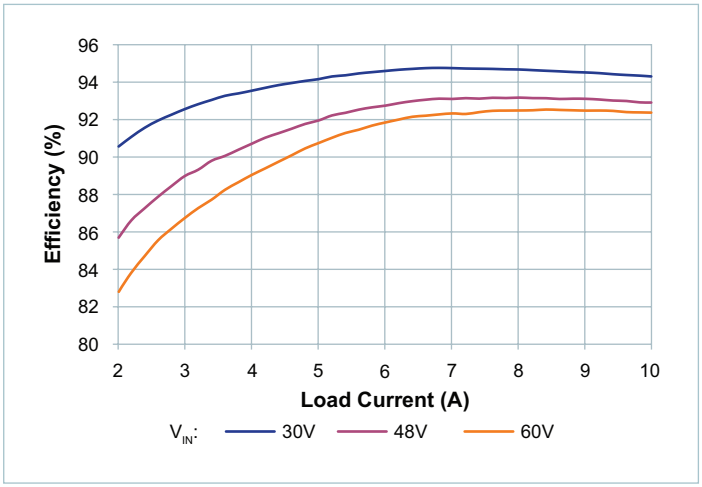


Figure 40 — *System efficiency, nominal trim, board temperature = –20°C*

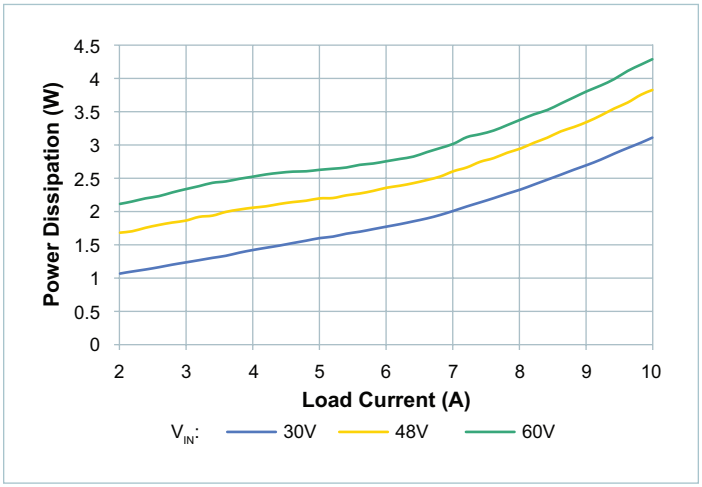


Figure 43 — *System power dissipation, nominal trim, board temperature = –20°C*

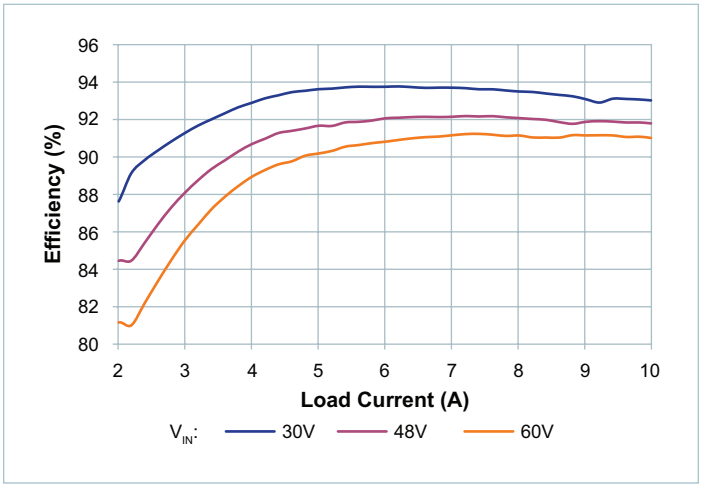


Figure 41 — *System efficiency, low trim, board temperature = –20°C*

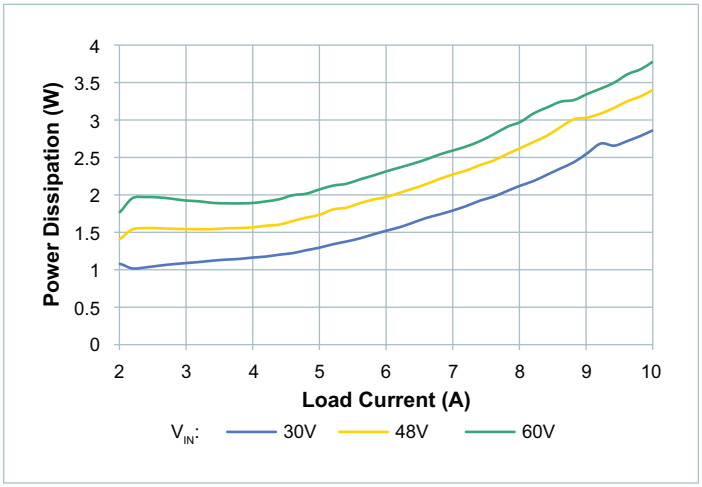


Figure 44 — *System power dissipation, low trim, board temperature = –20°C*

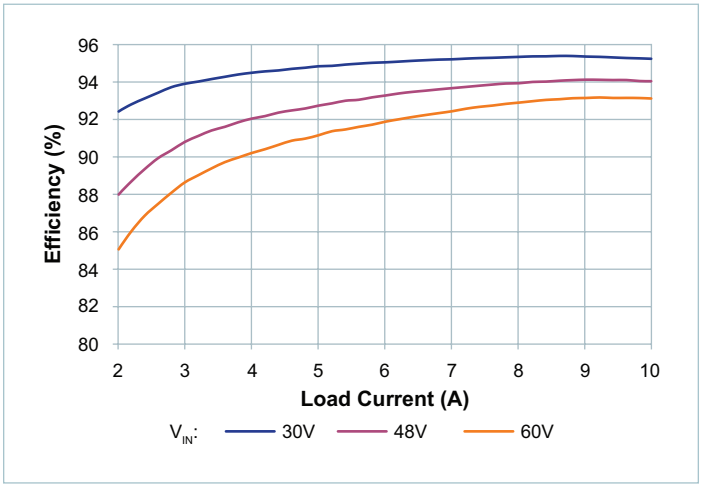


Figure 42 — *System efficiency, high trim, board temperature = –20°C*

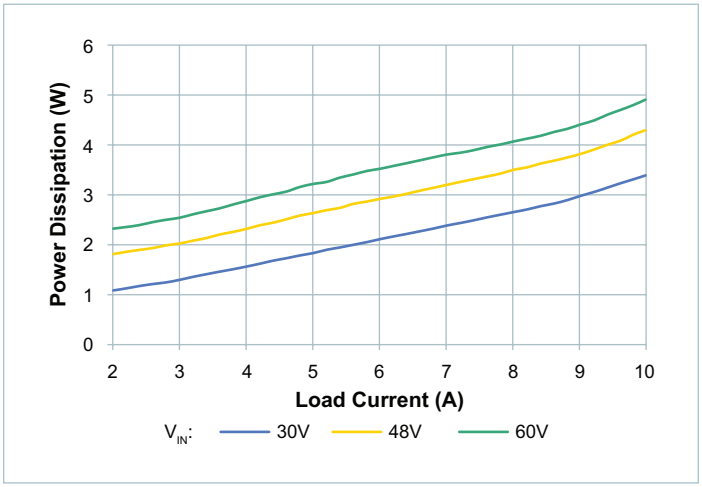


Figure 45 — *System power dissipation, high trim, board temperature = –20°C*

PI3585-00 (5.0V$_{OUT}$) Electrical Characteristics (Cont.)

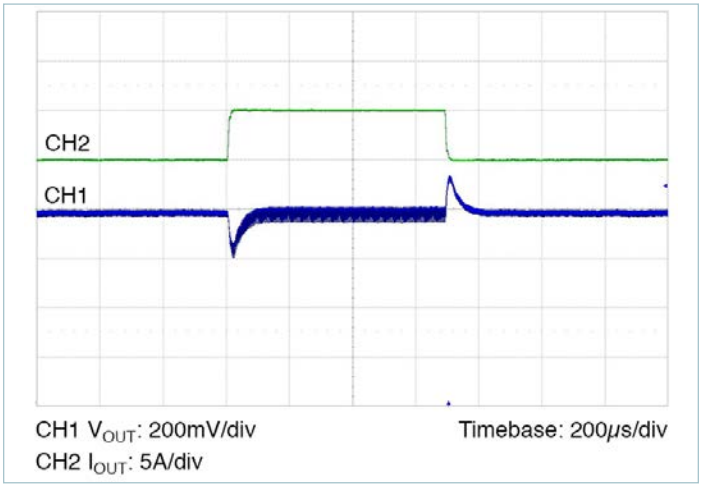


Figure 46 — *Transient response: 50% to 100% load, at 1A/µs; nominal line, nominal trim, C_{OUT} = 6 x 47µF ceramic*

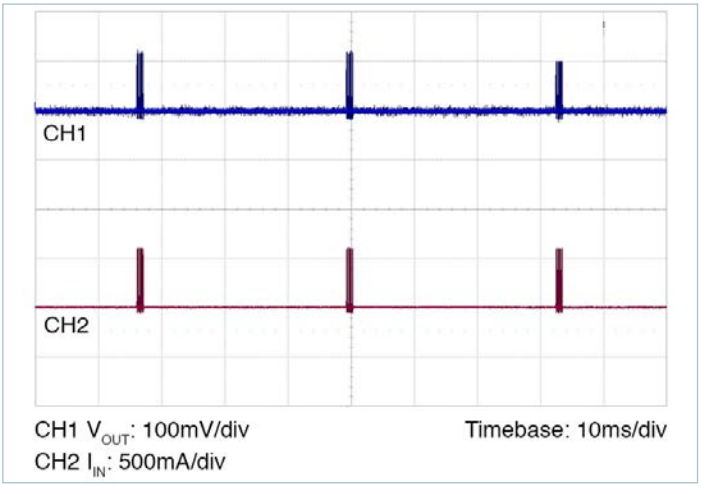


Figure 49 — *Output short circuit, nominal line*

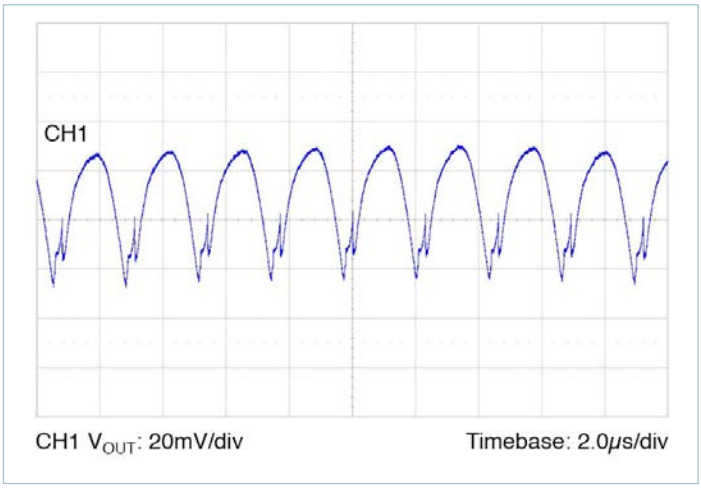


Figure 47 — *Output voltage ripple: nominal line, nominal trim, 100% load, C_{OUT} = 6 x 47µF ceramic, 20MHz BW*

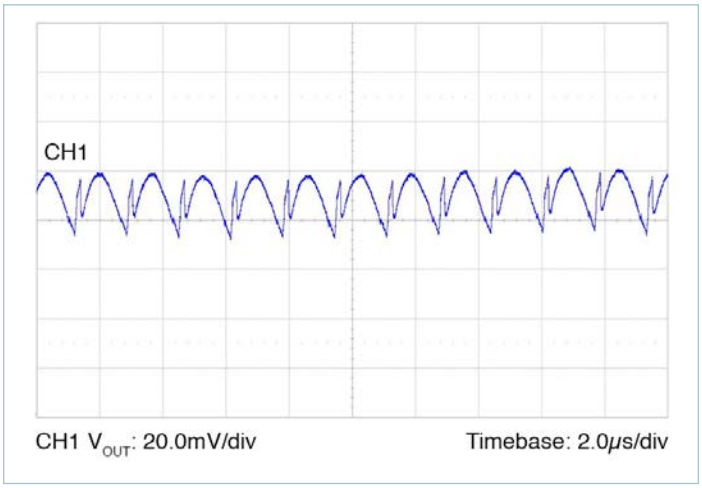


Figure 50 — *Output voltage ripple: nominal line, nominal trim, 50% load, C_{OUT} = 6 x 47µF ceramic, 20MHz BW*

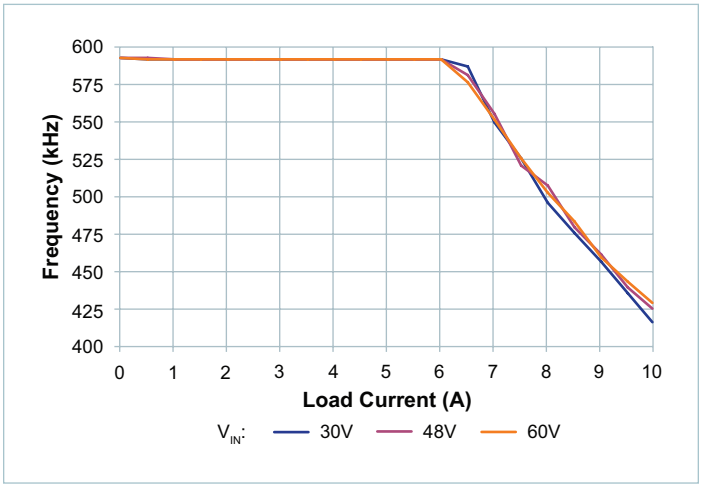


Figure 48 — *Switching frequency vs. load, nominal trim*

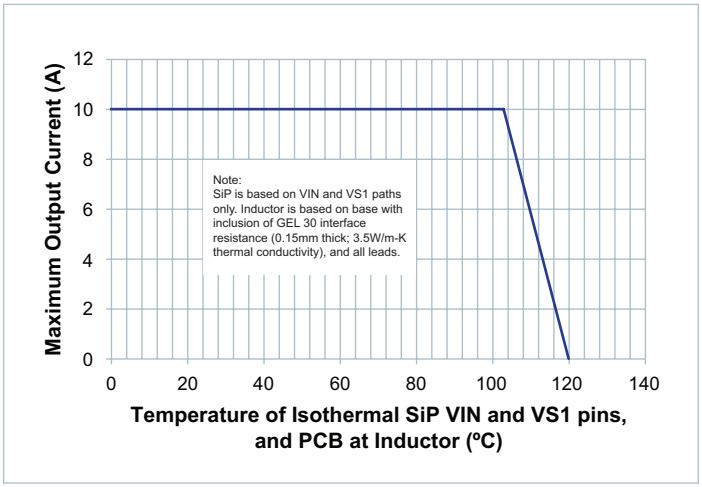


Figure 51 — *System thermal specified operating area: max I_{OUT} at nominal trim vs. temperature at locations noted*

PI3585-00 (5.0V_{OUT}) Electrical Characteristics (Cont.)

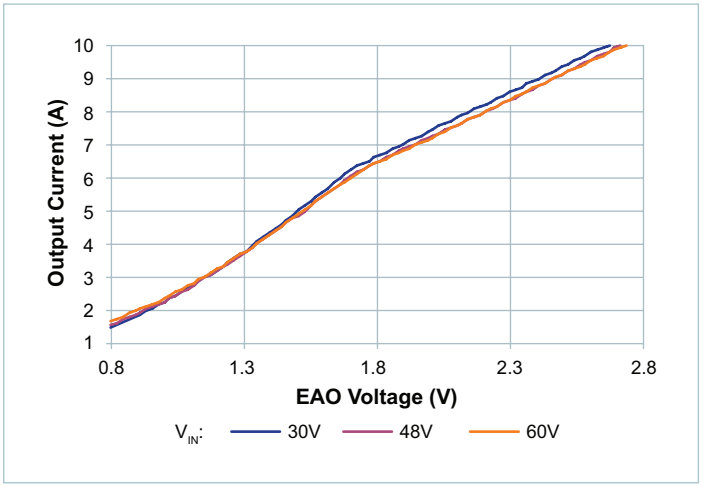


Figure 52 — *Output current vs. V_{EAO}, nominal trim*

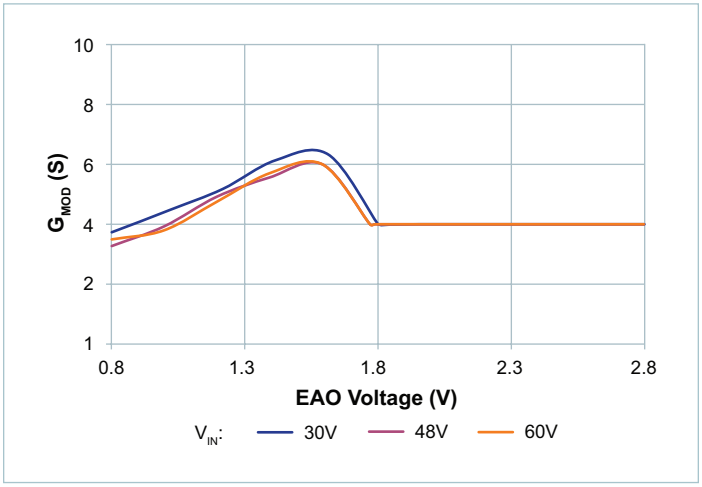


Figure 53 — *Small-signal modulator gain vs. V_{EAO}, nominal trim*

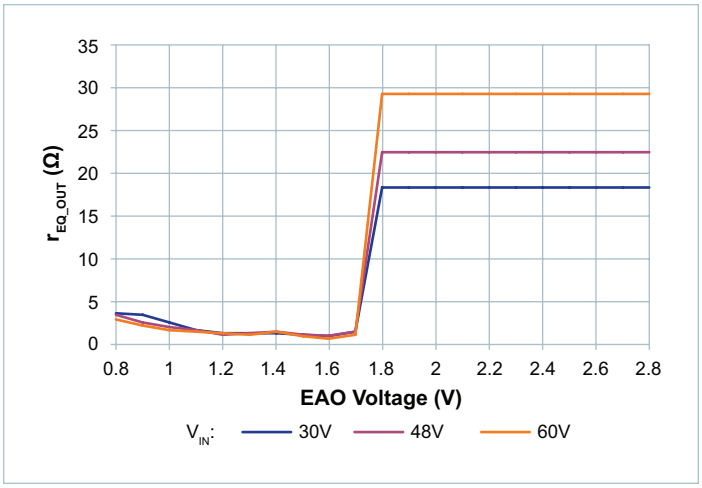


Figure 54 — *r_{EQ_OUT} vs V_{EAO}, nominal trim*

PI3586-00 (12.0V_{OUT}) Electrical Characteristics

Specifications apply for –20°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted. [c]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		30	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_{CASE} = 25°C, full load		2.35		A
Input Current at Output Short (Fault Condition Duty Cycle)	I_{IN_Short}	Short at terminals		3.5		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.65		mA
Input Quiescent Current	I_{Q_VIN}	Enabled, no load, T_{CASE} = 25°C		3		mA
Input Voltage Slew Rate	V_{IN_SR}	[j]			1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[d]	0.975	0.990	1.005	V
Output Voltage Trim Range	V_{OUT_DC}	[d] [e]	6.5	12.0	14.0	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	@ 25°C, 30V < V_{IN} < 60V		0.1		%
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	@ 25°C, 10% to 100% load		0.1		%
Output Voltage Ripple	V_{OUT_AC}	Full load, C_{OUT} = 6 x 10µF, 20MHz BW [f]		115		mV_{P-P}
Output Current	I_{OUT_DC}	[g]	0		9	A
Current Limit	I_{OUT_CL}	Typical current limit based on nominal 900nH inductor		10.5		A
Maximum Array Size	$N_{PARALLEL}$	[d]			3	Modules
Output Current, Array of 2	$I_{OUT\_DC\_ARRAY2}$	Total array capability, [d] see applications section for details	0		[i]	A
Output Current, Array of 3	$I_{OUT\_DC\_ARRAY3}$	Total array capability, [d] see applications section for details	0		[i]	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}			27.0	29.1	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		1.66	2.08	2.50	V
Input UVLO Response Time				1.25		µs
Input OVLO Stop Threshold	V_{OVLO_STOP}	[d]		64.3		V
Input OVLO Start Hysteresis	V_{OVLO_HYS}	Hysteresis active when OVLO present for at least t_{FR_DLY} [d]		1.17		V
Input OVLO Start Threshold	V_{OVLO_START}	[d]	60.5			V
Input OVLO Response Time	t_f			1.25		µs
Output Overvoltage Protection, Relative	V_{OVP_REL}	Above set V_{OUT}		20		%
Output Overvoltage Protection, Absolute	V_{OVP_ABS}		14.7	15.8		V

[c] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI358x evaluation board with 3 x 3in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[d] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[e] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[f] Refer to Output Ripple plots.
[g] Refer to Load Current vs. Ambient Temperature curves.
[h] Refer to Switching Frequency vs. Load current curves.
[i] Contact factory applications for array derating and layout best practices to minimize sharing errors.
[j] Informational only.

PI3586-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

Specifications apply for –20°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted. [c]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_s	[h] While in DCM operating mode only, SYNCI grounded	658	700	742	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Synchronization Input (SYNCI)						
Synchronization Frequency Range	f_{SYNCI}	–50% and +10% relative to set switching frequency (f_S), while in DCM operating mode only. [e] and [h]	350		770	kHz
SYNCI Threshold	V_{SYNCI}			2.5		V
Synchronization Output (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}			40		mV
TRK to EAIN Offset	V_{EAIN_OV}		40	80	120	mV
Charge Current (Soft Start)	I_{TRK}		30	50	70	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		8.7		mA
TRK Capacitance, External	C_{TRK_EXT}		47			nF
Soft Start Time	t_{SS}	C_{TRK} = 47nF		0.94		ms
Error Amplifier Transconductance	GM_{EAO}	[d]		7.6		mS
PSM Skip Threshold	PSM_{SKIP}	[d]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[d]	1			MΩ
Internal Compensation Resistor	R_{ZI}	[d]		6		kΩ

[c] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI358x evaluation board with 3 x 3in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[d] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[e] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[f] Refer to Output Ripple plots.
[g] Refer to Load Current vs. Ambient Temperature curves.
[h] Refer to Switching Frequency vs. Load current curves.
[i] Contact factory applications for array derating and layout best practices to minimize sharing errors.
[j] Informational only.

PI3586-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

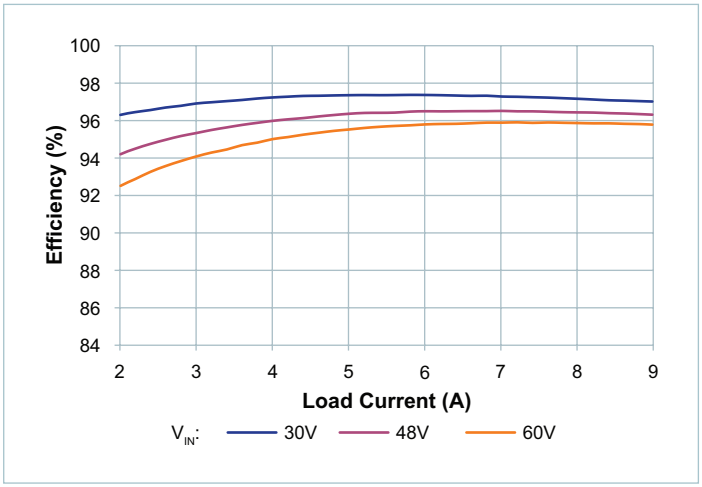


Figure 55 — *System efficiency, nominal trim, board temperature = 25°C*

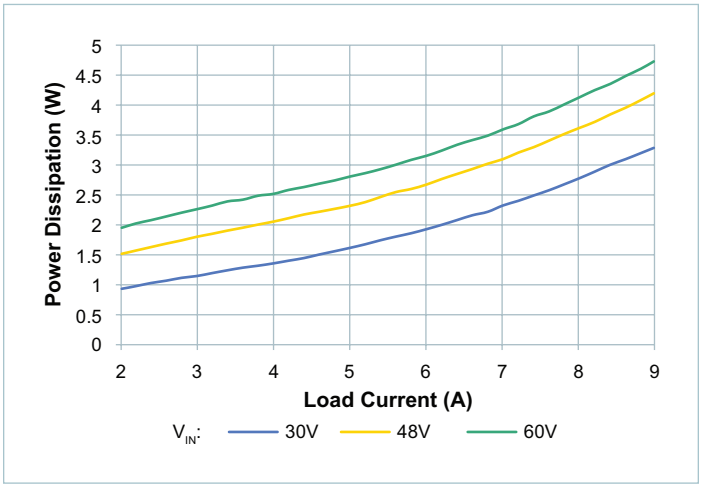


Figure 58 — *System power dissipation, nominal trim, board temperature = 25°C*

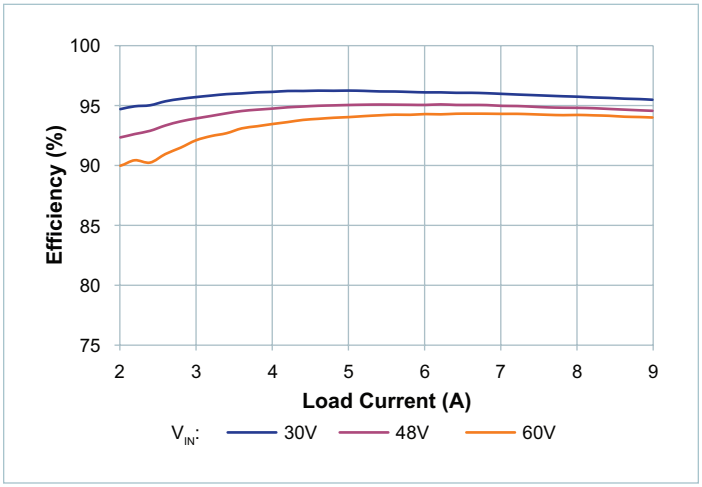


Figure 56 — *System efficiency, low trim, board temperature = 25°C*

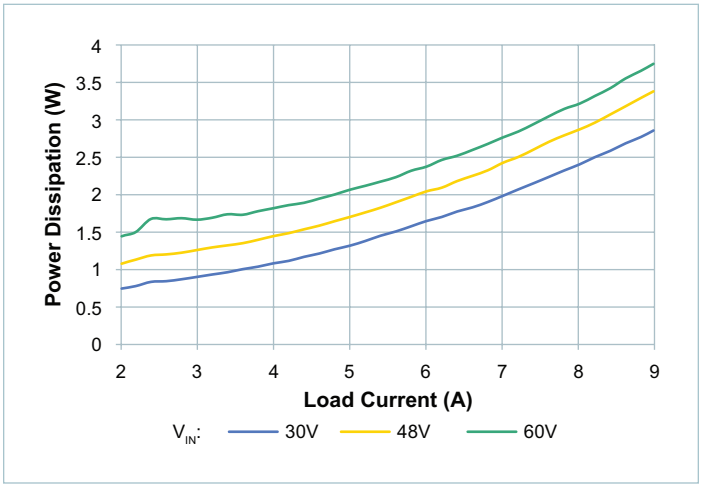


Figure 59 — *System power dissipation, low trim, board temperature = 25°C*

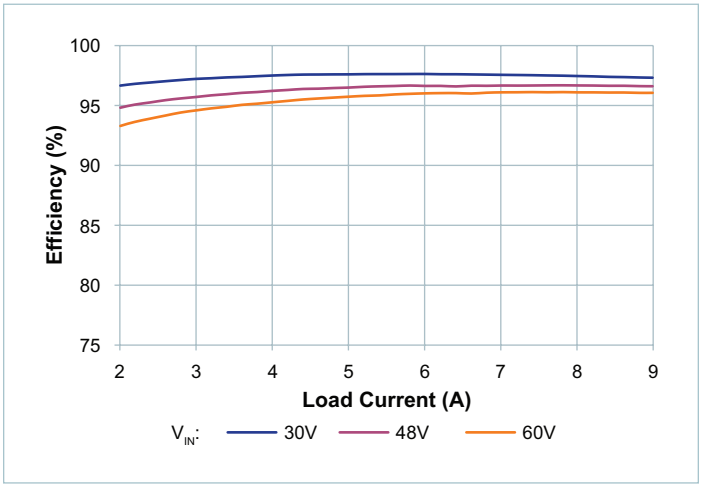


Figure 57 — *System efficiency, high trim, board temperature = 25°C*

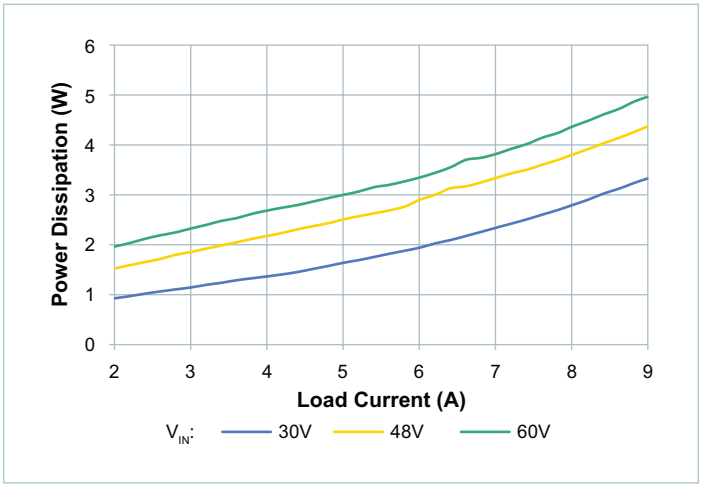


Figure 60 — *System power dissipation, high trim, board temperature = 25°C*

PI3586-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

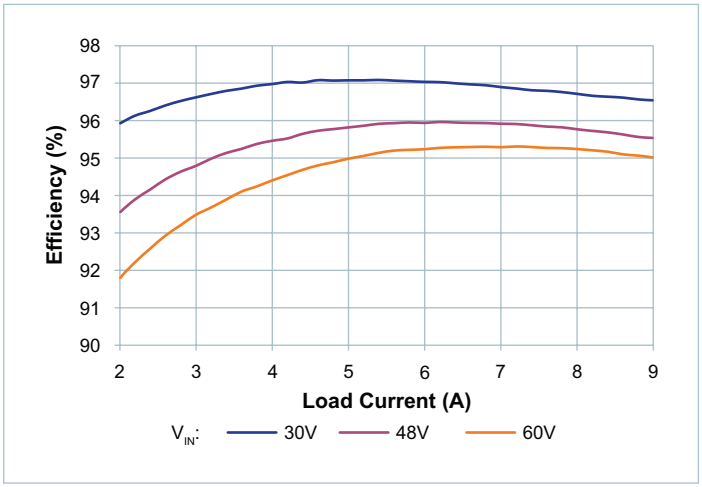


Figure 61 *— System efficiency, nominal trim, board temperature = 90°C*

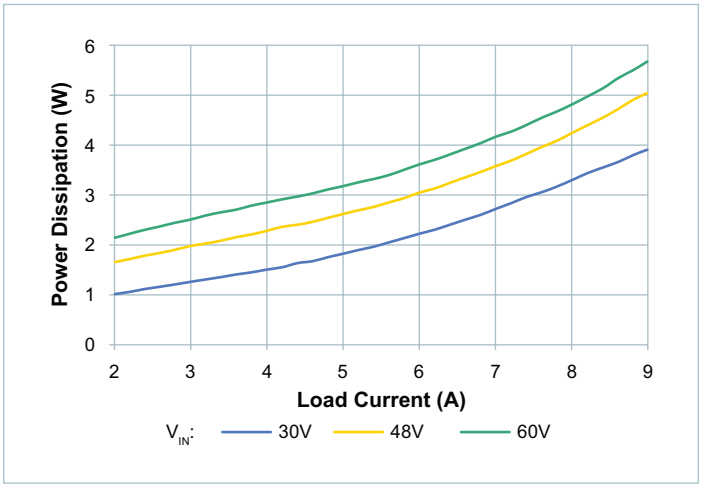


Figure 64 *— System power dissipation, nominal trim, board temperature = 90°C*

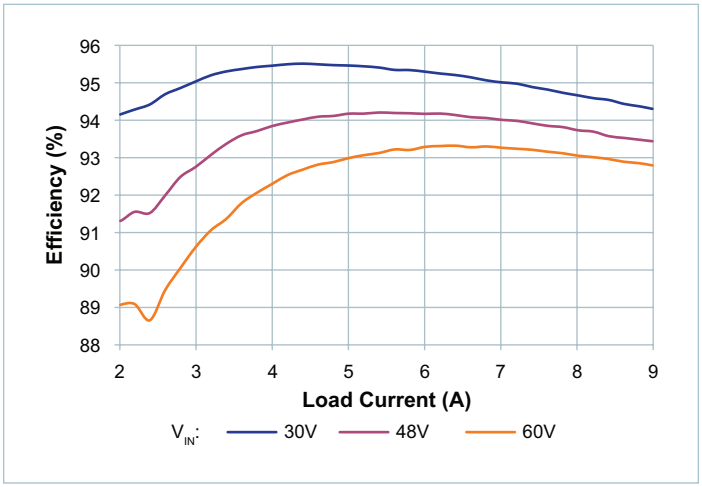


Figure 62 *— System efficiency, low Trim, board temperature = 90°C*

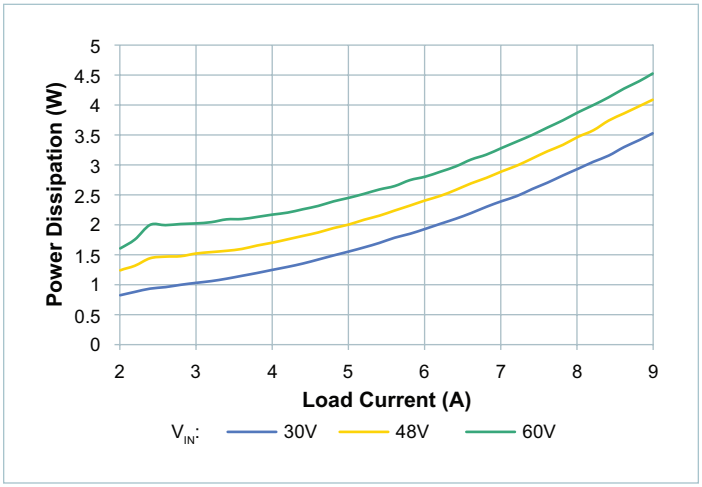


Figure 65 *— System power dissipation, low trim, board temperature = 90°C*

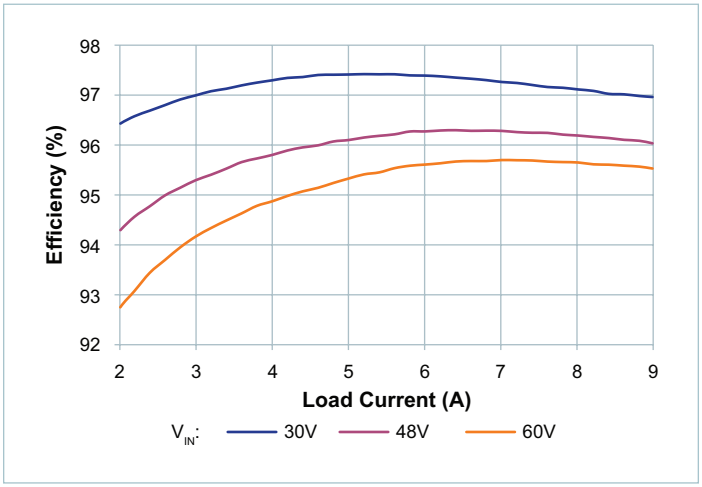


Figure 63 *— System efficiency, high trim, board temperature = 90°C*

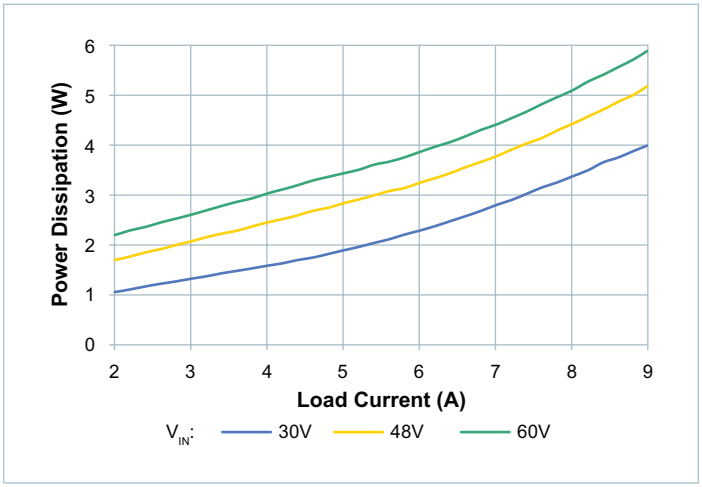


Figure 66 *— System power dissipation, high trim, board temperature = 90°C*

PI3586-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

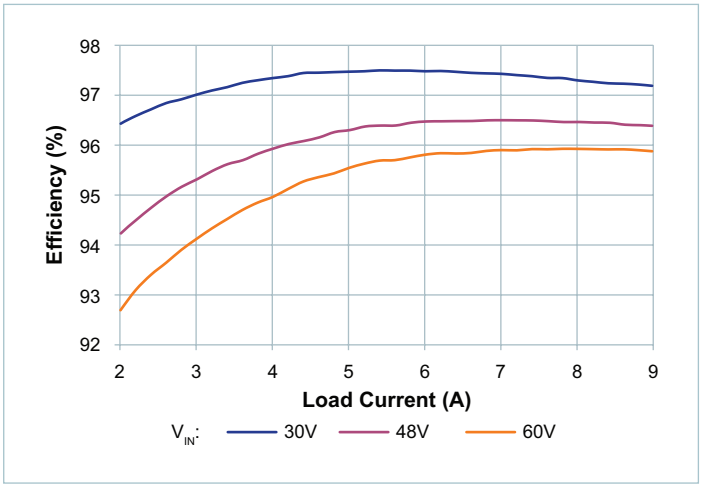


Figure 67 — *System efficiency, nominal trim, board temperature = –20°C*

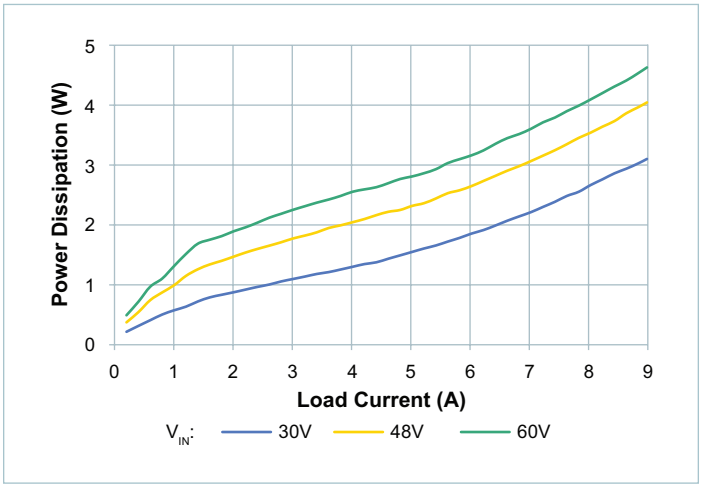


Figure 70 — *System power dissipation, nominal trim, board temperature = –20°C*

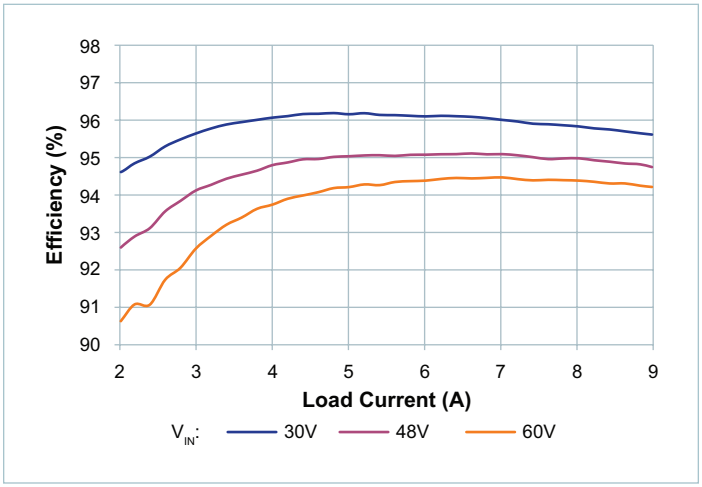


Figure 68 — *System efficiency, low trim, board temperature = –20°C*

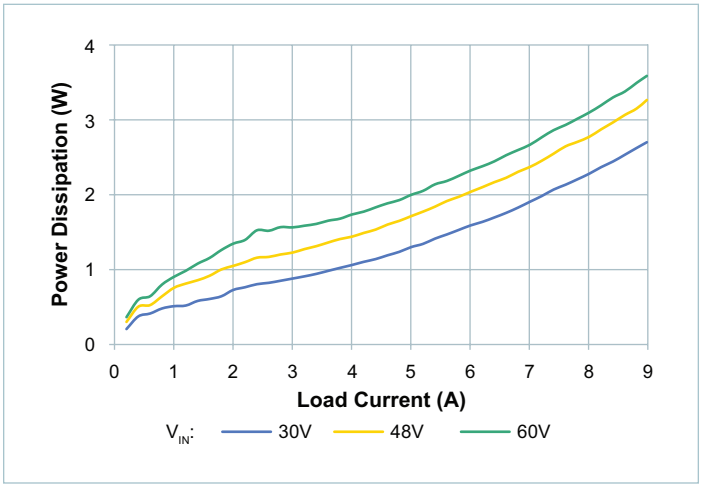


Figure 71 — *System power dissipation, low trim, board temperature = –20°C*

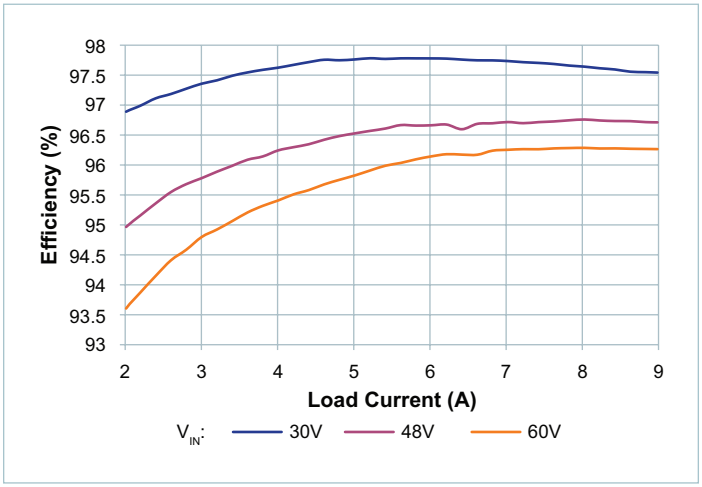


Figure 69 — *System efficiency, high trim, board temperature = –20°C*

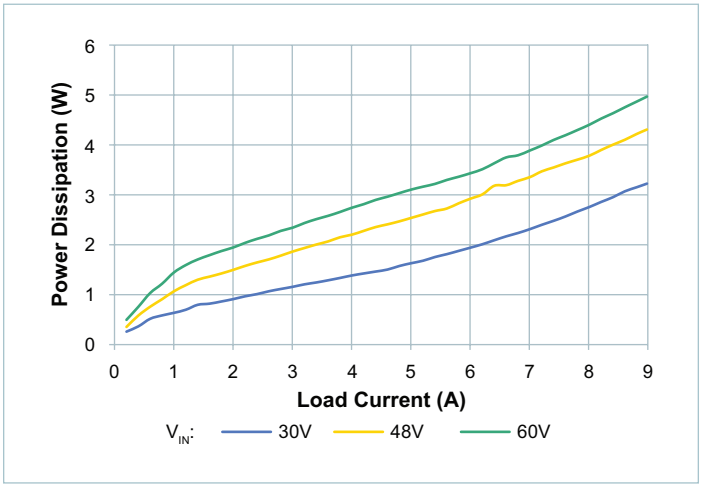


Figure 72 — *System power dissipation, high trim, board temperature = –20°C*

PI3586-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

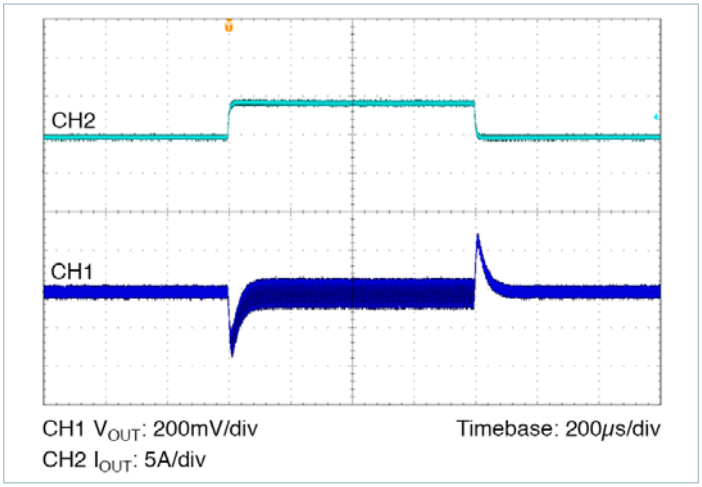


Figure 73 — *Transient response: 50% to 100% load, at 1A/µs; nominal line, nominal trim, C_{OUT} = 6 x 47µF ceramic*

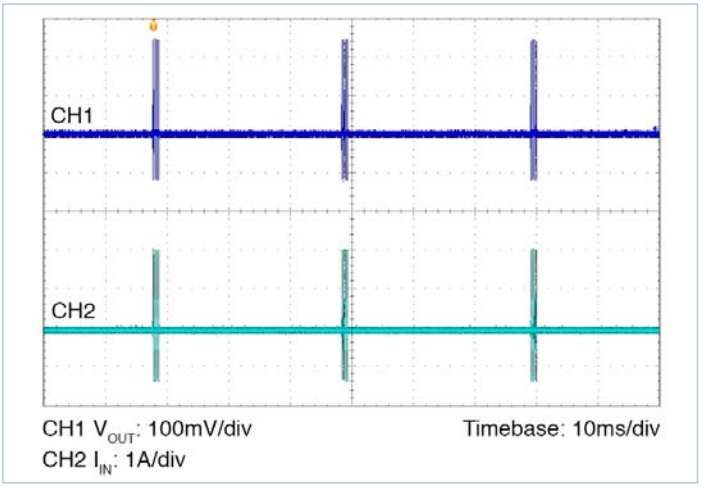


Figure 76 — *Output short circuit, nominal line*

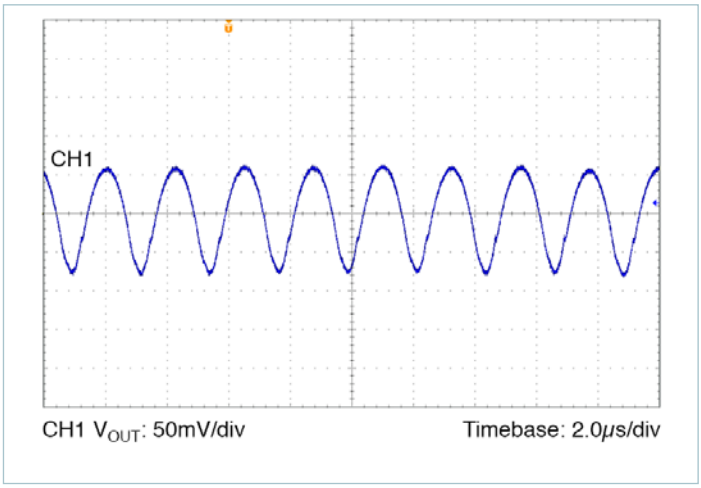


Figure 74 — *Output voltage ripple: nominal line, nominal trim, 100% load, C_{OUT} = 6 x 47µF ceramic, 20MHz BW*

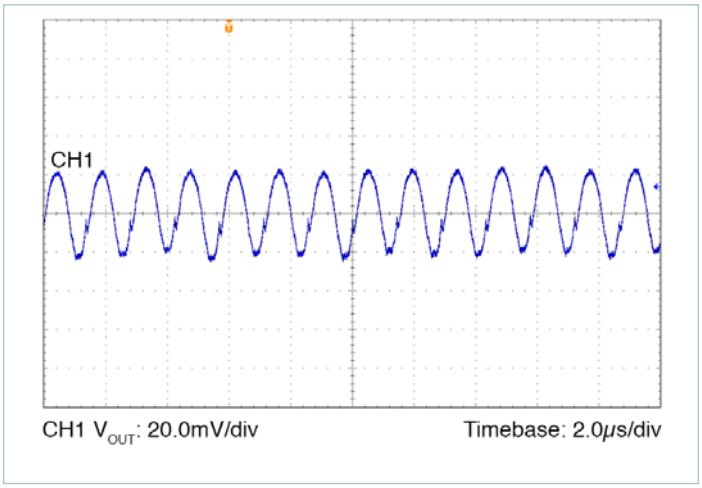


Figure 77 — *Output voltage ripple: nominal line, nominal trim, 50% load, C_{OUT} = 6 x 47µF ceramic, 20MHz BW*

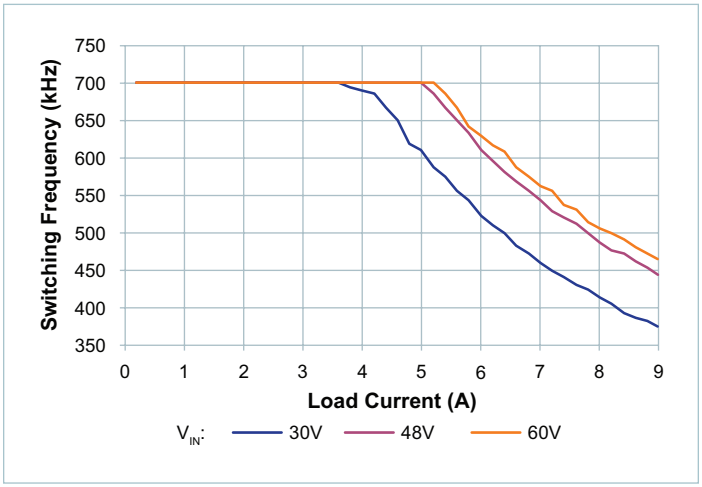


Figure 75 — *Switching frequency vs. load, nominal trim*

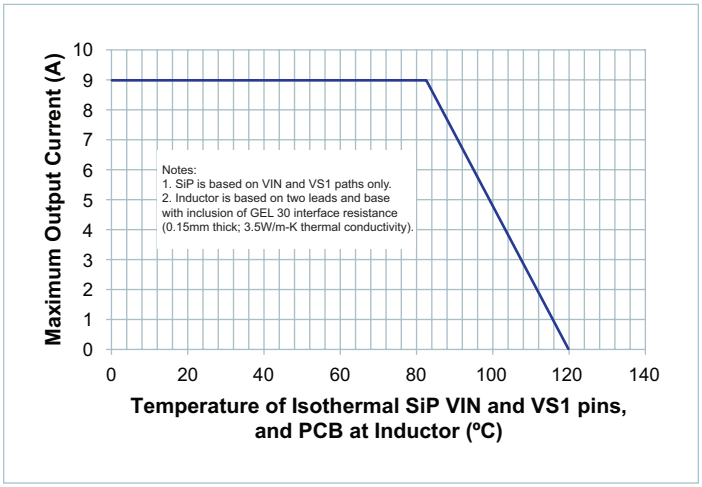


Figure 78 — *System thermal specified operating area: max I_{OUT} at nominal trim vs. temperature at locations noted*

PI3586-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

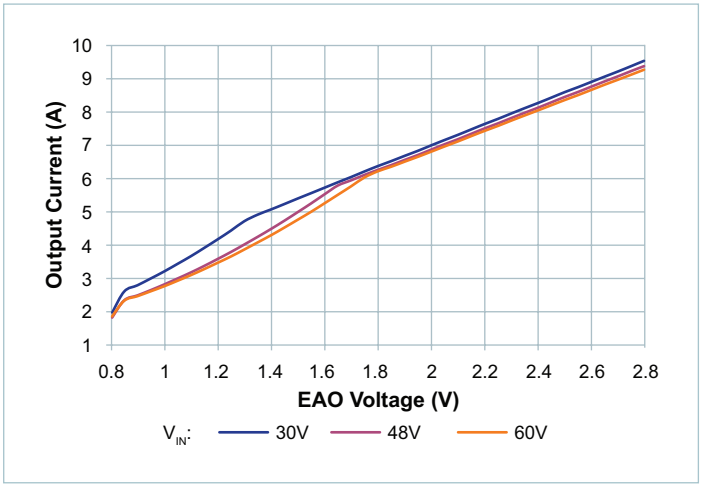


Figure 79 — *Output current vs. V_{EAO}, nominal trim*

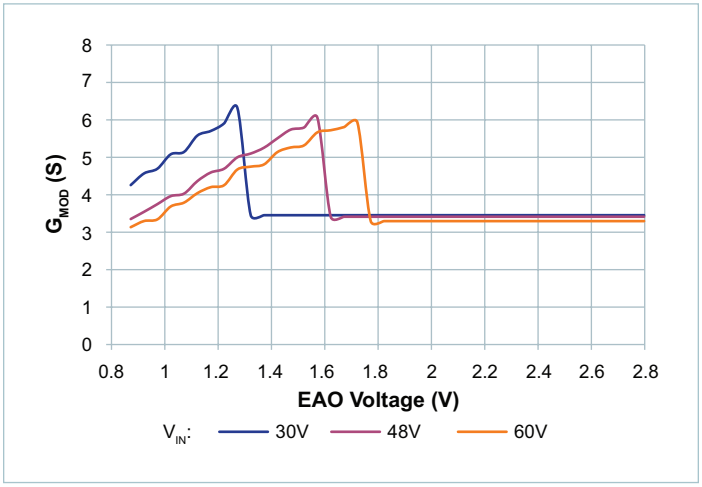


Figure 80 — *Small-signal modulator gain vs. V_{EAO}, nominal trim*

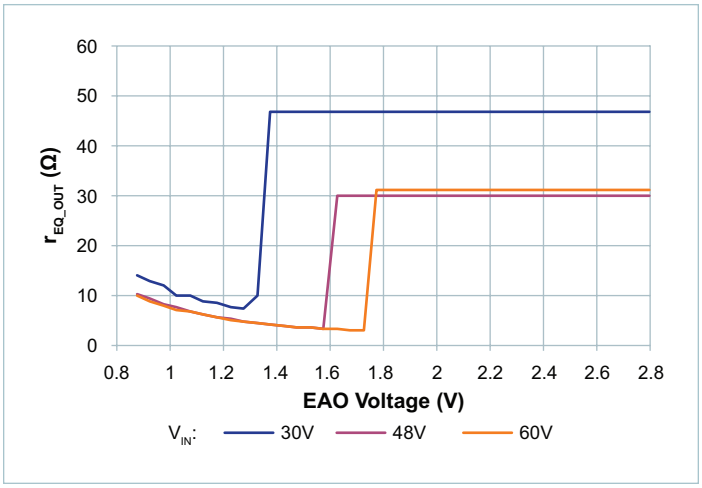


Figure 81 — *r_{EQ_OUT} vs V_{EAO}, nominal trim*

Functional Description

The PI358x-00 is a family of highly integrated ZVS Buck regulators. The PI358x-00 has an output voltage that can be set within a prescribed range. Performance and maximum output current are characterized with a specific external power inductor (see Table 4).

For basic operation, Figure 82 shows the connections and components required. No additional design or settings are required.

If the exact recommended part cannot be used, the description column of Table 1 serves as a guidance for an alternate part. Any substitute parts should be equal to or better than the original for all parameters.

Reasonable engineering judgment in making the choices for alternative components and a detailed verification of the performance would be highly recommended.

ENABLE (EN)

EN is the enable pin of the converter. The EN pin is referenced to SGND and permits the user to turn the regulator on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below V_{EN_LO} with respect to SGND will disable the regulator output.

Remote Sensing

If remote sensing is required, the PI358x-00 product family is equipped with a general purpose op-amp. This amplifier can allow full differential remote sense by configuring it as a differential follower and connecting the V_{DIFF} pin to the EAIN pin.

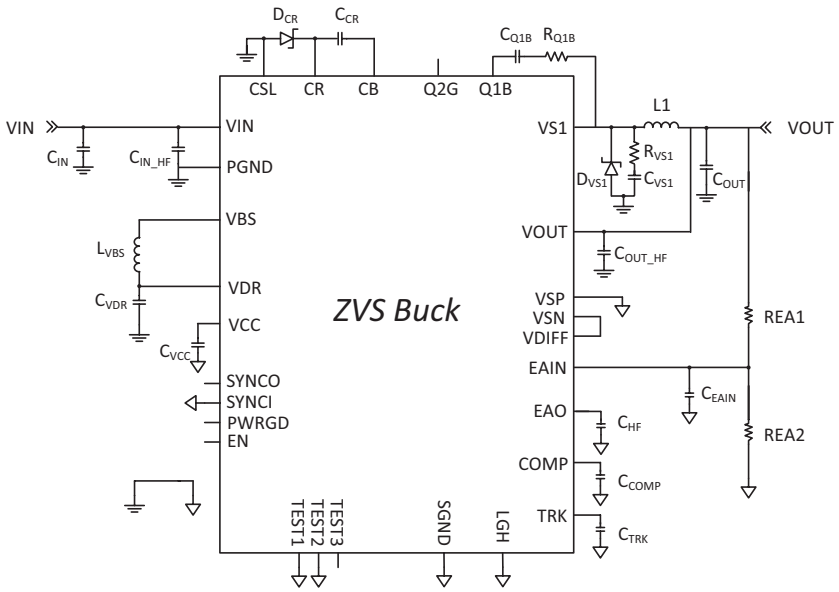


Figure 82 — *ZVS Buck with required components*

Reference Designation	Manufacturer	Part Number	Value	Description
C_{OUT}	Refer to Table 6 – Recommended input and output capacitor components			
C_{IN}				
C_{OUT_HF}	Murata	GRM21BR72A474KA73K	0.47µF	Capacitor, X7R Ceramic, 0.47uF, 100V, 10%, 0805
C_{IN_HF}	Murata	GRM21BR72A474KA73K	0.47µF	Capacitor, X7R Ceramic, 0.47µF, 100V, 10%, 0805
C_{Q1B}	TDK	C1608X7R1C224K080AC	0.22µF	Capacitor, X7R, 0.22µF, 16V, 10%, 0603
R_{Q1B}	Rohm	ESR03EZPJ1R3	1.3Ω	RES SMD 1.3Ω 5% 1/4W 0603
D_{CR}	Nexperia	PMEG4002EL		Diode, Schottky, PMEG4002EL Philips, 40V, 200mA, SOD882
C_{CR}	Murata	GCM188R71H473KA55D	47nF	Capacitor, Ceramic, 47nF, 50V, 0603
D_{VS1}	Nexperia	PMEG10010ELR		Diode, Schottky, 100V, 1A, low V_F, low leakage current, SOD123W
C_{VS1}	TDK	C1608C0G2A102J080AA	1nF	Capacitor, C0G, 100V, 1nF, 5%, 0603
R_{VS1}	Samsung	RUT1608FR300CS	0.3Ω	RES SMD 300mΩ 1%1/8W 0603
L_{VBS}	TDK	MLZ2012M100HT	10µH	Inductor, 10µH ±20%, 300mA, 2Mhz, 0805
C_{VDR}, C_{VCC}	Murata	GRM188R71A225KE15D	2.2µF	Capacitor, X7R Ceramic, 2.2µF, 10V, 0603
C_{EAIN}	56pF			
C_{COMP}	4.7nF			
C_{HF}	56pF			
C_{TRK}	47nF			
L1	Refer to Inductor Pairing			
REA1	Refer to Application Description for Output Voltage Set Point			
REA2				

Table 1 — *List of recommended components*

Soft Start

The PI358x-00 requires an external soft-start capacitor from the TRK pin to SGND to control the rate of rise of the output voltage. Increasing the capacitance of this soft-start capacitor will increase the start-up ramp period. See, "Soft Start Adjustment and Track," in the Applications Description section for more details.

Output Voltage Selection

The PI358x-00 output voltage can be set with REA1 and REA2 as shown in Figure 82. Table 2 defines the allowable operational voltage ranges for the PI358x-00 family. Refer to the Output Voltage Set Point Application Description for details.

Device	Output Voltage	
	Nominal	Range
PI3583-00-QFYZ	3.3V	2.2 – 4.0V
PI3585-00-QFYZ	5.0V	3.8 – 6.5V
PI3586-00-QFYZ	12.0V	6.5 – 14V

Table 2 — *PI358x-00 family output voltage ranges*

Output Current Limit Protection

The PI358x-00 has a current limit protection, which prevents the output from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024µs, a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

The PI358x-00 also has short circuit protection which can rapidly stop switching to protect against catastrophic failure of an external component such as a saturated inductor. If short circuit protection is triggered the PI358x-00 will complete the current cycle and stop switching. The module will attempt to soft start after Fault Restart Delay (t_{FR_DLY}).

Input Undervoltage Lockout

If V_{IN} falls below the input Undervoltage Lockout (UVLO) threshold, but remains high enough to power the bias supply, the PI358x-00 will complete the current cycle and stop switching. The system will soft start once the input voltage is reestablished and after the Fault Restart Delay.

Input Overvoltage Lockout

If V_{IN} exceeds the input Overvoltage Lockout (OVLO) threshold (V_{OVLO}), while the controller is running, the PI358x-00 will complete the current cycle and stop switching. If V_{IN} remains above OVLO for at least t_{FR_DLY}, then the input voltage is considered reestablished once V_{IN} goes below V_{OVLO}-V_{OVLO_HYS}. If V_{IN} goes below OVLO before t_{FR_DLY} elapses, then the input voltage is considered reestablished once V_{IN} goes below V_{OVLO}. The system will soft start once the input voltage is reestablished and after the Fault Restart Delay.

Output Overvoltage Protection

The PI358x-00 family is equipped with output Overvoltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds $V_{OVP\text{-}REL}$ or $V_{OVP\text{-}ABS}$, the regulator will complete the current cycle and stop switching. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

Overtemperature Protection

The PI358x features an over temperature protection (OTP), which will not engage until after the product is operated above the maximum rated temperature. The OTP circuit is only designed to protect against catastrophic failure due to excessive temperatures and should not be relied upon to ensure the device stays within the recommended operating temperature range. Thermal shutdown terminates switching and discharges the soft-start capacitor. The PI358x will restart after the excessive temperature decreases by 30°C.

Pulse Skip Mode (PSM)

PI358x-00 features a Pulse Skip Mode (PSM) to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold (PSM_{SKIP}). Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Pulse Skip Mode threshold.

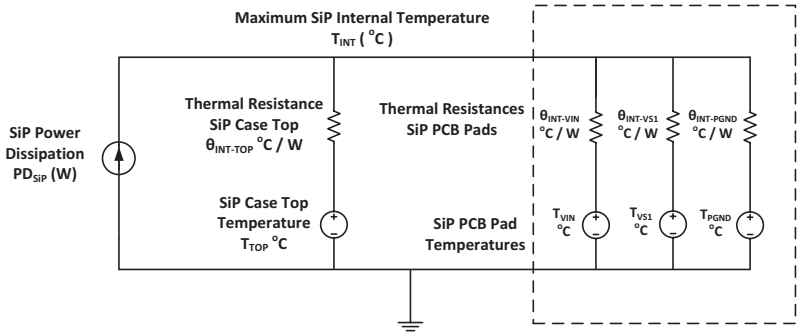
Variable Frequency Operation

Each PI358x-00 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 3), to operate at peak efficiency across line and load variations. At higher loads, the base operating frequency will decrease to accommodate storage of more energy in the main inductor. By increasing the switching period, ZVS operation is preserved throughout the total input line and output trim voltage ranges, maintaining optimum efficiency. The ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

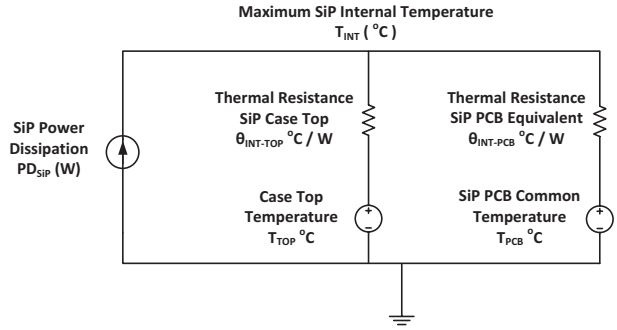
Thermal Characteristics

Figure 83(a) and 83(c) thermal impedance models that can predict the maximum temperature of the hottest component for a given operating condition. This model assumes that all customer PCB connections are at one temperature, which is PCB equivalent Temperature T_{PCB} °C.

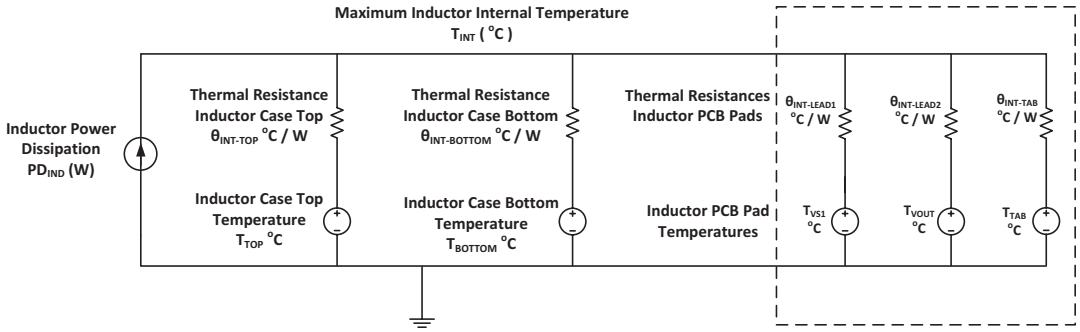
The SiP model can be simplified as shown in Figure 83(b). which assumes all PCB nodes are at the same temperature.



(a)



(b)



(c)

Figure 83 — *PI358x-00 thermal model (a), SiP simplified version (b) and inductor thermal model (c)*

Where the symbol in Figure 83(a) and (b) is defined as the following:

$\theta_{INT\text{-}TOP}$	the thermal impedance from the hottest component inside the SiP to the top side
$\theta_{INT\text{-}PCB}$	the thermal impedance from the hottest component inside the SiP to the customer PCB, assuming all pins are at one temperature.
$\theta_{INT\text{-}VIN}$	the thermal impedance from the hottest component inside the SiP to the circuit board VIN pads.
$\theta_{INT\text{-}VS1}$	the thermal impedance from the hottest component inside the SiP to the circuit board VS1 pads.
$\theta_{INT\text{-}PGND}$	the thermal impedance from the hottest component inside the SiP to the circuit board for PGND pin 1 and pin 37 combined.

Where the symbol in Figure 83(c) is defined as the following:

$\theta_{INT\text{-}TOP}$	the thermal impedance from the hot spot to the top surface of the core.
$\theta_{INT\text{-}BOT}$	the thermal impedance from the hot spot to the bottom surface of the core.
$\theta_{INT\text{-}TAB}$	the thermal impedance from the hot spot to the metal mounting tab on the core body.
$\theta_{INT\text{-}LEAD1}$	the thermal impedance from the hot spot to one of the mounting leads. Since the leads are the same thermal impedance, there is no need to specify by explicit pin number.
$\theta_{INT\text{-}LEAD2}$	the thermal impedance from the hot spot to the other mounting lead.

The following equation can predict the junction temperature based on the heat load applied to the SiP and the known ambient conditions with the simplified thermal circuit model:

$$T_{INT} = \frac{PD + \frac{T_{TOP}}{\theta_{INT\text{-}TOP}} + \frac{T_{PCB}}{\theta_{INT\text{-}PCB}}}{\frac{1}{\theta_{INT\text{-}TOP}} + \frac{1}{\theta_{INT\text{-}PCB}}} \qquad (1)$$

Thermal Characteristics (Cont.)

Product System	Simplified SiP Thermal Impedances		Detailed SiP Thermal Impedances			
	$\theta_{INT-TOP}$ (°C / W)	$\theta_{INT-PCB}$ (°C / W)	$\theta_{INT-TOP}$ (°C / W)	$\theta_{INT-VIN}$ (°C / W)	$\theta_{INT-VS1}$ (°C / W)	$\theta_{INT-PGND}$ (°C / W)
PI3583-00	44	0.53	44	1.4	0.95	7.7
PI3585-00	54	0.64	54	2.6	0.92	9.6
PI3586-00	29	0.42	29	0.88	1.2	2.2

Table 3 — *PI358x-00 SiP thermal impedance*

Product System	Inductor Part Number	Thermal Impedances			
		$\theta_{INT-TOP}$ (°C / W)	$\theta_{INT-LEAD1}$, $\theta_{INT-LEAD2}$ (°C / W)	$\theta_{INT-BOTTOM}$ (°C / W)	$\theta_{INT-TAB}$ (°C / W)
PI3583-00	HCV1206-R42-R	68	58	16	180
PI3585-00	HCV1206-R42-R	110	58	21	140
PI3586-00	HCV1206-R90-R	13	40	20	190

Table 4 — *Inductor thermal model parameters*

SiP Power Dissipation as Percentage of Total System Losses

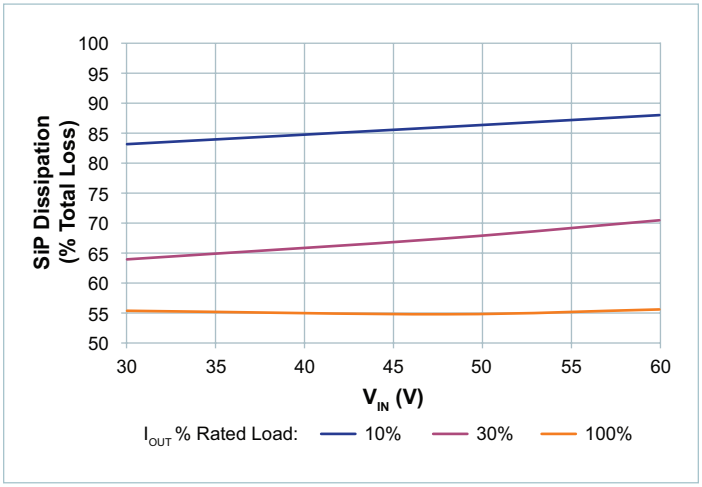


Figure 84 — *PI3583-00-QFYZ*

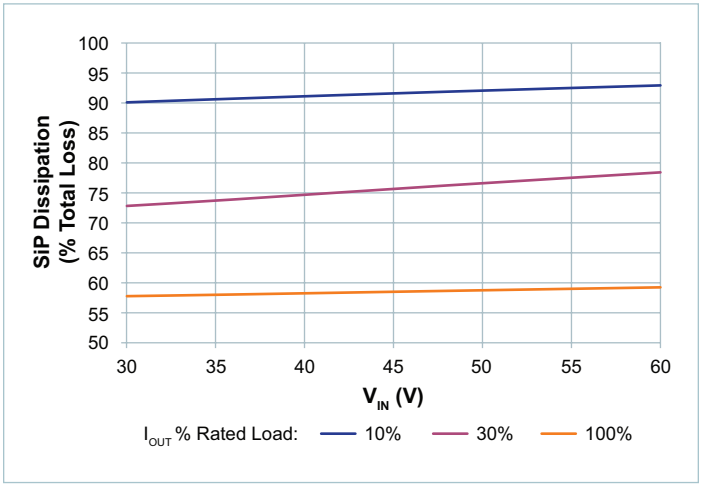


Figure 85 — *PI3585-00-QFYZ*

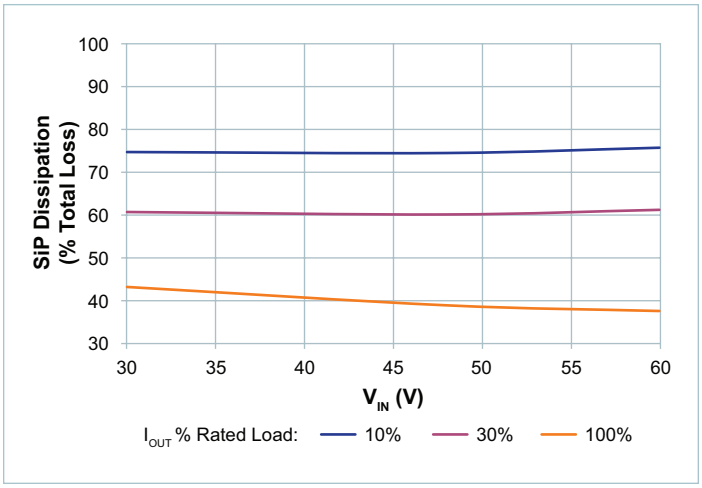


Figure 86 — *PI3586-00-QFYZ*

Application Description

Output Voltage Set Point

The PI358x-00 family of Buck Regulators utilizes V_{REF}, an internal reference for regulating the output voltage. The output voltage setting is accomplished using external resistors as shown in Figure 87. Select R2 to be at or around 1kΩ for best noise immunity. Use Equations 2 and 3 to determine the proper value based on the desired output voltage.

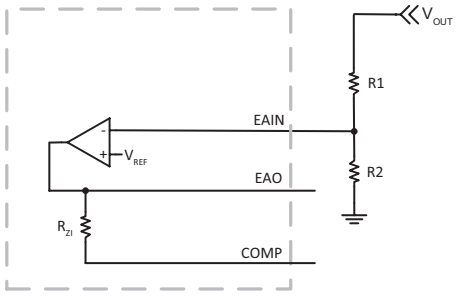


Figure 87 — *External resistor divider network*

$$V_{OUT} = V_{REF} \bullet \frac{R1 + R2}{R2} \qquad (2)$$

$$R1 = R2 \bullet \frac{V_{OUT} - V_{REF}}{V_{REF}} \qquad (3)$$

Where:

$V_{REF} = V_{EAIN}$

Soft Start Adjust and Tracking

The TRK pin offers a means to adjust the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an external capacitor and a fixed charge current to provide a Soft-Start Time t_{SS} for all PI358x-00 regulators. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = \left(t_{TRK} \bullet I_{TRK} \right) \qquad (4)$$

where t_{TRK} is the soft-start time and I_{TRK} is a 50µA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at start up, simply connect all PI358x-00 device TRK pins together. This type of tracking will force all connected regulators to start up and reach regulation at the same time (see Figure 88(a)).

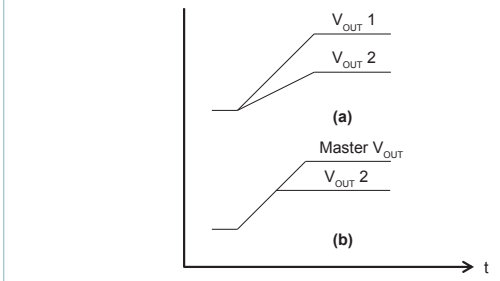


Figure 88 — *PI358x-00 tracking responses*

For Direct Tracking, choose the PI358x-00 with the highest output voltage as the master and connect the master to the TRK pin of the other PI358x-00 regulators through a divider (Figure 88) with the same ratio as the slave's feedback divider.

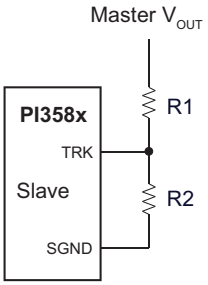


Figure 89 — *Voltage divider connections for direct tracking*

All connected PI358x-00 regulator soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 88(b). All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI358x-00 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 5 details the specific inductor value and part number utilized for each PI358x-00.

Product System	Value (nH)	Mfr.	Part Number	Max Operating Temperature $T_{INT-IND}$ (°C)
PI3583-00-QFYZ	420	Eaton	HCV1206-R42-R	125
PI3585-00-QFYZ	420	Eaton	HCV1206-R42-R	125
PI3586-00-QFYZ	900	Eaton	HCV1206-R90-R	125

Table 5 — *PI358x-00 inductor pairing*

Parallel Operation

Multiple PI358x-00 can be connected in parallel to increase the output capability of a single output rail. When connecting modules in parallel, each EAO, TRK and EN pin should be connected together. EAIN pins should remain separated, each with a REA1 and REA2, to reject noise differences between different modules' SGND pins. Current sharing will occur automatically in this manner so long as each inductor is the same value. Refer to the Electrical Characteristics table for maximum array size and array rated output current. Current sharing may be considered independent of synchronization and/or interleaving. Modules do not have to be interleaved or synchronized to share current.

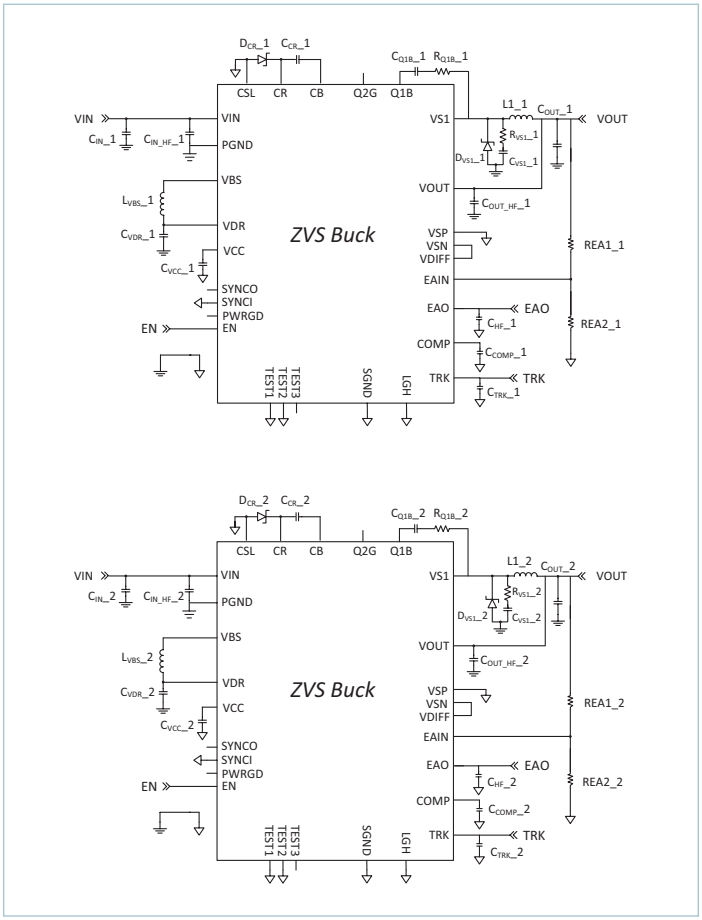


Figure 90 — *PI358x-00 parallel operation*

Due to the high output current capability of a single module and CrCM occurring at approximately 50% rated load, interleaving is not supported.

Use of the PI358x-00 SYNCI pin is practical only under a limited set of conditions. Synchronizing to another converter or to a fixed external clock source can result in a significant reduction in output power capability or higher than expected ripple.

Filter Considerations

The PI358x-00 requires low impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high frequency decoupling for the power stage. The PI358x-00 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source.

Table 7 shows the recommended input and output capacitors to be used for the PI358x-00 as well as per capacitor RMS ripple current and the input and output ripple voltages. Table 6 lists the recommended input and output ceramic capacitors manufacturer and part numbers. It is very important to verify that the voltage supply source as well as the interconnecting lines are stable and do not oscillate.

Input Filter Case 1 — Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e.: ceramic type):

The voltage source impedance can be modeled as a series R_{LINE} L_{LINE} circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{LINE} > \frac{L_{LINE}}{C_{IN} \bullet \left| r_{EQ\_IN} \right|} \tag{5}$$

$$R_{LINE} << \left| r_{EQ\_IN} \right| \tag{6}$$

Where r_{EQ_IN} can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, Equation 6. However, R_{LINE} cannot be made arbitrarily low otherwise Equation 5 is violated and the system will show instability, due to an under-damped RLC input network.

Input Filter case 2 — Inductive source and local, external input decoupling capacitance with significant $R_{C_{IN}}$ ESR (i.e., electrolytic type):

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor L_{LINE}.

Notice that the high performance ceramic capacitors C_{IN_INT} within the PI358x-00 should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$\left| r_{EQ\_IN} \right| > R_{C_{IN}} \tag{7}$$

$$\frac{L_{LINE}}{C_{IN} \bullet R_{C_{IN}}} < \left| r_{EQ\_IN} \right| \tag{8}$$

Equation 8 shows that if the aggregate ESR is too small – for example by using very high quality input capacitors (C_{IN}) – the system will be under-damped and may even become destabilized. As noted, an octave of design margin in satisfying Equation 7 should be considered the minimum. When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

VDR Bias Regulator

The VDR bias regulator is a ZVS switching regulator that is intended primarily to power the internal controller and driver circuitry. The power capability of this regulator is sized for the PI358x-00, with adequate reserve for the application it was intended for.

It may be used for as a pullup source for open collector applications and for other very low power uses with the following restrictions:

1. The total external loading on VDR must be less than I_{VDR}.
2. No direct connection is allowed. Any noise source that can disturb the VDR voltage can also affect the internal controller operation. A series impedance is required between the VDR pin and any external circuitry.
3. All loads must be locally decoupled using a 0.1µF ceramic capacitor. This capacitor must be connected to the VDR output through a series resistor no smaller than 1kΩ, which forms a low-pass filter.

Additional System Design Considerations

1. *Inductive loads:* As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high current Schottky diode from the output voltage to PGND close to the PI358x-00 is recommended for these applications.
2. *Low voltage operation:* There is no isolation from an SELV (Safety-Extra-Low-Voltage) power system. Powering low voltage loads from input voltages as high as 60V may require additional consideration to protect low voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS (transient voltage suppressor) gating an external load switch is an example of such protection.

Input / Output	Manufacturer	Part Number	Value	Description
Output	Murata	GRM32EC70J107ME15	100µF	100µF 6.3V 1210 X7S
	Murata	GRM32ER71A476KE15	47µF	47µF 10V 1210 X7R
	Murata	GRM32DR71E106KA12	10µF	10µF 25V 1210 X7R
Input	Murata	GRM32ER72A225KA35	2.2µF	2.2µF 100V 1210 X7R
	or Murata	GRM32ER71K475KE14L	4.7µF	4.7µF 80V 1210 X7R

Table 6 — *Recommended input and output capacitor components*

Product	Load Current (A)	C_{IN}	C_{OUT}	C_{IN} Ripple Current (A_{RMS})	C_{OUT} Ripple Current (A_{RMS})	V_{IN} Ripple (mV_{P-P})	V_{OUT} Ripple (mV_{P-P})	Load Step (A) (1A/µs)	V_{OUT} Droop and Kick (mV_{PP})	V_{OUT} Recovery Time (µs)
PI3583	10	6 x 2.2µF	6 x 100µF	3.3	7.0	430	40	5	160	80
PI3585	10	6 x 2.2µF	6 x 47µF	4.3	8.3	380	60	5	130	80
PI3586	10	6 x 2.2µF	6 x 10µF	5	6.0	600	140	4.5	330	80

Table 7 — *Recommended input and output capacitor quantity and performance*

Layout Guidelines

To optimize maximum efficiency and low noise performance from a PI358x-00 design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 91. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

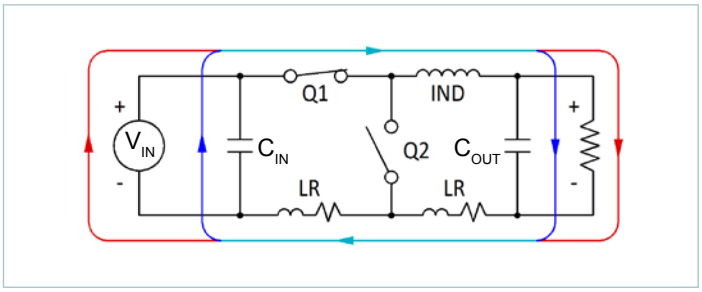


Figure 91 — *Typical buck regulator*

The path between the C_{OUT} and C_{IN} capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on. Figure 92, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI358x-00 performance.

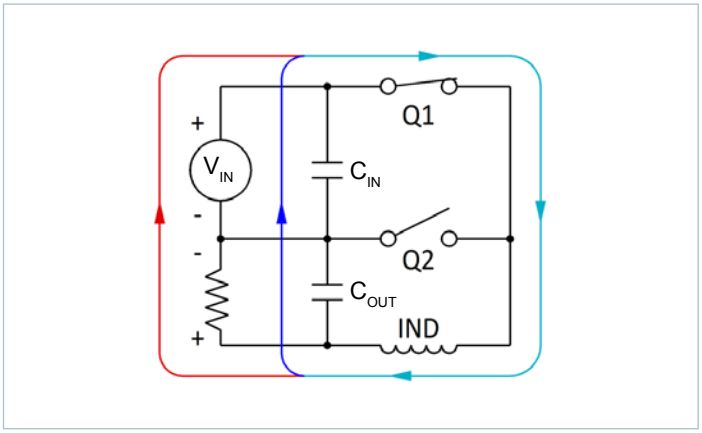


Figure 92 — *Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of C_{IN}'s current is used to satisfy the output load and to recharge the C_{OUT} capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the C_{OUT} capacitor as shown in Figure 93. During this period C_{IN} is also being recharged by the V_{IN}. Minimizing C_{IN} loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the C_{IN} loop and C_{OUT} loop is vital to minimize switching and GND noise.

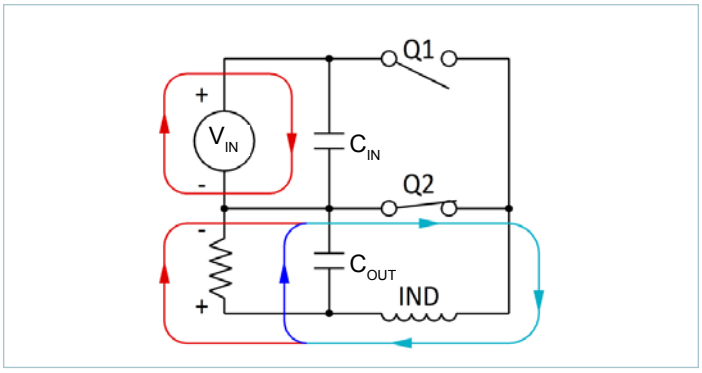


Figure 93 — *Current flow: Q2 closed*

Figure 94 illustrates the tight path between C_{IN} and C_{OUT} (and V_{IN} and V_{OUT}) for the high AC return current. The external C_{IN} capacitor needs to be connected to the input of the SiP through a low inductance connection, which is especially important due to the lack of internal input capacitance. The PI358x-00 evaluation board uses a layout optimized for performance in this way.

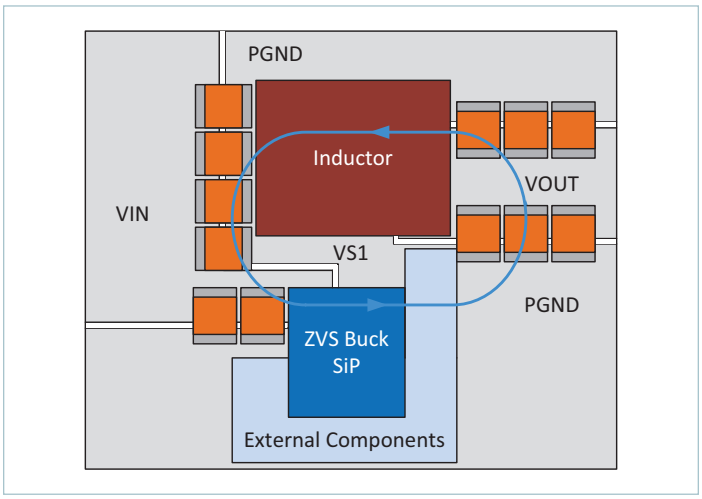


Figure 94 — *Recommended layout for optimized AC current within the SiP, inductor, and ceramic input and output capacitors*

Besides the critical power path involving the input/output of the converter, the input/output capacitors and the inductor, the routing of some powertrain supporting components are also sensitive to routing parasitics. For example, L_{VBS} and C_{VDR} are passive components for internal bias supply switcher; D_{VS1}, C_{VS1} and R_{VS1} are clamped to protect VS1, the main switching node. In either condition, a path with low inductance is required.

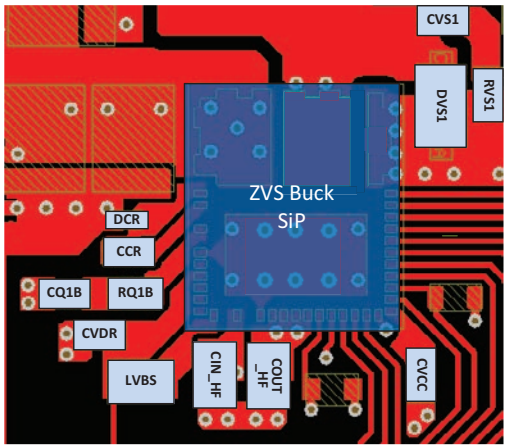


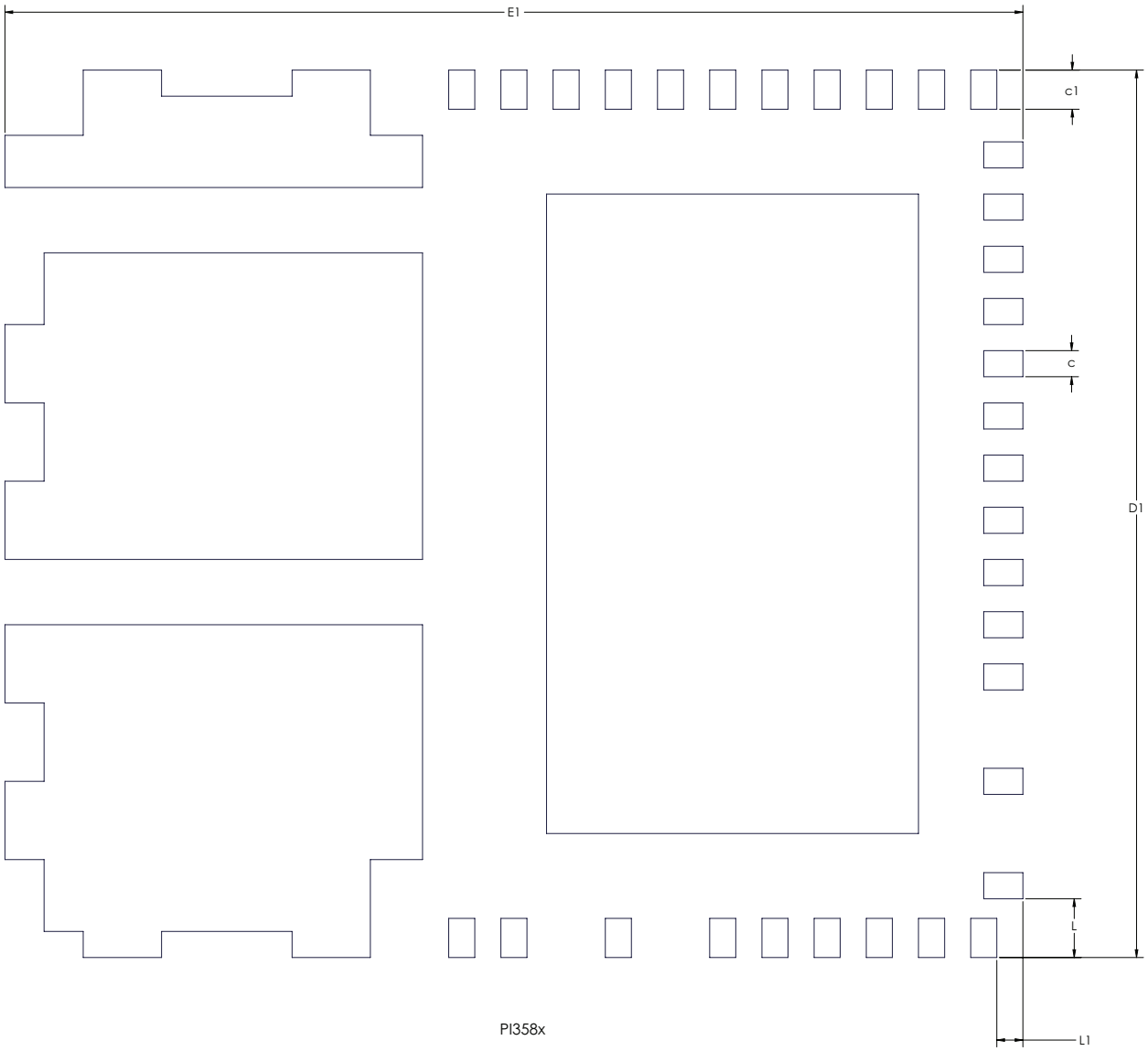
Figure 95 — *Example layout of external components on a PI358x evaluation board*

Here is a list of external components to the SiP which needs to have low inductance routes:

C_{OUT_HF}, C_{IN_HF}, C_{Q1B}, R_{Q1B}, D_{CR}, C_{CR}, D_{VS1}, C_{VS1}, R_{VS1}, L_{VBS}, C_{VDR}, C_{VCC}. An example layout from the evaluation board is shown in Figure 95. These external components are placed locally to the SiP and connect to the relevant pin with wide traces. Some of them have the other end connecting through vias to the ground plane in the underneath layer. A similar practice is expected in customer applications.

In many cases the powertrain or its related layout is critical and sensitive to routing parasitics. A direct copy of the Vicor reference PCB layout is recommended.

Recommended PCB Footprint



PI358x

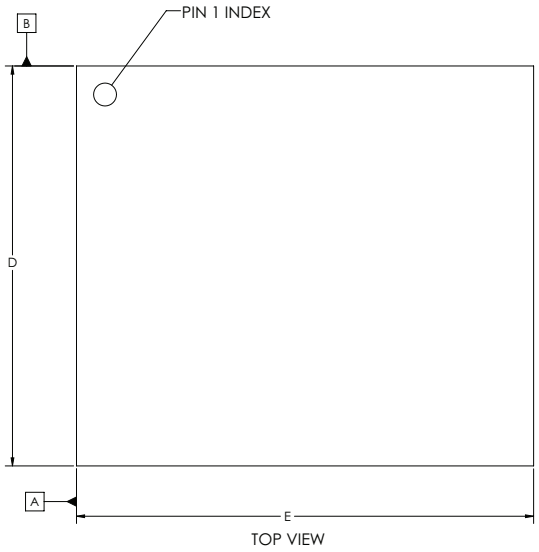
PCB LAND PATTERN

GQFN PACKAGE

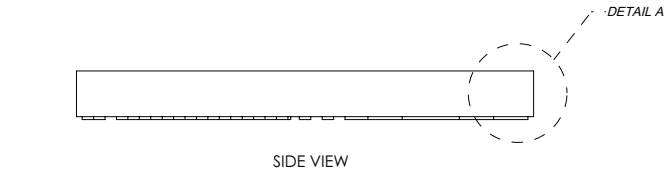
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
C	.15	.20	.25
C1	.25	.30	.35
D1		6.80	
E1		7.80	
L		.50	
L1	.15	.20	.25

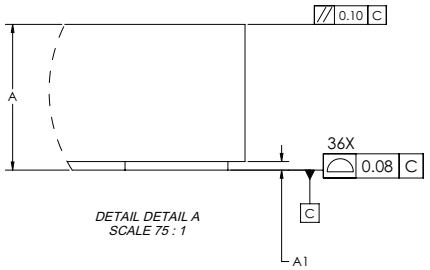
Recommended receiving footprint for PI358x-00 7 x 8mm package.

Package Drawings

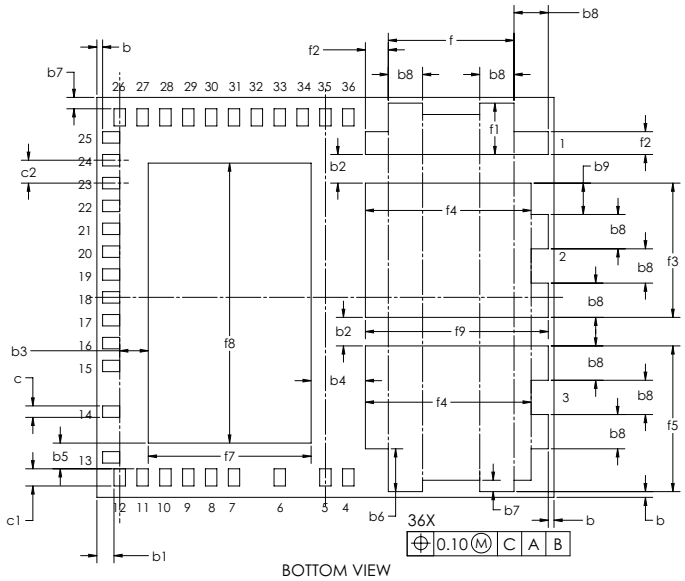


PI358X GQFN			
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	.80	.85	.90
A1	.00	-	.05
b		.10 REF	
b1		.30 REF	
b2		.50 REF	
b3		.50 REF	
b4		.95 REF	
b5		.65 REF	
b6		.75 REF	
b7		.20 REF	
b8		.60 REF	
b9		.55 REF	
c	.15	.20	.25
c1	.25	.30	.35
c2		.40 BSC	
D		7.00 BSC	
E		8.00 BSC	
f	2.15	2.20	2.25
f1	.85	.90	.95
f2	.35	.40	.45
f3	2.30	2.35	2.40
f4	2.85	2.90	2.95
f5	2.50	2.55	2.60
f7	2.80	2.85	2.90
f8	4.85	4.90	4.95
f9	3.15	3.20	3.25





NOTES:
1. 'c2' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. COPLANARITY SHALL NOT EXCEED 0.08 MM.
4. WARPAGE SHALL NOT EXCEED 0.10 MM.
5. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERD AS SPECIAL CHARACTERISTIC(S).
6. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
7. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.
8. RoHS COMPLIANT PER CST-0001LATEST REVISION.



Revision History

Revision	Date	Description	Page Number(s)
1.0	10/09/18	Initial release	n/a

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