VIA PFM™ Family

PFA175x240x400Axx

C US RoHS CE TÜV C NRTL US

Isolated AC-DC Converter with PFC in 125 mm Package

Features & Benefits

- Universal input (85 to 264 V_{AC})
- 24 V_{OUT}, regulated, isolated
- 400 W maximum power
- High efficiency
- Built-in EMI filtering
- Chassis mount or board mount packaging options
- Always-on, self-protecting converter control architecture
- SELV Output
- Two temperature grades including operation to -40°C
- Robust package
- Versatile thermal management
- Safe and reliable secondary-side energy storage
- High MTBF
- 127 W/cubic inch power density
- External rectification and transient protection required

Typical Applications

- Small cell base stations
- Telecom switching equipment
- LED lighting
- Test and measurement equipment
- 200 - 400 W Industrial power systems
- Office equipment

Product Description

The VIA PFM is a highly advanced 400 W AC-DC converter operating from a rectified universal AC input which delivers an isolated and regulated Safety Extra Low Voltage (SELV) 24 V secondary output.

This unique, ultra-low profile module incorporates AC-DC conversion, integrated filtering and transient surge protection in a chassis mount or PCB mount form factor.

The VIA PFM enables a versatile two-sided thermal strategy which greatly simplifies thermal design challenges.

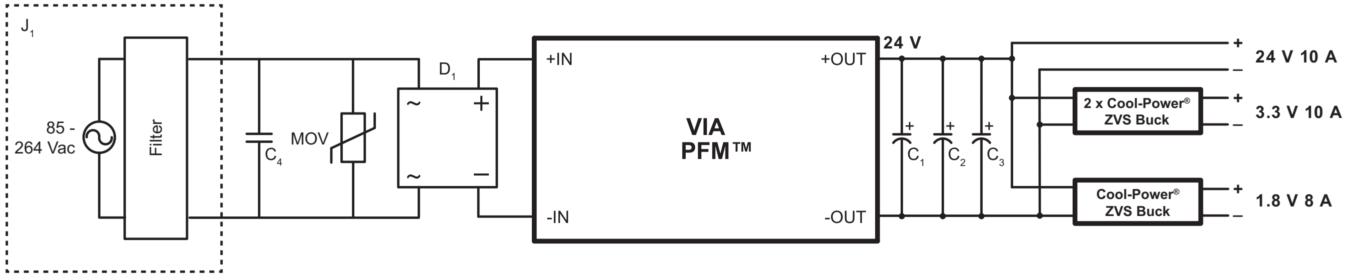
When combined with downstream Vicor DC-DC conversion components and regulators, the VIA PFM allows the Power Design Engineer to employ a simple, low-profile design which will differentiate the end-system without compromising on cost or performance metrics.

Size:
4.91 x 1.40 x .37 in
124.8 x 35.5 x 9.3 mm

Part Ordering Information

Device	Input Voltage Range	Package/Pin Type	Output Voltage x 10	Temperature Grade	Output Power	Revision	Package Size	Version
VIA PFM	175	x	x	x	400	A	x	x
PFA = VIA PFM	175 = 85 to 264 V	B = Chassis C = PCB Short Pin G = PCB Long Pin	240 = 24.0 V	T = Telecom C = Comm	400 = 400 W	A	3 = 125 mm	3 = Always On

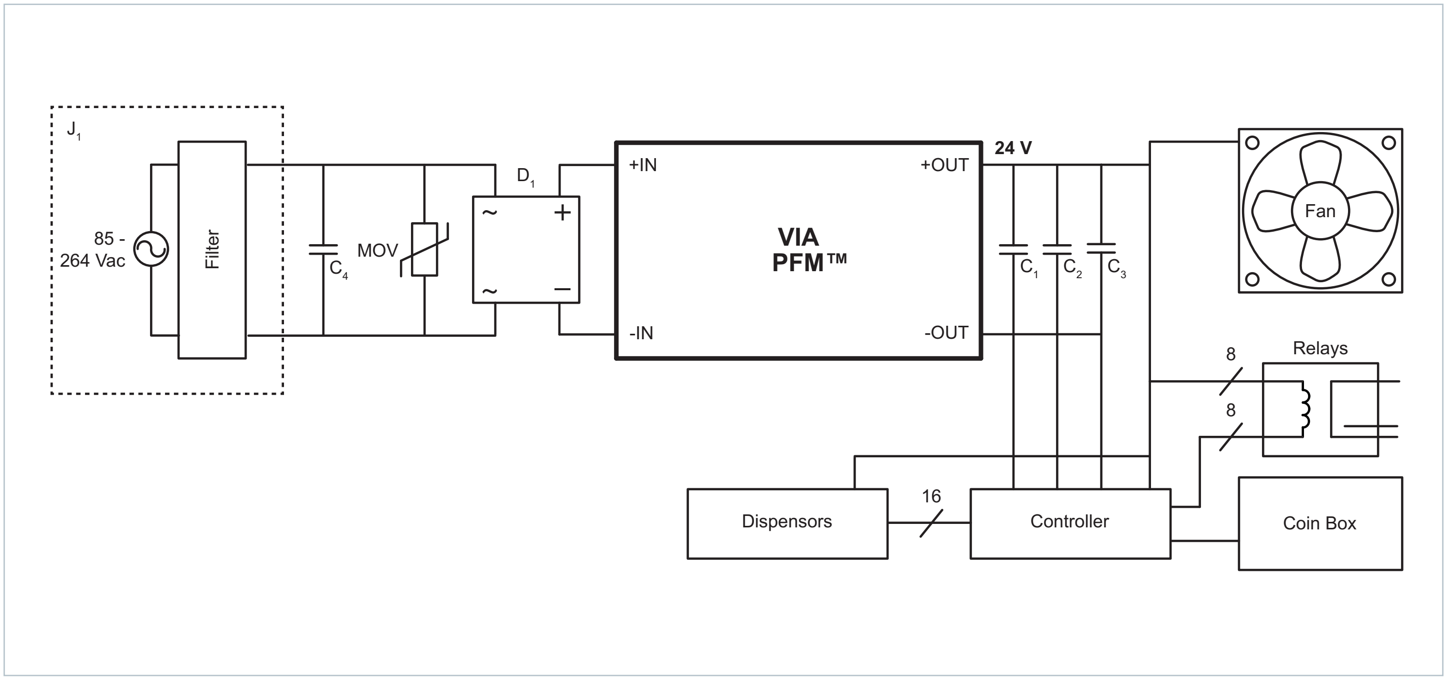
Typical PCB Mount Applications



The PCB terminal option allows mounting on an industry standard printed circuit board, with two different pin lengths. Vicor offers a variety of downstream DC-DC converters driven by the 24V output of the VIA PFM. The 24V output is usable directly by loads that are tolerant of the PFC line ripple, such as fans, motors, relays, and some types of lighting. Use downstream DC-DC Point of Load converters where more precise regulation is required.

Parts List for Typical PCB Mount Applications	
J1	**Delta** 06AR2 EMI Filter Entry Module, C14 6 A 250 V 5 x 20 mm fuseholder
F1 (mount in J1)	**Littelfuse** 0216008.MXP 8 A 250 VAC 5 x 20 mm holder
D1	**Fairchild** GBPC1210W 12 A 100 V PTH
C1, C2, C3	**Nichicon** UVR1V153MRD 15,000 µF 35 V 4.3 A 25 x 50 mm bent 90° **or**
	CDE 380LX153M035A022 15,000 µF 35 V 5.6 A 35 x 30 mm snap in **or**
	Sic Safco Cubisic LP A712062 22,000 µF 35 V 5.8 A 45 x 75 x 12 mm rectangular
C4	**Panasonic** ECQ-U2A474ML 0.47 µF 275 V

Typical Chassis Mount Applications



The VIA PFM is available in Chassis Mount option, saving the cost of a PCB and allowing access to both sides of the power supply for cooling. The parts list below minimizes the number of interconnects required between necessary components, and selects components with terminals traditionally used for point to point chassis wiring.

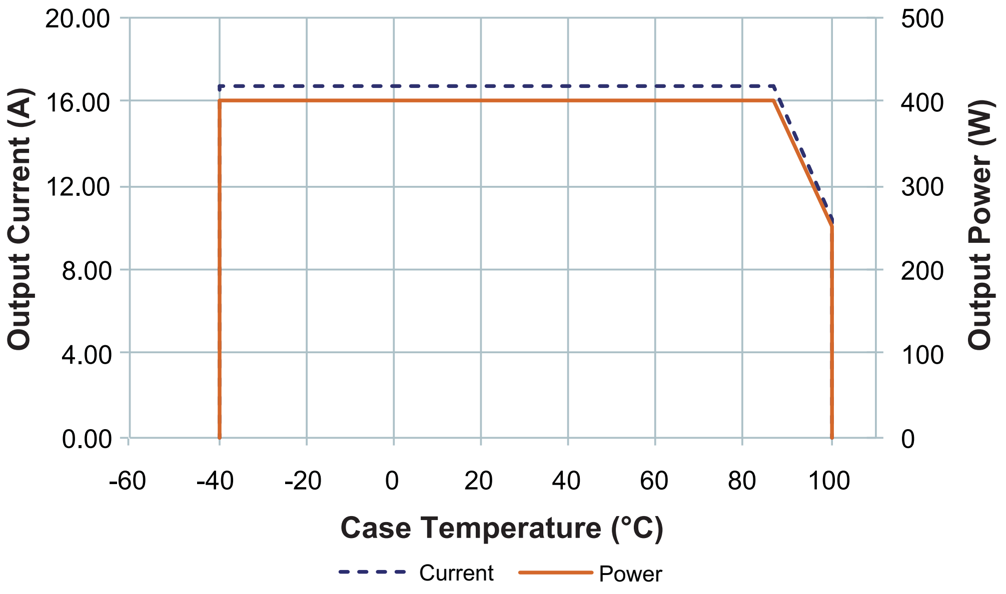
Parts List for Typical Chassis Mount Applications	
J1	**Delta** 06AR2 EMI Filter Entry Module, C14 6 A 250 V 5 x 20 mm fuseholder
F1 (mount in J1)	**Littelfuse** 0216008.MXP 8 A 250 VAC 5 x 20 mm holder
D1	**Fairchild** GBPC1210FS 12 A 1000 V 0.25” QC TERMINAL
C1, C2, C3	**Nichicon** LNT1V153MSE 35 V 5.1 A 35 x 83 mm screw terminal **or**
C1	**Kemet** ALS30A23KE063 35 V 14.2 A 51 x 84 mm screw terminal
C4	**Panasonic** ECQ-U2A474ML 0.47 µF 275 V
MOV	**Littelfuse** TMOV20RP300E VARISTOR 10 kA 300 V 250J 20 mm

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
Input voltage +IN to –IN	1 ms max	0	600	Vpk
Input voltage (+IN to -IN)	Continuous, Rectified	0	275	V_{RMS}
Output voltage (+Out to -Out)		-0.5	29	V_{DC}
Output current		0.0	24.7	A
Operating junction temperature	T-Grade	-40	125	°C
Storage temperature	T-Grade	-40	125	°C
Dielectric Withstand*	See note below			
Input-Case	Basic Insulation	2121		Vdc
Input-Output	Reinforced Insulation	2121		Vdc
Output-Case	Functional Insulation	707		Vdc

* Please see Dielectric Withstand section. See page 18.



Safe Operating Area

Electrical Specifications

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, T_J = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified product grade. C_{OUT} is 44,000 µF +/- 20% unless otherwise specified.

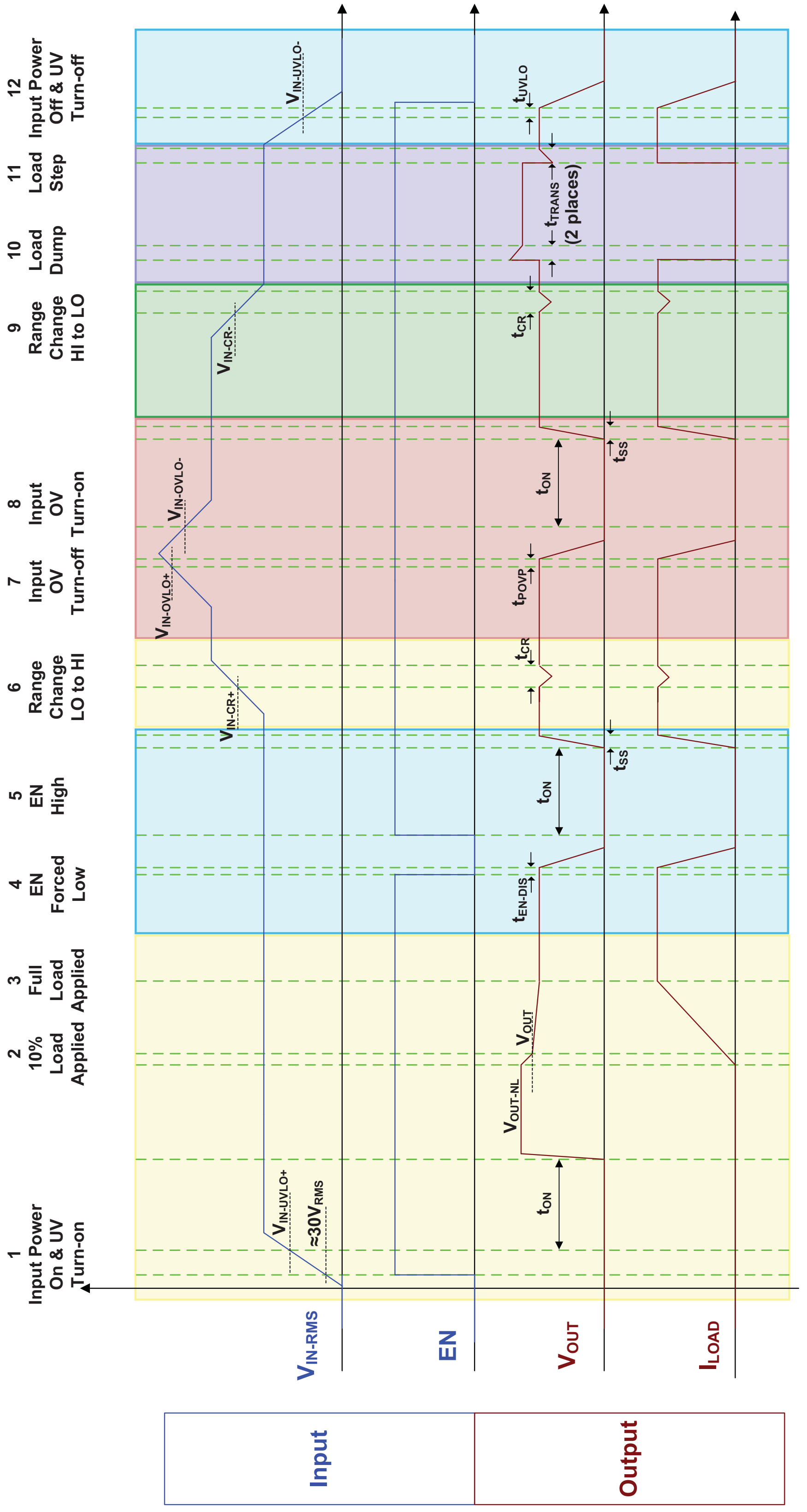
Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specification						
Input voltage range, continuous operation	V_{IN}		**85**		**264**	V_{RMS}
Input voltage range, transient, non-operational (peak)	V_{IN}	1 ms			600	V
Input voltage cell reconfiguration low-to-high threshold	$V_{IN\text{-}CR+}$			145	**148**	V_{RMS}
Input voltage cell reconfiguration high-to-low threshold	$V_{IN\text{-}CR-}$		**132**	135		V_{RMS}
Input current (peak)	I_{INRP}	See Figure 8, Startup Waveforms			12	A
Source line frequency range	f_{line}		47		63	Hz
Power factor	PF	Input power >200 W		0.96		-
Input inductance, maximum	L_{IN}	Differential mode inductance, common mode inductance may be higher			1	mH
Input capacitance, maximum	C_{IN}	After bridge rectifier, between +IN and - IN			1.5	µF
No Load Specification						
Input power – no load, maximum	P_{NL}				7	W
Power Output Specification						
Output voltage set point	V_{OUT}	V_{IN} = 230 Vrms, 100% Load	23	24	25	V
Output voltage, no load	$P_{OUT\text{-}NL}$	Over all operating steady state line conditions	**21**		**26**	V
Output voltage range (transient)	V_{OUT}	Non-faulting abnormal line and load transient conditions	**15**		**28.8**	V
Output power	P_{OUT}	See SOA on Page 4			**400**	W
Efficiency	η	V_{IN} = 230 V, full load, exclusive of input rectifier losses	90.5	92		%
		85 V < V_{IN} < 264 V, full load, exclusive of input rectifier losses	**90**			%
		85 V < V_{IN} < 264 V, 75% load, exclusive of input rectifier losses	90			%
Output voltage ripple, switching frequency	$V_{OUT\text{-}PP\text{-}HF}$	Over all operating steady-state line and load conditions, 20 MHz BW, measured at C3, Figure 5		100	**1000**	mV
Output voltage ripple line frequency	$V_{OUT\text{-}PP\text{-}LF}$	Over all operating steady-state line and load conditions, 20 MHz BW		1.5	3.5	V
Output capacitance (external)	$C_{OUT\text{-}EXT}$	Allows for ±20% capacitor tolerance	**27000**		**60000**	µF
Output turn-on delay	T_{ON}	From V_{IN} applied		500	**1000**	ms
Start-up setpoint aquisition time	T_{SS}	Full load		500	1000	ms
Cell reconfiguration response time	T_{CR}	Full load		5.5	11	ms
Voltage deviation (transient)	$\%V_{OUT\text{-}TRANS}$		-37.5		20	%
Recovery time	T_{TRANS}			300	600	ms
Line regulation	$\%V_{OUT\text{-}LINE}$	Full load			3	%
Load regulation	$\%V_{OUT\text{-}LOAD}$	10% to 100% load			3	%
Output current (continuous)	I_{OUT}	SOA			16.7	A
Output current (transient)	$I_{OUT\text{-}PK}$	20 ms duration, average power ≤P_{OUT}, max			**24.7**	A

Electrical Specifications (Cont.)

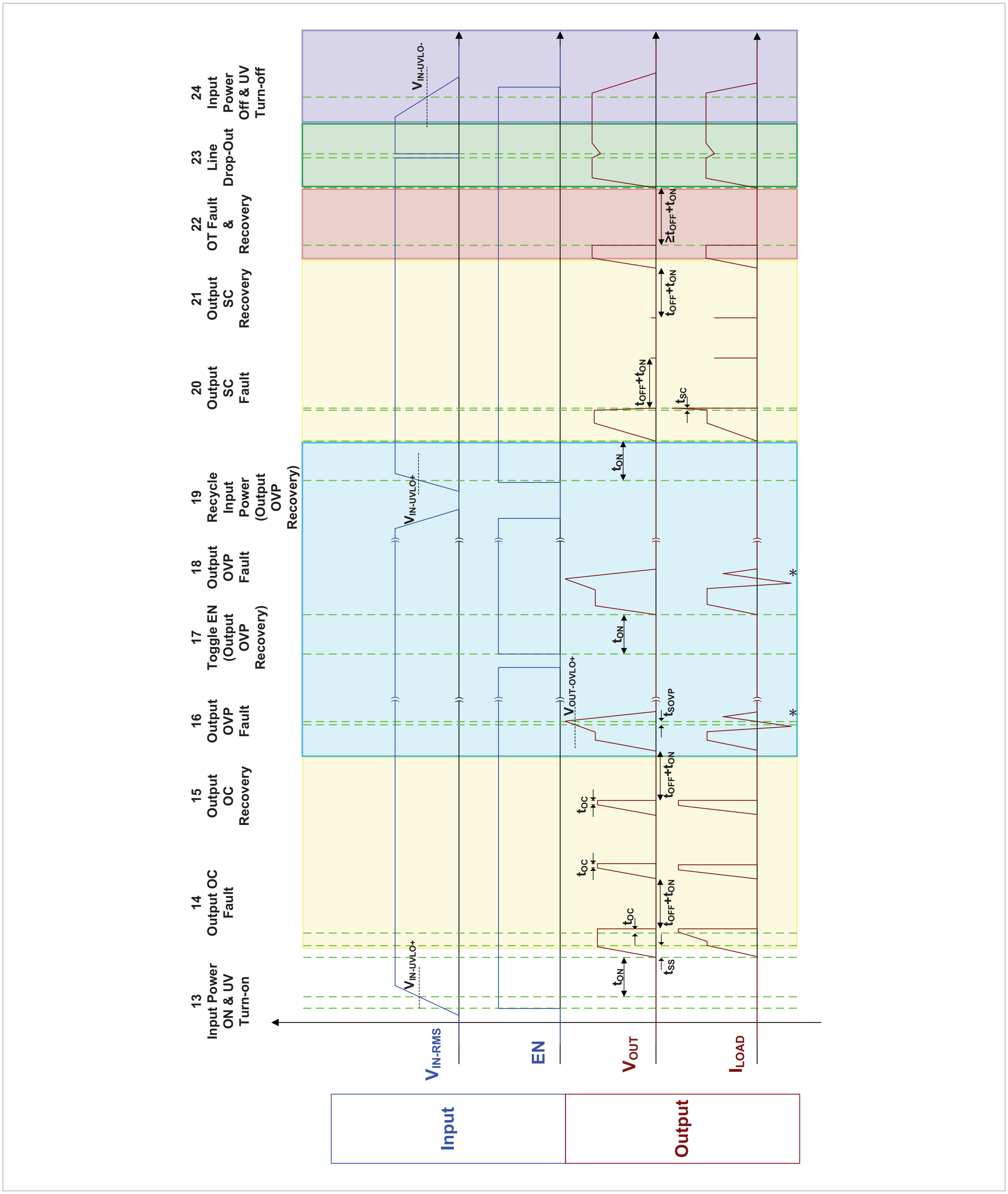
Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, T_J = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified product grade. C_{OUT} is 44,000 µF +/- 20% unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protections						
Input undervoltage turn-on	$V_{IN\text{-}ULVO+}$	See Timing Diagram		74	**83**	V_{RMS}
Input undervoltage turn-off	$V_{IN\text{-}ULVO-}$		**65**	71		V_{RMS}
Input overvoltage turn-on	$V_{IN\text{-}ULVO-}$	See Timing Diagram	**265**	270		V_{RMS}
Input overvoltage turn-off	$V_{IN\text{-}ULVO+}$			273	**287**	V_{RMS}
Output overvoltage threshold	$V_{OUT\text{-}ULVO+}$	Instantaneous, latched shutdown	**29**	30.5	**32**	V
Upper start / restart temperature threshold (case)	$T_{CASE\text{-}OTP-}$		**100**			°C
Overtemperature shutdown threshold (junction)	$T_{J\text{-}OTP+}$			125		°C
Overtemperature shutdown threshold (case)	$T_{CASE\text{-}OTP+}$			**110**		°C
Overcurrent blanking time	T_{OC}	Based on line frequency	**400**	460	**550**	ms
Input overvoltage response time	T_{POVP}			40		ms
Input undervoltage response time	T_{UVLO}	Based on line frequency		200		ms
Output overvoltage response time	T_{SOVP}	Powertrain on		30		ms
Short circuit response time	T_{SC}	Powertrain on, operational state		270		µs
Fault retry delay time	T_{OFF}	See Timing Diagram		10		s
Output power limit	P_{PROT}	50% overload for 20 ms typ allowed	**400**			W

Timing diagram



Timing diagram (Cont.)



Application Characteristics

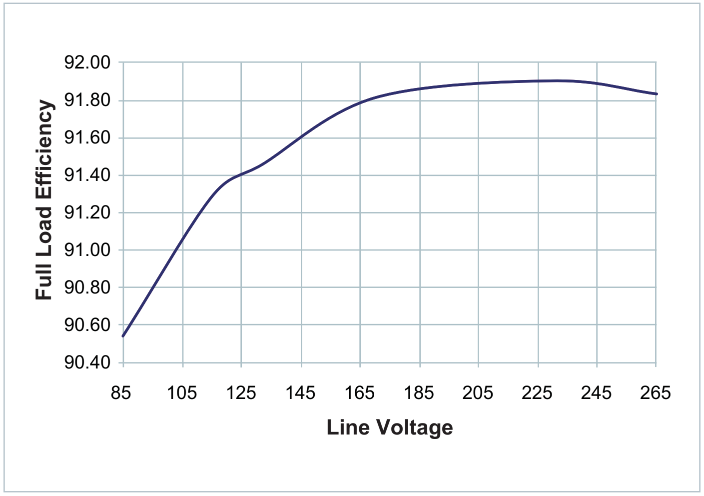


Figure 1 — *Full load efficiency vs. line voltage*

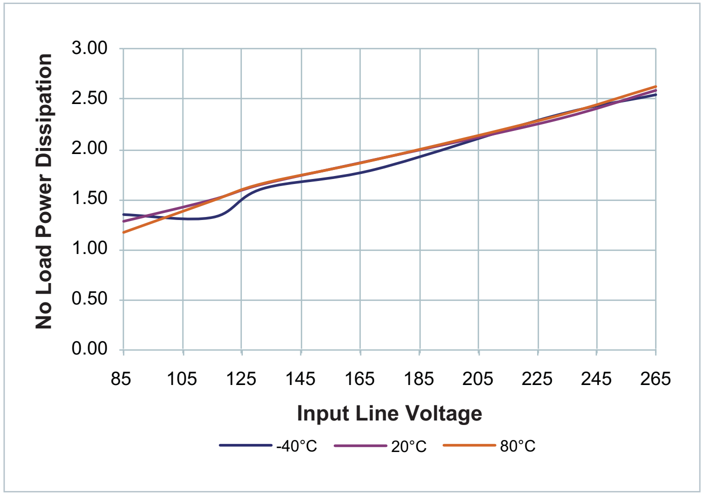


Figure 2 — *Typical no load power dissipation vs. V_{IN}, module enabled*

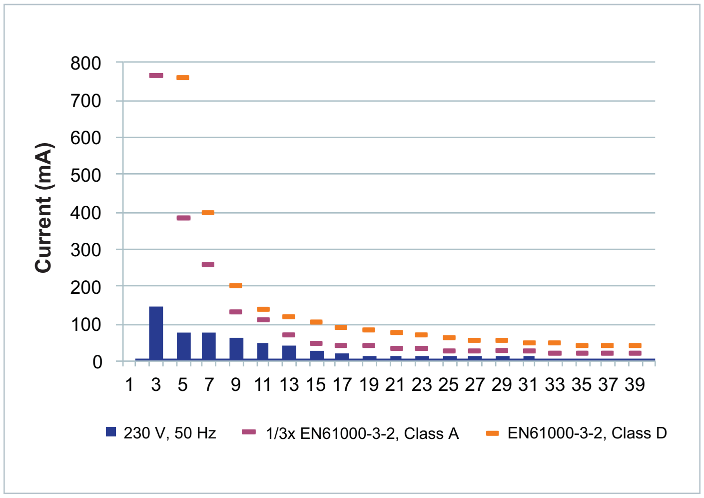


Figure 3 — *Typical input current harmonics, full load vs. V_{IN} using typical applications circuit on pages 2 & 3*

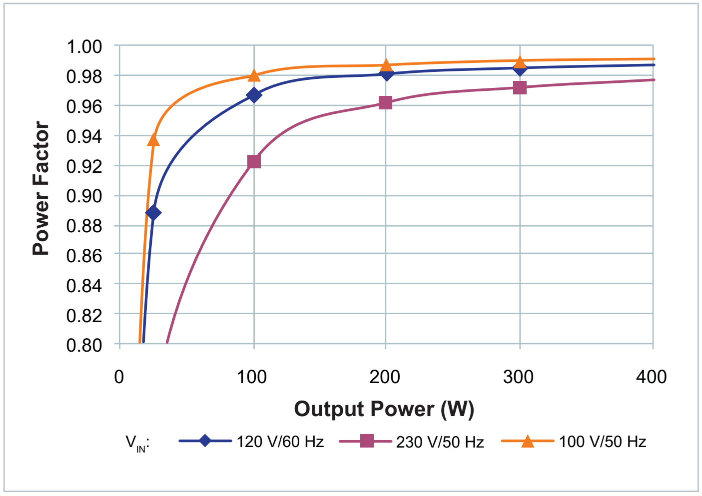


Figure 4 — *Typical power factor vs. V_{IN} and I_{OUT} using typical applications circuit on pages 2 & 3*

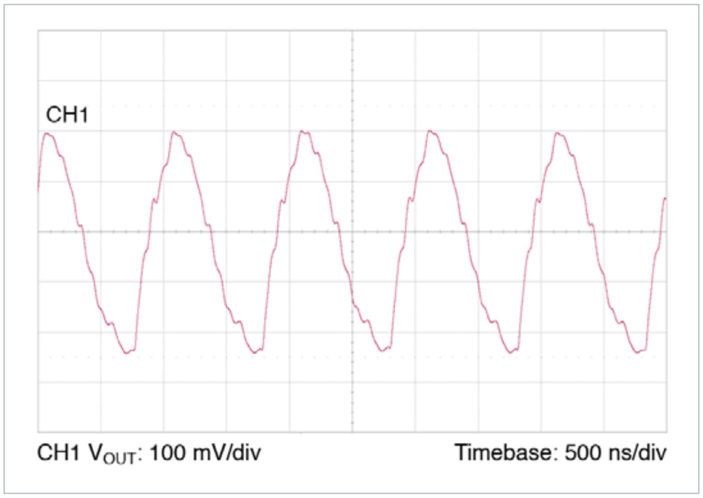


Figure 5 — *Typical switching frequency output voltage ripple waveform, $T_{CASE} = 30°C$, $V_{IN} = 230$ V, $I_{OUT} = 16.7$ A, no external ceramic capacitance, 20 MHZ BW*

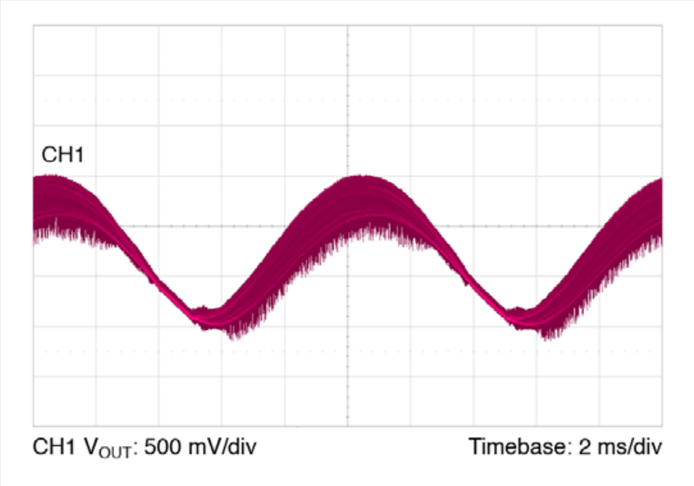


Figure 6 — *Typical line frequency output voltage ripple waveform, $T_{CASE} = 30°C$, $V_{IN} = 230$ V, $I_{OUT} = 16.7$ A, $C_{OUT} = 44{,}000$ µF. 20 MHZ BW*

Application Characteristics (Cont.)

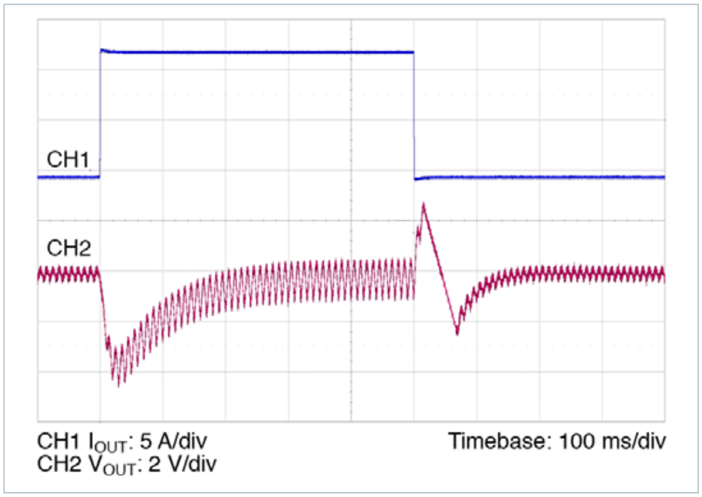


Figure 7 — *Typical output voltage transient response, T_{CASE} = 30°C, V_{IN} = 230 V, I_{OUT} = 16.7 A, 4.2 A C_{OUT} = 44,000 µF*

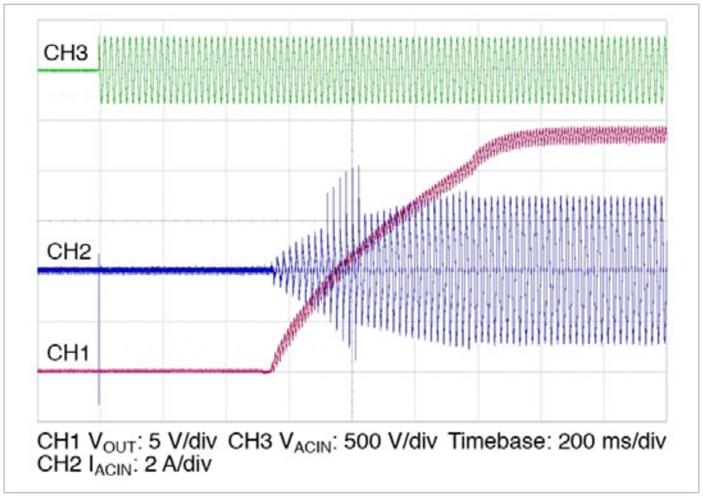


Figure 8 — *Typical startup waveform, application of V_{IN}, R_{LOAD} = 1.4 Ω, C_{OUT} = 44,000 µF*

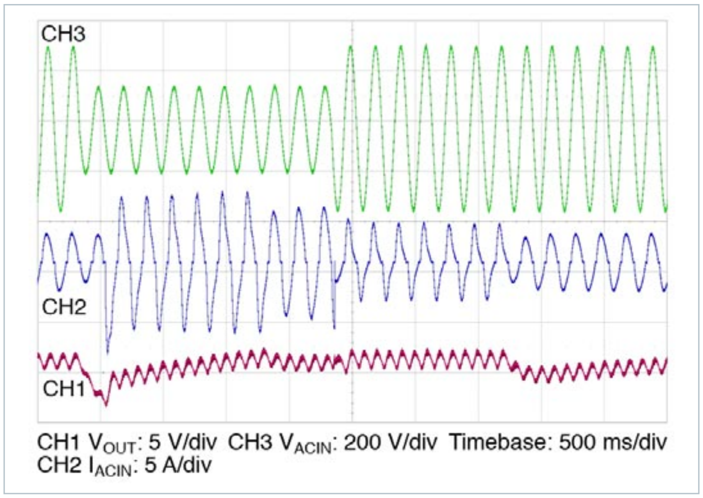


Figure 9 — *230 V, 120 V range change transient response 16.7 A, I_{OUT} = 16.7 A, C_{OUT} = 44,000 µF*

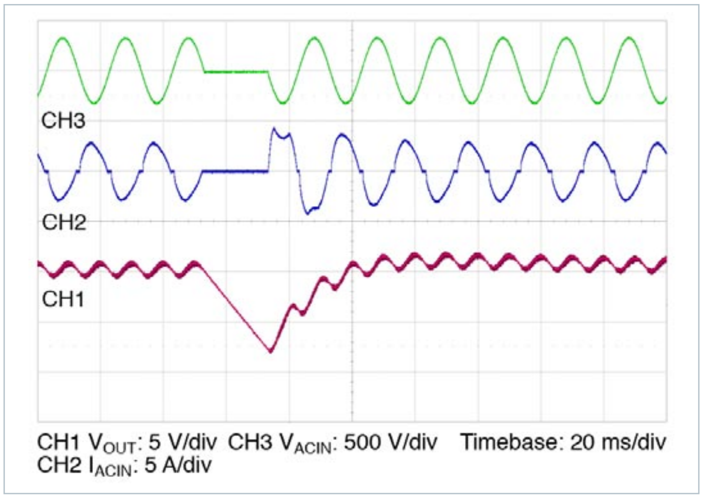


Figure 10 — *Line drop out, 230 V 50 Hz, 0° phase, I_{OUT} = 16.7 A, C_{OUT} = 44,000 µF*

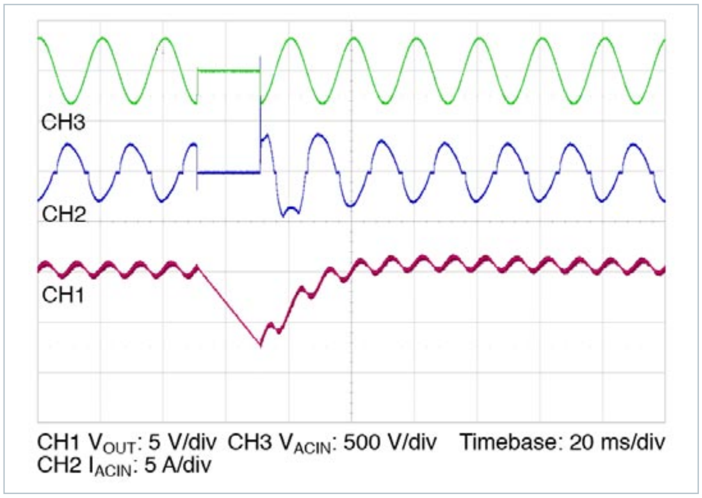


Figure 11 — *Line drop out, 230 V50 Hz, 90° phase, V_{IN} = 230 V, I_{OUT} = 16.7 A, C_{OUT} = 44,000 µF*

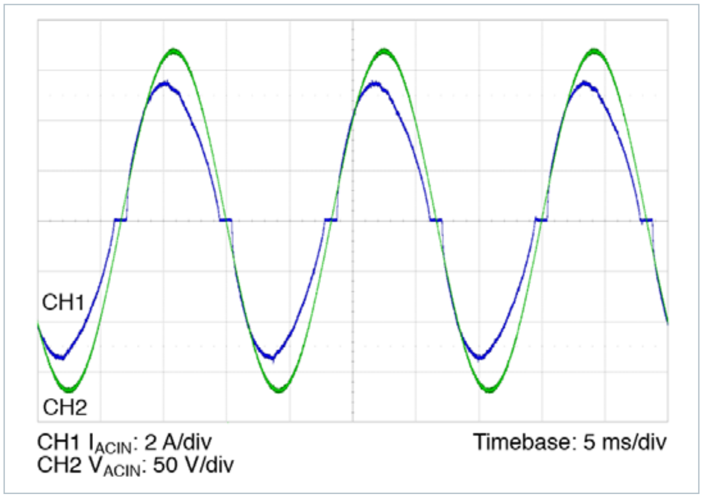


Figure 12 — *Typical line current waveform, 60 Hz, V_{IN} = 120 V, 60 HZ I_{OUT} = 16.7 A, C_{OUT} = 44,000 µF*

Application Characteristics (Cont.)

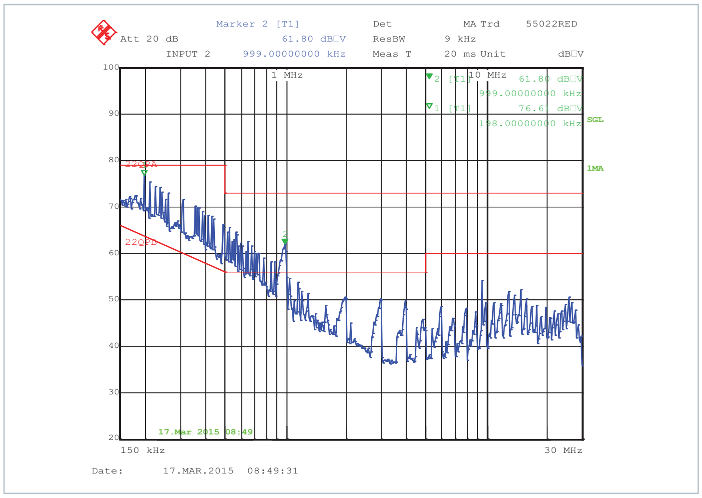


Figure 13 — Typical EMI Spectrum, Peak Scan, 90% load, 115 V_{IN}, C_{OUT} = 44,000 µF, No Inlet Filter, C4

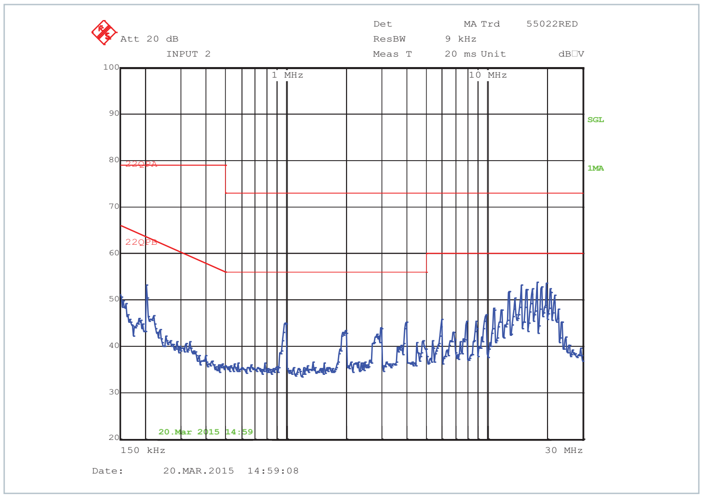


Figure 14 — Typical EMI Spectrum, Peak Scan, 90% load, 115 V_{IN}, C_{OUT} = 44,000 µF using Typical Chassis Mount Application Circuit

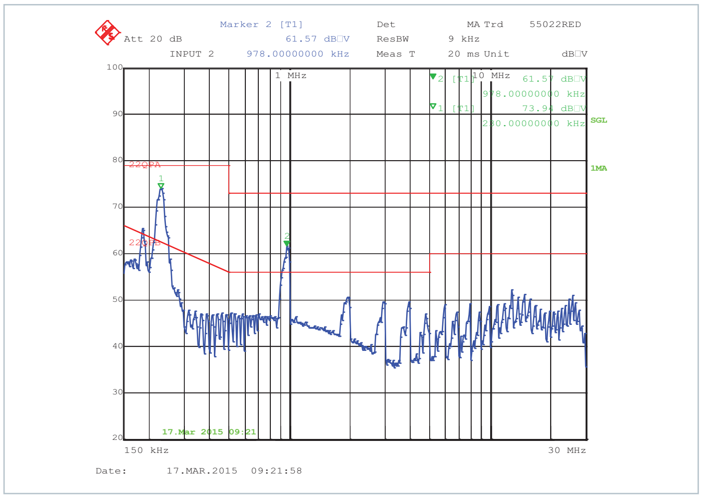


Figure 15 — Typical EMI Spectrum, Peak Scan, 90% load, 230 V_{IN}, C_{OUT} = 44,000 µF, No Inlet Filter, C4

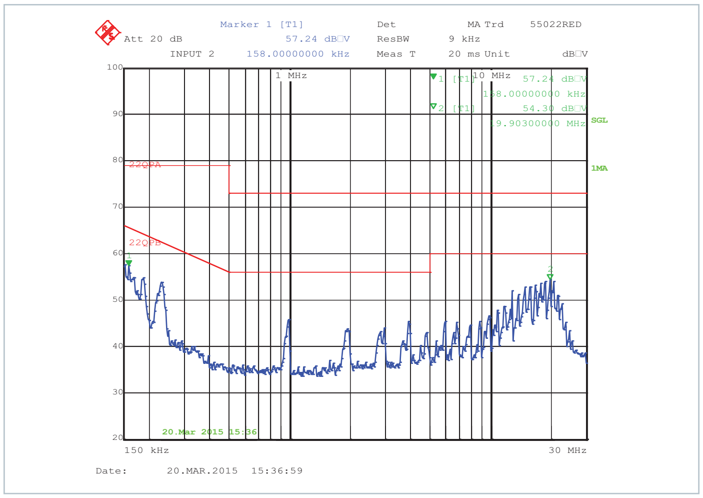


Figure 16 — Typical EMI Spectrum, Peak Scan, 90% load, 230 V_{IN}, C_{OUT} = 44,000 µF using Typical Chassis Mount Application Circuit

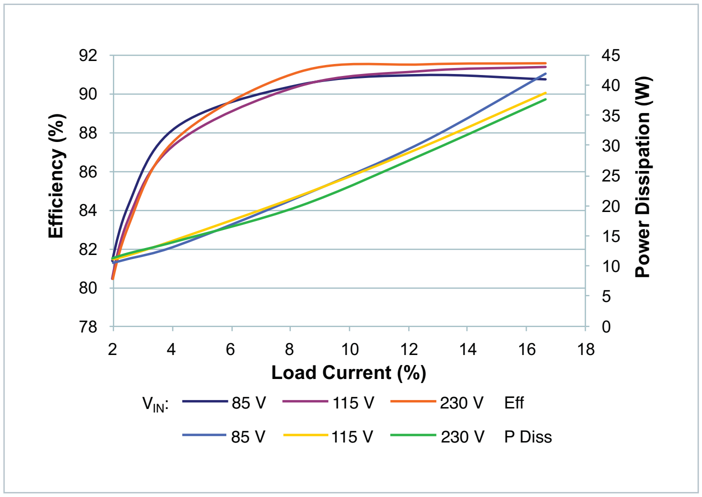


Figure 17 — V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = -40°C

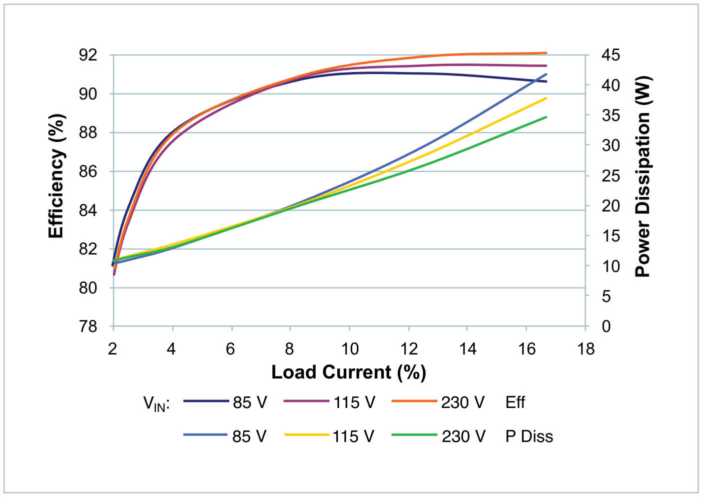


Figure 18 — V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 20°C

Application Characteristics (Cont.)

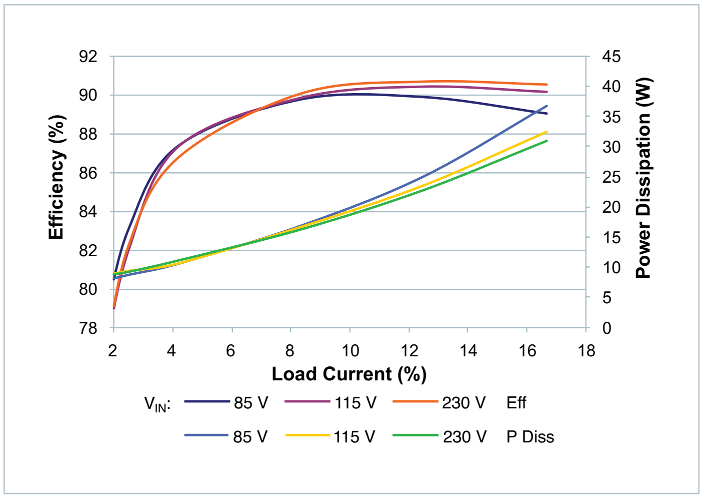


Figure 19 — *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 80°C*

General Characteristics

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, TC = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L			124.8 / [4.91]		mm / [in]
Width	W			35.5 / [1.40]		mm / [in]
Height	H			9.3 / [0.37]		mm / [in]
Volume	Vol	Without heatsink		42.0 / [2.56]		cm^3/ [in^3]
Weight	W			156 / [5.5]		g / [oz]
Pin material		C10200 copper, full hard				µin
Underplate		Nickel	100		150	
Pin finish		Pure matte tin, whisker resistant chemistry	200		300	
Thermal						
Operating case temperature	T_C	C - Grade, see derating curve in SOA	-20		100	°C
		T - Grade, see derating curve in SOA	-40		100	°C
Thermal resistance, junction to case, top	R_{JC_TOP}			1.04		°C/W
Thermal resistance, junction to case, bottom	R_{JC_BOT}			1.83		°C/W
Coupling thermal resistance, top to bottom of case, internal	R_{HOU}			0.15		°C/W
Shell Thermal capacity				32		J/K
Thermal design		See Thermal Design on Page 17				
Assembly						
ESD rating	ESD_{HBM}	Human Body Model, "JEDEC JESD 22-A114C.01"	1,000			V
	ESD_{MM}	Machine Model, "JEDEC JESD 22-A115B"	N/A			
	ESD_{CDM}	Charged Device Model, "JEDEC JESD 22-C101D"	200			
Safety						
Agency approvals/standards		cTÜVus (EN60950-1)				
		cURus (UL/CSA 60950-1)				
		CE, Low Voltage Directive 2006/95/EC				
		Touch Current measured in accordance with IEC 60990 using measuring network Figure 3 (VIA PFM only)		0.5		mA
Pending EMI/EMC Compliance						
FCC Part 15, EN55022, CISPR22: 2006 + A1: 2007, Conducted Emissions		Class B Limits - with –OUT connected to GND				
EN61000-3-2: 2009, Harmonic Current Emissions		Class A				

General Characteristics (Cont.)

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, TC = 25°C, unless otherwise noted.

Boldface specifications apply over the temperature range of the specified Product Grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Pending EMI/EMC Compliance (cont.)						
EN61000-3-3: 2005, Voltage Changes & Flicker		P_{ST} <1.0; P_{LT} <0.65; dc <3.3% dmax <6%				
EN61000-4-4: 2004, Electrical Fast Transients		Level 2, Performance Criteria A				
EN61000-4-5: 2006, Surge Immunity		Level 3, Immunity Criteria A, external TMOV required				
EN61000-4-6: 2009, Conducted RF Immunity		Level 2, 130 dBμV (3.0 V_{RMS})				
EN61000-4-8: 1993 + A1 2001, Power Frequency H-Field 10A/m, continuous field		Level 3, Performance Criteria A				
EN61000-4-11: 2004, Voltage Dips & Interrupts		Class 2, Performance Criteria A Dips, Performance Criteria B Interrupts				

Product Details and Design Guidelines

Building Blocks and System Designs

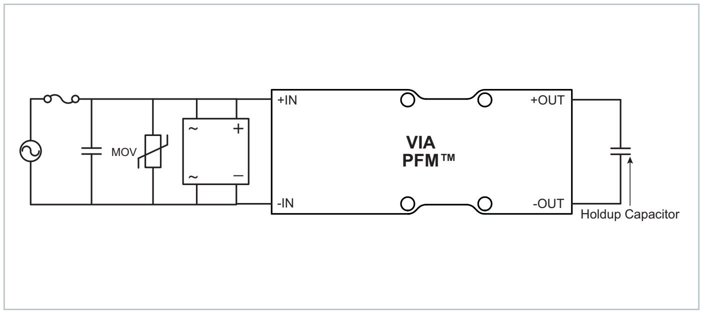


Figure 21 – *400 W Universal AC-to-DC Supply*

The VIA PFM is a high efficiency AC-to-DC converter, operating from a universal AC input to generate an isolated SELV24 VDC output bus with power factor correction. It is the key component of an AC-to-DC power supply system such as the one shown in Figure 21 above.

The input to the VIA PFM is a rectified sinusoidal AC source with a power factor maintained by the module with harmonics conforming to IEC 61000-3-2. Internal filtering enables compliance with the standards relevant to the application (Surge, EMI, etc.). See EMI/EMC Compliance standards on Page 13.

The module uses secondary-side energy storage (at the SELV 24 V bus) to maintain output hold up through line dropouts and brownouts. Downstream regulators also provide tighter voltage regulation, if required.

Traditional PFC Topology

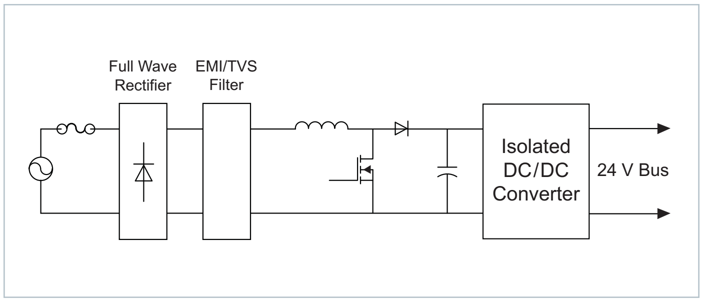


Figure 22 – *Traditional PFC AC-to-DC supply*

To cope with input voltages across worldwide AC mains (85 – 264 Vac), traditional AC-DC power supplies (Figure 22) use two power conversion stages: 1) a PFC boost stage to step up from a rectified input as low as 85 Vac to ~380 Vdc; and 2) a DC-DC down converter from 380 Vdc to a 24 V bus.

The efficiency of the boost stage and of traditional power supplies is significantly compromised operating from worldwide AC lines as low as 85 Vac.

Adaptive Cell™ Topology

With its single stage Adaptive Cell™ topology, the VIA PFM enables consistently high efficiency conversion from worldwide AC mains to a 24 V bus and efficient secondary-side power distribution.

Input Fuse Selection

VI Brick products are not internally fused in order to provide flexibility in configuring power systems. Input line fusing is recommended at system level, in order to provide thermal protection in case of catastrophic failure. The fuse shall be selected by closely matching system requirements with the following characteristics:

- Recommended fuse: 8 A, 216 Series Littelfuse or lower current rating (usually greater than the VIA PFM maximum current at lowest input voltage)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Breaking capacity per application requirements
- Nominal melting I^2t

Fault Handling

Input Undervoltage (UV) Fault Protection

The input voltage is monitored by the micro-controller to detect an input under voltage condition. When the input voltage is less than the $V_{IN\text{-}UVLO\text{-}}$, a fault is detected, the fault latch and reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the unit falls. After a time t_{UVLO}, the unit shuts down. Faults lasting less than t_{UVLO} may not be detected. Such a fault does not go through an auto-restart cycle. Once the input voltage rises above $V_{IN\text{-}UVLO+}$, the unit recovers from the input UV fault, the powertrain resumes normal switching after a time t_{ON} and the output voltage of the unit reaches the set-point voltage within a time t_{SS}.

Overcurrent (OC) Fault Protection

The unit's output current, determined by V_{EAO}, V_{IN_B} and the primary-side sensed output voltage is monitored by the microcontroller to detect an output OC condition. If the output current exceeds its current limit, a fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the module falls after a time t_{OC}. As long as the fault persists, the module goes through an auto-restart cycle with off time equal to $t_{OFF} + t_{ON}$ and on time equal to t_{OC}. Faults shorter than a time t_{OC} may not be detected. Once the fault is cleared, the module follows its normal start up sequence after a time t_{OFF}.

Short Circuit (SC) Fault Protection

The microcontroller determines a short circuit on the output of the unit by measuring its primary sensed output voltage and EAO. Most commonly, a drop in the primary-sensed output voltage triggers a short circuit event. The module responds to a short circuit event within a time t_{SC}. The module then goes through an auto restart cycle, with an off time equal to $t_{OFF} + t_{ON}$ and an on time equal to t_{SC}, for as long as the short circuit fault condition persists. Once the fault is cleared, the unit follows its normal start up sequence after a time t_{OFF}. Faults shorter than a time t_{SC} may not be detected.

Temperature Fault Protection

The microcontroller monitors the temperature within the VIA PFM. If this temperature exceeds $T_{J\text{-}OTP+}$, an overtemperature fault is detected, the reset logic block disables the modulator, the modulator stops the powertrain switching and the output voltage of the VIA PFM falls. Once the case temperature falls below $T_{CASE\text{-}OTP-}$, after a time greater than or equal to t_{OFF}, the converter recovers and undergoes a normal restart. For the C-grade version of the converter, this temperature is 75°C. Faults shorter than a time t_{OTP} may not be detected. If the temperature falls below $T_{CASE\text{-}UTP-}$, an undertemperature fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching and the output voltage of the unit falls. Once the case temperature rises above $T_{CASE\text{-}UTP}$, after a time greater than or equal to t_{OFF}, the unit recovers and undergoes a normal restart.

Output Overvoltage Protection (OVP)

The microcontroller monitors the primary sensed output voltage to detect output OVP. If the primary sensed output voltage exceeds $V_{OUT\text{-}OVLO+}$, a fault is latched, the logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the module falls after a time t_{SOVP}. Faults shorter than a time t_{SOVP} may not be detected. This type of fault is a latched fault and requires that 1) the EN pin be toggled or 2) the input power be recycled to recover from the fault.

Hold-up Capacitance

The VI Brick AC Front End uses secondary-side energy storage (at the SELV 24 V bus) and optional PRM® regulators to maintain output hold up through line dropouts and brownouts. The module's output bulk capacitance can be sized to achieve the required hold up functionality.

Hold-up time depends upon the output power drawn from the VI Brick AC Front End based AC-to-DC front end and the input voltage range of downstream DC-to-DC converters.

The following formula can be used to calculate hold-up capacitance for a system comprised of VI Brick AC Front End and a downstream regulator:

Output Filtering

$$C = 2*P_{OUT}*(0.005+t_d)/(V_2^{\,2} - V_1^{\,2})$$

where:

C	*VIA PFM's output bulk capacitance in farads*
t_d	*Hold-up time in seconds*
P_{OUT}	*VIA PFM's output power in watts*
V_2	*Output voltage of VIA PFM's converter in volts*
V_1	*Downstream regulator undervoltage turn off (volts)* *–OR–* $P_{OUT}/I_{OUT\text{-}PK}$*, whichever is greater.*

The VIA PFM requires an output bulk capacitor in the range of 27,000 µF to 60,000 µF for proper operation of the PFC front-end. A minimum 40,000 µF is recommended for full rated output. Capacitance can be reduced proportionally for lower maximum loads.

The output voltage has the following two components of voltage ripple:

1) Line frequency voltage ripple: $2*f_{LINE}$ Hz component

2) Switching frequency voltage ripple: 1 MHz module switching frequency component (see Figure 5).

Line Frequency Filtering

Output line frequency ripple depends upon output bulk capacitance. Output bulk capacitor values should be calculated based on line frequency voltage ripple. High-grade electrolytic capacitors with adequate ripple current ratings, low ESR and a minimum voltage rating of 35 V are recommended.

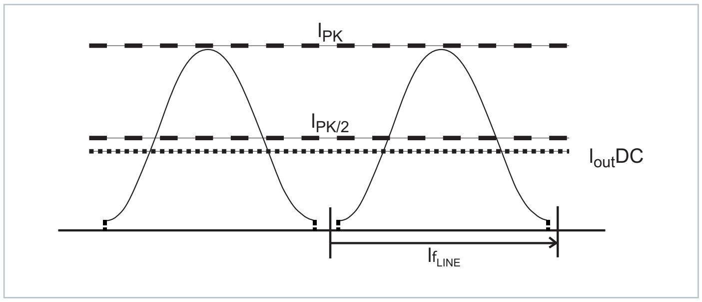


***Figure 23** – Output current waveform*

Based on the output current waveform, as seen in Figure 23, the following formula can be used to determine peak-to-peak line frequency output voltage ripple:

$$V_{PP}l \cong 0.2 * P_{OUT}/(V_{OUT} * f_{LINE} * C)$$

where:

$V_{PP}l$	*Output voltage ripple Peak-to-peak line frequency*
P_{OUT}	*Average output power*
V_{OUT}	*Output voltage set point, nominally 24 V*
f_{LINE}	*Frequency of line voltage*
C	*Output bulk capacitance*
I_{DC}	*Maximum average output current*
I_{PK}	*Peak-to-peak line frequency output current ripple*

In certain applications, the choice of bulk capacitance may be determined by hold-up requirements and low frequency output voltage filtering requirements. Such applications may use the greater capacitance value determined from these requirements. The ripple current rating for the bulk capacitors can be determined from the following equation:

$$I_{ripple} \cong 0.8 * P_{OUT}/V_{OUT}$$

Switching Frequency Filtering

This is included within the VIA PFM. No external filtering is necessary for most applications. For the most noise sensitive applications, a common mode choke followed by two caps to PE GND will reduce switching noise further.

EMI Filtering and Transient Voltage Suppression

EMI Filtering

The VI Brick AC® Front End with PFC is designed such that it will comply with EN55022 Class B for Conducted Emissions with a commercially available off-the-shelf EM filter. The emissions spectrum is shown in Figures 13 - 16. If one of the outputs is connected to earth ground, a small output common mode choke is also recommended.

EMI performance is subject to a wide variety of external influences such as PCB construction, circuit layout etc. As such, external components in addition to those listed herein may be required in specific instances to gain full compliance to the standards specified.

Transient Voltage Suppression

The VIA PFM contains line transient suppression circuitry to meet specifications for surge (i.e. EN61000-4-5) and fast transient conditions (i.e. EN61000-4-4 fast transient/"burst").

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the top surface, the bottom surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a VIA, as can be seen from specified thermal operating area on Page 4. Since the VIA has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. To this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 24 shows the "thermal circuit" for the VIA module.

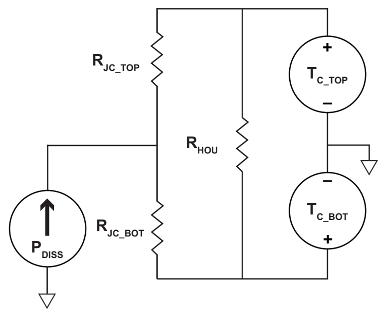


Figure 24 – *Double sided cooling VIA thermal model*

In this case, the internal power dissipation is P_{DISS}, R_{JC_TOP} and R_{JC_BOT} are thermal resistance characteristics of the VIA module and the top and bottom surface temperatures are represented as T_{C_TOP}, and T_{C_BOT}. It interesting to notice that the package itself provides a high degree of thermal coupling between the top and bottom case surfaces (represented in the model by the resistor R_{HOU}). This feature enables two main options regarding thermal designs:

- Single side cooling: the model of Figure 1 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for bottom side cooling only is shown in Figure 25.

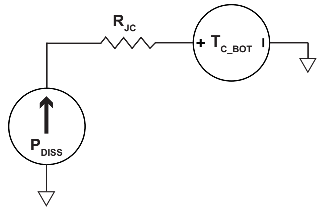


Figure 25 – *Single-sided cooling VIA thermal model*

In this case, RJC can be derived as following:

$$R_{JC} = \frac{(R_{JC\_TOP} + R_{HOU}) \bullet R_{JC\_BOT}}{R_{JC\_TOP} + R_{HOU} + R_{JC\_BOT}}$$

- Double side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, like for example heatsinks with independent airflows or a combination of chassis/air cooling.

Powering a Constant Power Load

When the output voltage of the VIA PFM module is applied to the input of the downstream regulator, the regulator turns on and acts as a constant-power load. When the module's output voltage reaches the input undervoltage turn on of the regulator, the regulator will attempt to start. However, the current demand of the downstream regulator at the undervoltage turn-on point and the hold-up capacitor charging current may force the VIA PFM into current limit. In this case, the unit may shut down and restart repeatedly. In order to prevent this multiple restart scenario, it is necessary to delay enabling a constant-power load when powered up by the upstream VIA PFM until after the output set point of the VIA PFM is reached.

This can be achieved by

1. keeping the downs- sequence

   and

2. turning the downstream constant-power load on after the output voltage of the module reaches 24 V steady state

After the initial startup, the output of the VIA PFM can be allowed to fall to 15 V during a line dropout at full load. In this case, the circuit should not disable the downstream regulator if the input voltage falls after it is turned on; therefore, some form of hysteresis or latching is needed on the enable signal for the constant power load. The output capacitance of the VIA PFM should also be sized appropriately for a constant power load to prevent collapse of the output voltage of the module during line dropout (see Hold up Capacitance on Page 16). A constant-power load can be turned off after completion of the required hold up time during the power-down sequence or can be allowed to turn off when it reaches its own undervoltage shutdown point.

The timing diagram in Figure 26 shows the output voltage of the VIA PFM and the downstream regulator's enable pin voltage and output voltage of the PRM regulator for the power up and power down sequence. It is recommended to keep the time delay approximately 10 to 20 ms.

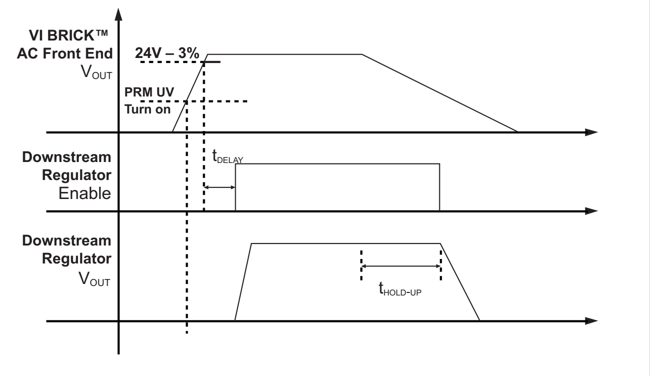


***Figure 26** – PRM Enable Hold off Waveforms*

Special care should be taken when enabling the constant-power load near the auto-ranger threshold, especially with an inductive source upstream of the VIA PFM. A load current spike may cause a large input voltage transient, resulting in a range change which could temporarily reduce the available power (see Adaptive Cell™ Topology below).

Adaptive Cell™ Topology

The Adaptive Cell topology utilizes magnetically coupled "top" and "bottom" primary cells that are adaptively configured in series or parallel by a configuration controller comprised of an array of switches. A microcontroller monitors operating conditions and defines the configuration of the top and bottom cells through a range control signal.

A comparator inside the microcontroller monitors the line voltage and compares it to an internal voltage reference.

If the input voltage of the VI Brick AC Front End crosses above the positive going cell reconfiguration threshold voltage, the top cell and bottom cell configure in series and the unit operates in "high" range.

If the peak of input voltage of the unit falls below the negative-going range threshold voltage for two line cycles, the cell configuration controller configures the top cell and bottom cell in parallel, the unit operates in "low" range.

Power processing is held off while transitioning between ranges and the output voltage of the unit may temporarily droop. External output hold up capacitance should be sized to support power delivery to the load during cell reconfiguration. The minimum specified external output capacitance is sufficient to provide adequate ride-through during cell reconfiguration for typical applications. Waveforms showing active cell reconfiguration can be seen in Figure 9.

Dielectric Withstand

The chassis of the VIA PFM is required to be connected to Protective Earth when installed in the end application and must satisfy the requirements of IEC 60950-1 for Class I products.

The VIA PFM contains an internal safety approved isolating component (VI ChiP) that provides the Reinforced Insulation from Input to Output. The isolating component is individually tested for Reinforced Insulation from Input to Output at 3000 Vac or 4242 Vdc prior to the final assembly of the VIA.

When the VIA assembly is complete the Reinforced Insulation can only be tested at Basic Insulation values as specified in the electric strength Test Procedure noted in clause 5.2.2 of IEC 60950-1.

Test Procedure Note from IEC 60950-1

"For equipment incorporating both REINFORCED INSULATION and lower grades of insulation, care is taken that the voltage applied to the REINFORCED INSULATION does not overstress BASIC INSULATION or SUPPLEMENTARY INSULATION."

Summary

The final VIA assembly contains basic insulation from input to case, reinforced insulation from input to output, and functional insulation from output to case.

The output of the VIA complies with the requirements of SELV circuits so only functional insulation is required from the output (SELV) to case (PE) because the case is required to be connected to protective earth in the final installation. The construction of the VIA can be summarized by describing it as a "Class II" component installed in a "Class I" subassembly. The reinforced insulation from input to output can only be tested at basic insulation values on the completely assembled VIA product.

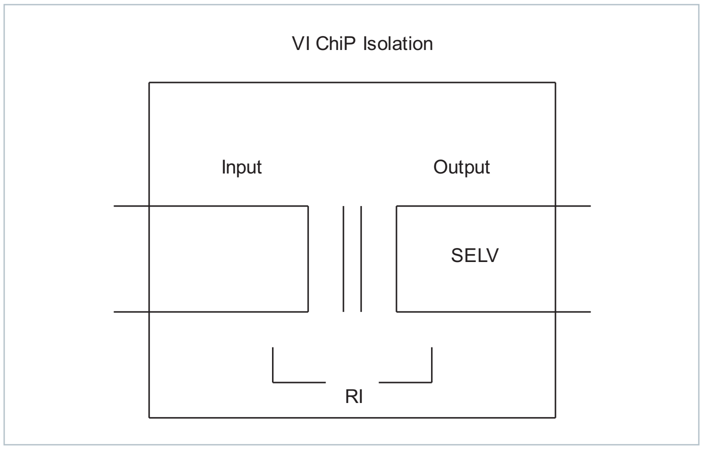


***Figure 27** – VI Chip before final assembly in the VIA*

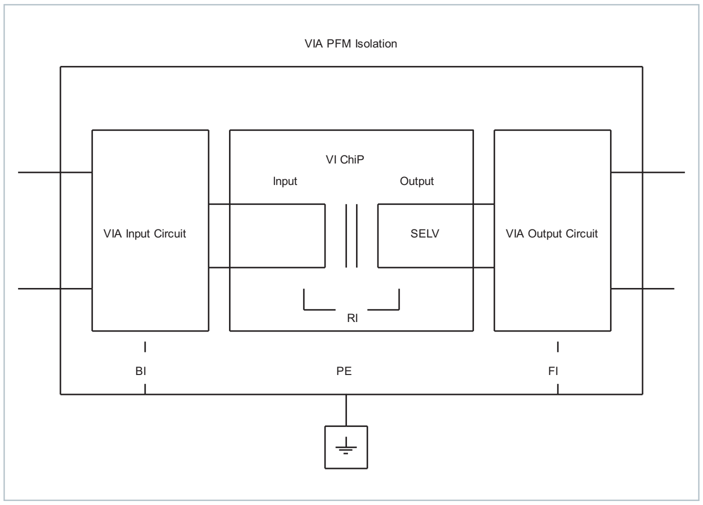
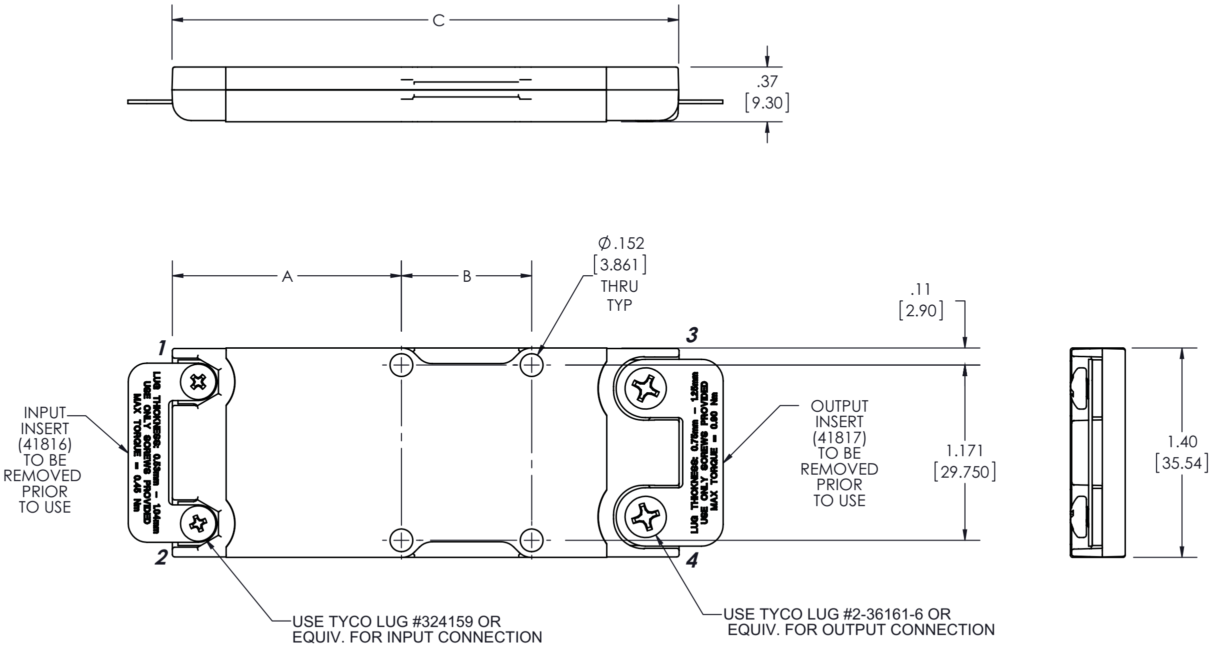
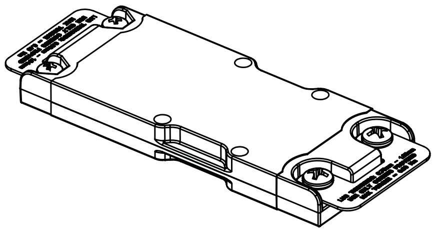


***Figure 28** – PFM VIA after final assembly*

VIA PFM Chassis Mount Package Mechanical Drawing





NOTES:

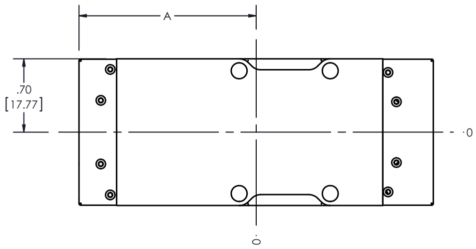
1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.

2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.

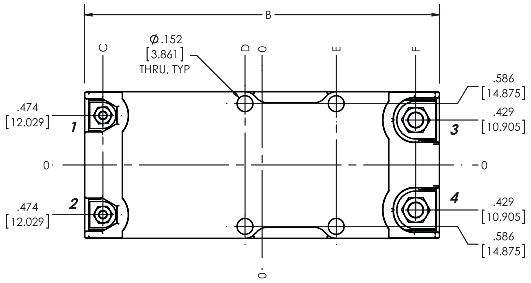
PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'
125 mm VIA PFM	2.17 [55.15]	1.757 [44.625]	4.91 [124.77]

Product outline drawing; Product outline drawings are available in .pdf and .dxf formats.
3D mechanical models are available in .pdf and .step formats.
See www.vicorpower.com/ac-dc-converters-board-mount/ac-front-end-module for more details.

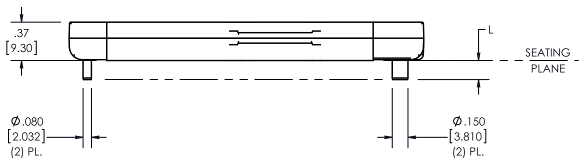
VIA PFM PCB Mount Package Mechanical Drawing and Recommended Land Pattern

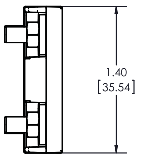


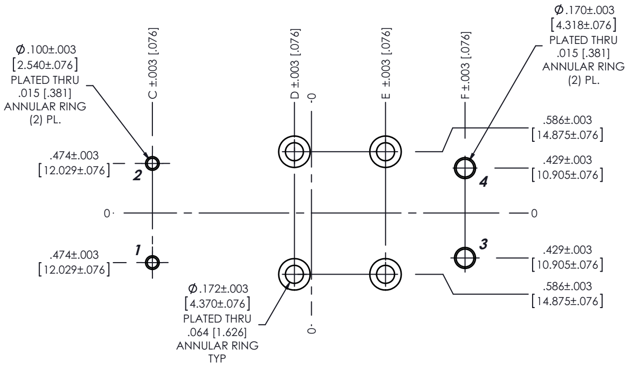
TOP VIEW
(COMPONENT SIDE)



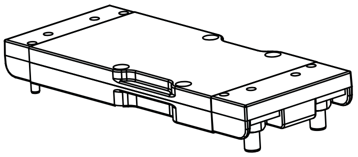
BOTTOM VIEW







RECOMMENDED HOLE PATTERN
(COMPONENT SIDE)



NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.

PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'E'	DIM 'F'	DIM 'L'	
125 mm VIA PFM	2.18 [55.27]	4.35 [110.55]	2.004 [50.903]	.565 [14.350]	1.192 [30.275]	1.953 [49.614]	LONG	.103 [2.607]
							EXTRA LONG	.182 [4.614]

Revision History

Revision	Date	Description	Page Number(s)
1.0	04/01/15	Intital release	n/a

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