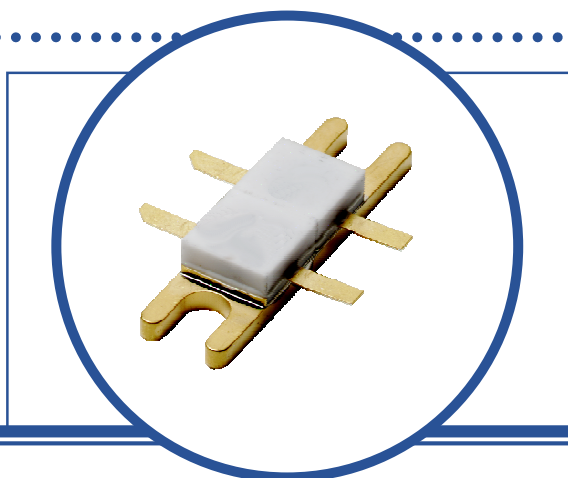


D1008UK  
GOLD METALLISED  
MULTI-PURPOSE SILICON  
DMOS RF FET  
80W—28V—500MHZ  
PUSH-PULL



FEATURES:

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW  $C_{RSS}$
- SIMPLE BIAS CIRCUIT
- LOW NOISE
- HIGH GAIN — 13dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS from 1MHz to 500MHz

**ABSOLUTE MAXIMUM RATINGS** ( $T_{CASE} = 25^{\circ}C$  unless otherwise stated)

$P_D$	Power Dissipation	175W
$BV_{DSS}$	Drain – Source Breakdown Voltage	70V
$BV_{GSS}$	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(SAT)}$	Drain Current (Per Side)	10A
$T_{stg}$	Storage Temperature Range	-65 to +150°C
$T_J$	Maximum Operating Junction Temperature	200°C

Semelab Limited reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

TETRA FET

**D1008UK**

ROHS COMPLIANT METAL GATE RF SILICON FET

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$  unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ.	Max.	Units
<b>PER SIDE</b>						
$BV_{DSS}$	Drain – Source Breakdown Voltage	$V_{GS} = 0V$ $I_D = 100mA$	70			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 28V$ $V_{GS} = 0V$			2	mA
$I_{GSS}$	Gate Leakage Current	$V_{GS} = 20V$ $V_{DS} = 0V$			1	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage *	$I_D = 10mA$ $V_{DS} = V_{GS}$	1		7	V
$g_{fs}$	Forward Transconductance*	$V_{DS} = 10V$ $I_D = 2A$	1.6			S

\* Pulse Width  $\leq 380\mu s$ ,  $\delta \leq 2\%$ **DYNAMIC CHARACTERISTICS**

Symbols	Parameters	Test Conditions	Min.	Typ.	Max.	Units
<b>Per Side</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 28V$ $V_{GS} = -5V$ $f = 1.0MHz$			120	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 28V$ $V_{GS} = 0V$ $f = 1.0MHz$			60	
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = 28V$ $V_{GS} = 0V$ $f = 1.0MHz$			5	
<b>Total Device</b>						
$G_{ps}$	Common Source Power Gain	$P_o = 80W$ $V_{DS} = 28$	13			dB
$\eta$	Drain Efficiency	$I_{DQ} = 0.4A$ $f = 400MHz$	50			%
VSWR	Load Mismatch Tolerance		20:1			

**HAZARDOUS MATERIAL WARNING**

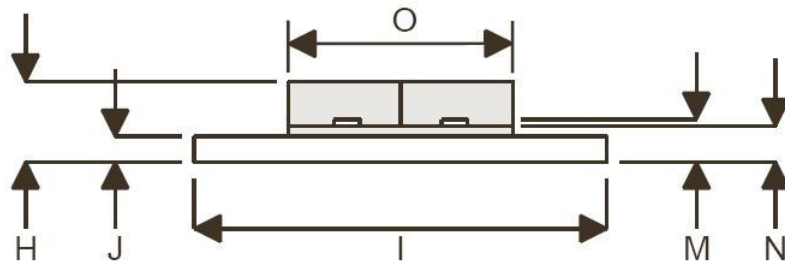
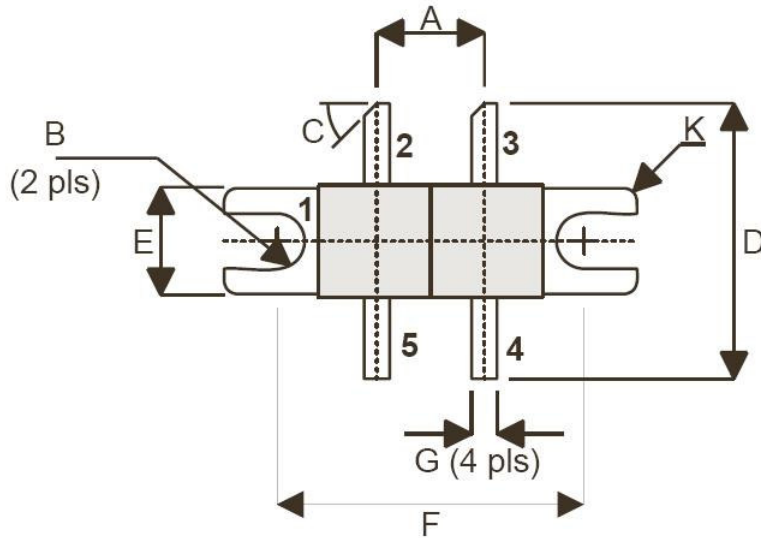
The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

**THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE**

**Thermal Properties**

Symbols	Parameters	Max.	Units
$R_{THj-case}$	Thermal Resistance, Junction To Case	1.0	$^{\circ}C/W$

## MECHANICAL DATA



DIM	mm	Tol.	Inches	Tol.
A	6.45	0.13	0.254	0.005
B	1.65R	0.13	0.065R	0.005
C	45°	5°	45°	5°
D	16.51	0.76	0.650	0.03
E	6.47	0.13	0.255	0.005
F	18.41	0.13	0.725	0.005
G	1.52	0.13	0.060	0.005
H	4.82	0.25	0.190	0.010
I	24.76	0.13	0.975	0.005
J	1.52	0.13	0.060	0.005
K	0.81R	0.13	0.032R	0.005
M	0.13	0.02	0.005	0.001
N	2.16	0.13	0.085	0.005

### DK METAL PACKAGE

Pin 1 – Source (Common)

Pin 2 – Drain1

Pin 3 – Drain2

Pin 4 – Gate 2

Pin 5 – Gate 1

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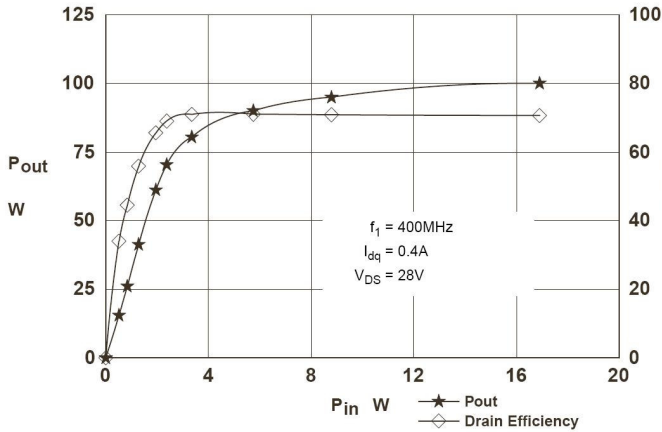


Figure 01— Power Output and Efficiency vs. Power Input.

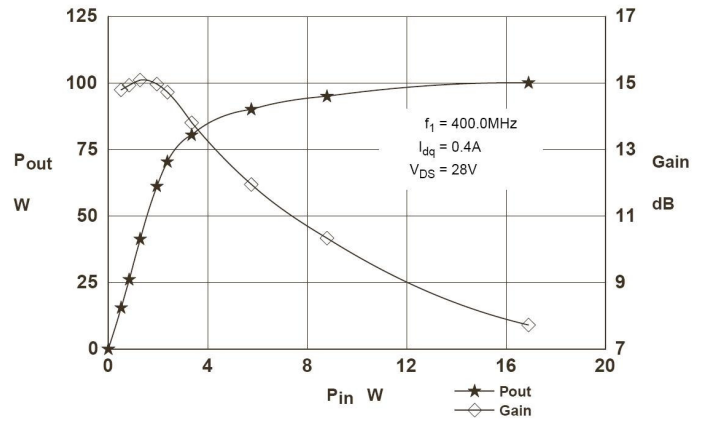


Figure 02— Power Output and Gain vs. Power Input.

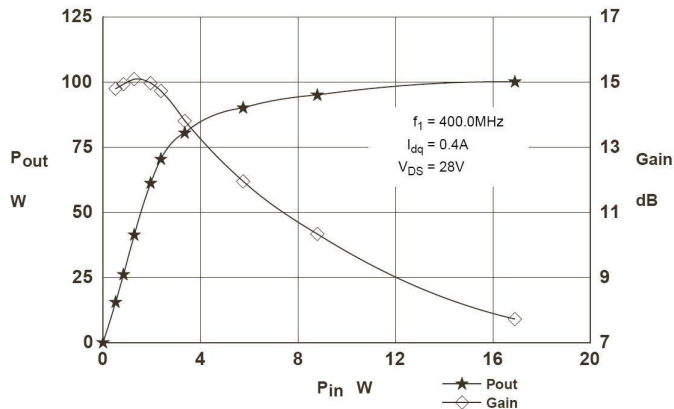


Figure 03— IMD vs. Output Power.

## D1008UK OPTIMUM SOURCE AND LOAD IMPEDANCE

FREQUENCY MHZ	$Z_S$ $\Omega$	$Z_L$ $\Omega$
400	1.5 + j0.2	5.0 + j2.0

## Typical S Parameters

Vds = 28V, Id=1A  
MHz S MA R 50

IFreq MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
100	0.794	-158	14.622	69	0.0115	-7	0.61	-145
200	0.881	-167	5.821	42	0.0061	3	0.794	-156
300	0.923	-171	3.02	28	0.0068	60	0.871	-162
400	0.923	-176	1.82	18	0.117	77	0.902	-167
500	0.937	-179	1.439	15	0.0168	76	0.923	-169
600	0.952	177	1.057	13	0.0234	75	0.945	-171
700	0.966	174	0.676	10	0.0285	74	0.966	-174
800	0.966	171	0.543	5	0.0335	69	0.955	-177
900	0.977	167	0.447	1	0.0394	64	0.966	178
1000	0.966	165	0.359	1	0.0432	64	0.955	178

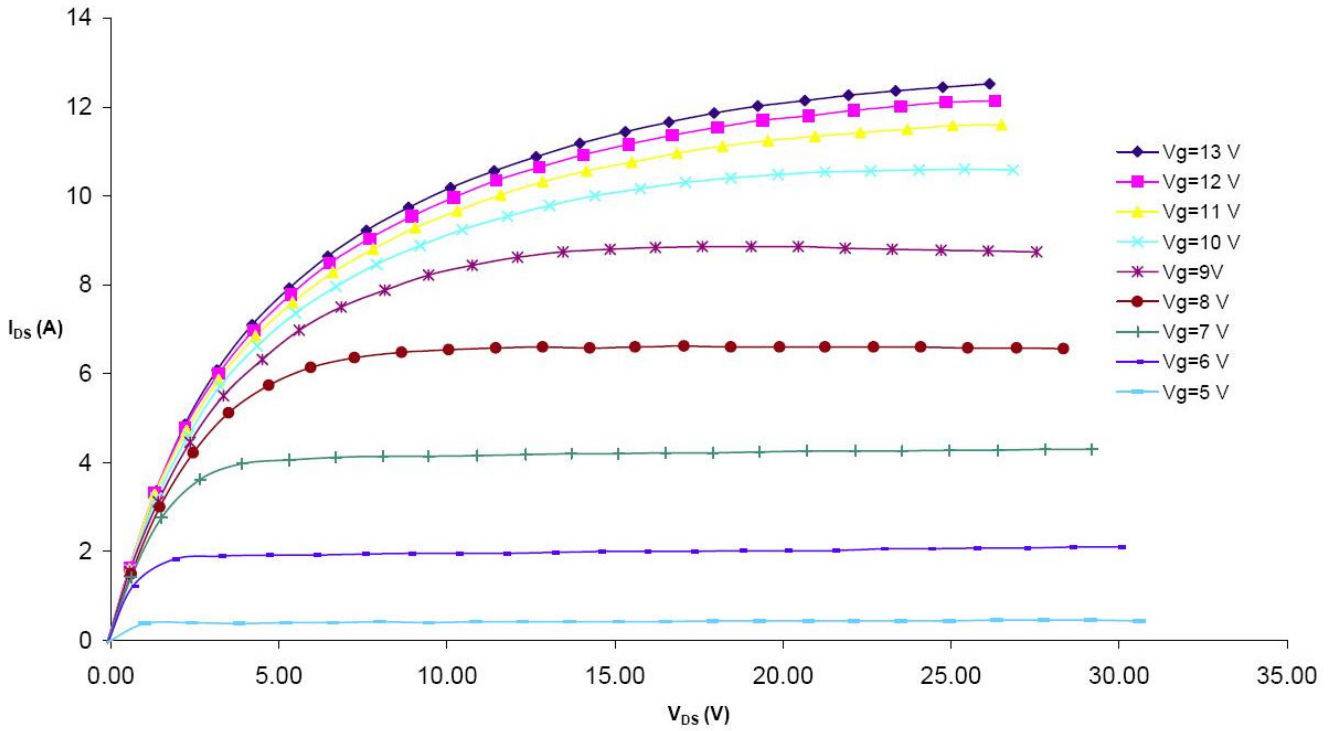


Figure 4—Typical IV Characteristics

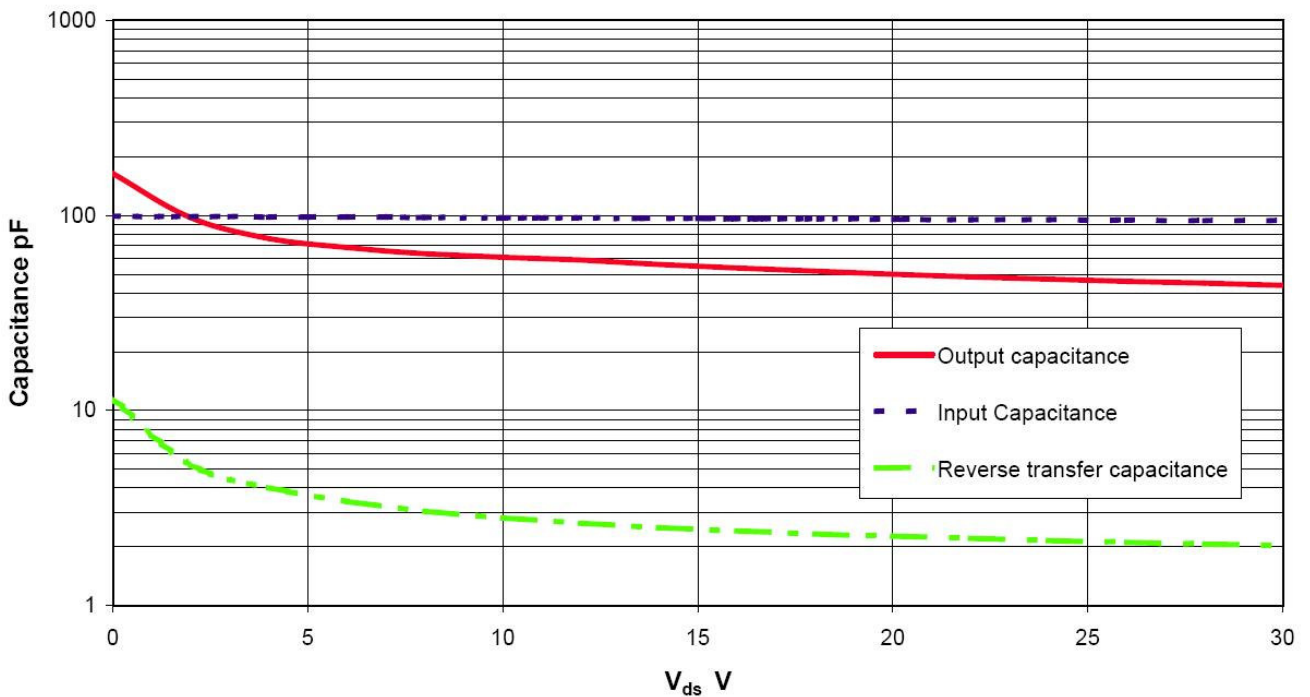
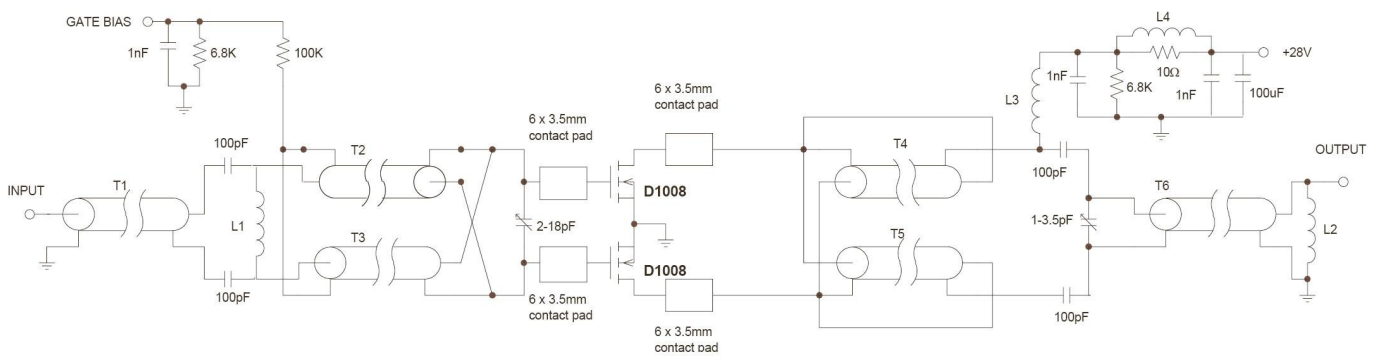


Figure 5—Typical CV Characteristics

TETRA FET

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ROHS COMPLIANT METAL GATE RF SILICON FET



## D1008UK TEST FIXTURE

Substrate 1.6mm PTFE/glass,  $\epsilon_r = 2.5$

All microstrip lines  $W = 4.4\text{mm}$

T1	70mm 50	UT34 SEMI RIGID COAX	L1	3.5 turns of 24swg ECW, 3mm ID
T2, T3	85mm 25	UT70-25 SEMI RIGID COAX	L2	5.5 turns of 24swg ECW, 4mm ID
T4, T5	100mm 15	UT85-15 SEMI RIGID COAX	L3	4 turns of 21swg ECW, 7mm ID
T6	70mm 50	UT85 SEMI RIGID COAX	L4	3 turns of 21swg ECW on Fair-Rite FT50-75 core