Ultra-Linear Mixer with Integrated LO Buffer

Description

The CMY210 is an all port, single-ended, general purpose up- and down-converter.
It combines small conversion losses and excellent intermodulation characteristics with a low demand of LO- and DC-power.
The internal level controlled LO-buffer enables good performance over a wide range of LO level inputs.
The mixer configuration allows RF or IF feed to either pin 1 or 6 and thus requires a frequency separation circuit on the pc board.

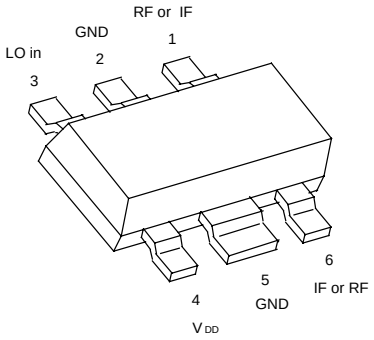
Applications

- Up- or Down-Converters
- Mobile Phones Receivers
- WLAN Receivers
- Mobile Phone or WLAN Basestations

Features

- Very High Input IP3 of 24 dBm typical
- Very Low LO Power demand of 0 dBm typical; Wide input range
- Wide LO Frequency Range: <500 MHz to >2.5 GHz
- Single-Ended Ports
- RF- and IF-Port Impedance 50 ohms
- Operating Voltage Range: <3 to 6 V
- Very Low Current Consumption: 6 mA typical
- All Gold Metalization

Package Outline, MW-6



Maximum Ratings

Parameter	Port	Symbol	Value		Unit
			min	max	
Supply Voltage	4	V_{DD}	0	6	V
DC-Voltage at LO Input	3	V_3	-3	0,5	V
DC-Voltage at RF-IF Ports [2)]	1, 6	$V_{1,6}$	- 0,5	+ 0,5	V
Power into RF-IF Ports	1, 6	$P_{in,RF}$		17	dBm
Power into LO Input	3	$P_{in,LO}$		10	dBm
Channel Temperature		T_{Ch}		150	°C
Storage Temperature		T_{stg}	-55	150	°C

Thermal Resistance			
Channel to Soldering Point (GND)	R_{thChS}	≤100	K/W

1) For detailed dimensions see page 7.
2) For DC test purposes only, no DC voltages at pins 1, 6 in application

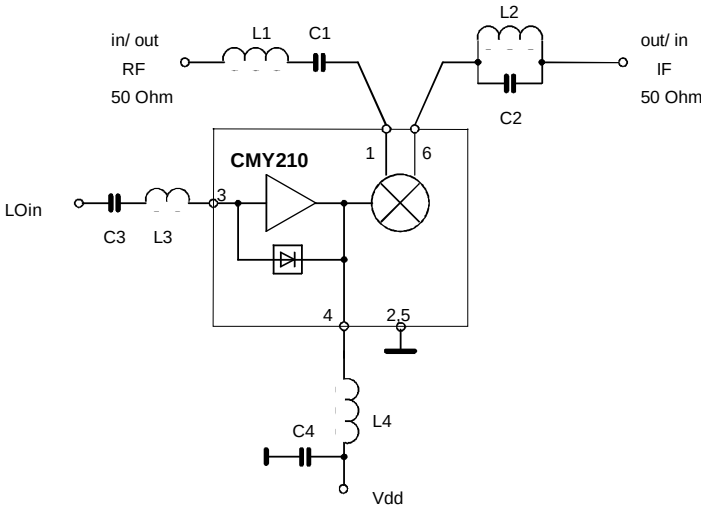
Electrical Characteristics

Test conditions: T_a = 25°C; V_{DD}= 3V, see test circuit; f_{RF} = 808MHz; f_{LO} = 965MHz; P_{LO} = 0dBm; f_{IF} = 157MHz, unless otherwise specified:

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Operating Current	I_{op}	-	6.0	8.0	mA
Conversion Loss	L_c	-	5.7	7.0	dB
SSB Noise Figure	F_{ssb}	-	6.0	-	dB
2 Tone 3rd Order IMD $P_{RF1} = P_{RF2}$ = -3dBm f_{RF1} = 806MHz; f_{RF2} = 810MHz; f_{LO} =965MHz	d_{IM3}	-	54	-	dBc
3rd Order Input Intercept Point	$IP3_{in}$	20	24	-	dBm
P_{-1dB} Input Power	P_{-1dB}	-	14	-	dBm
LO Leakage at RF/IF-Port (1,6)	$P_{LO\ 1,6}$	-	-8	-	dBm

Applications Information

Test circuit / application example



Notes for external elements:

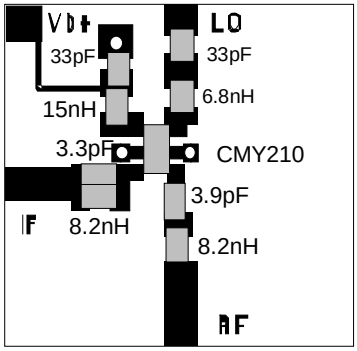
L1, C1: Filter for upper frequency;
C2, L2: Filter for lower frequency;
each filter is a throughpath for the desired frequency (RF or IF) and isolates the other frequency (IF or RF) and its harmonics.
These two filters must be connected to pin 1 and pin 6 directly.
Parasitic capacitances at the ports 1 and 6 must be as small as possible.
L4 and C4 are optimized by indicating lowest I_{op} at used LO-frequency; same procedure for L3.
The ports 1, 3 and 6 must be DC open.

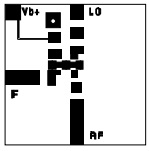
Lumped element values for 800MHz test and application circuit:

f *LO*	F *RF*	F *IF*	L1	C1	L2	C2	L3	C3	L4	C4
MHz	MHz	MHz	nH	pF	nH	pF	nH	pF	nH	pF
965	808	157	8.2	3.9	8.2	3.3	6.8	47	15	33

Applications Information (cont)

PCB-Layout for 800MHz test and application circuit:





Actual size

Typical lumped element values for different RF-frequencies:

f *RF*	L1	C1	L2	C2
MHz	nH	pF	nH	pF
400	12	15	12	12
450	12	12	12	10
900	8.2	3.9	8.2	3.3
1500	3.3	2.7	3.3	2.2
1800	3.3	2.2	3.3	1.8
2000	3.3	1.8	3.3	1.2
2400	1.8	2.7	1.8	1.5

Typical lumped element values for different LO-frequencies:

f *LO*	L3	C3	L4	C4
MHz	nH	pF	nH	pF
500	15	82	47	82
750	6.8	33	22	33
800	6.8	33	18	33
950	6.8	27	15	27
1100	6.8	27	12	27
1400	6.8	22	6.8	22
1600	6.8	18	4.7	18
1800	6.8	15	3.3	15
2000	6.8	12	2.2	12
2100	6.8	12	1.8	12
2300	4.7	12	1.2	12

General description and notes

The CMY 210 is an all port single ended general purpose Up- and Down-Converter.
It combines small conversion losses and excellent intermodulation characteristics with a low demand of LO- and DC-power.
The internal level controlled LO-Buffer enables a good performance over a wide LO level range.
The internal mixers principle with one port RF and IF requires a frequency separation at pin 1 and 6 respectively.

Note 1:
Best performance with lowest conversion loss is achieved when each circuit or device for the frequency separation meets the following requirements:

Input Filter: Throughpass for the signal to be mixed; reflection of the mixed signal and the harmonics of both.

Output Filter: Throughpass for the mixed signal and reflection of the signal to be mixed and the harmonics of both.

The impedance for the reflecting frequency range of each filter toward the ports 1 and 6 should be as high as possible.
In the simplest case a series- and a parallel- resonator circuit will meet these requirements but also others as appropriate drop in filters or micro stripline elements can be used.
The two branches with filters should meet immediately at the package leads of the port 1 and 6.
Parasitic capacitances at these ports must be kept as small as possible.
The mixer also can be driven with a source- and load impedance different to 50Ω, but performance will degrade at larger deviations.

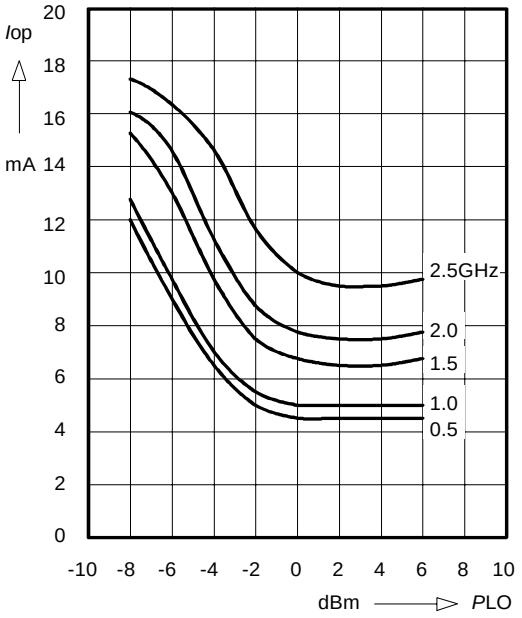
Note 2:
The LO-Buffer needs an external inductor L4 at port 4; the value of inductance depends on the LO frequency. It is tuned for minimum I_{op} consumption into port 4.
At lower LO frequencies it can be reduced by an additional capacitor C5.

Note 3:
The LO Input impedance at Port 3 can be matched with a series inductor. It also can be tuned for a minimum current I_{op} into port 4. C3 is a DC blocking capacitor.
Since the input impedance of port 3 can be slightly negative, the source reflection coefficient should be kept below 0.8 ($Z_0 = 50\ \Omega$).

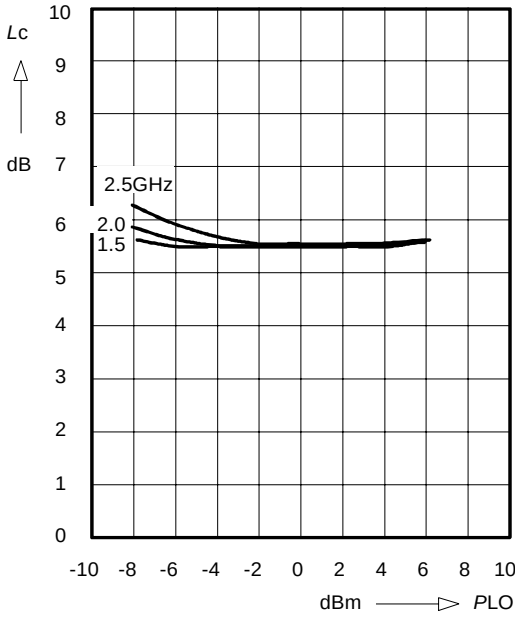
The Conversion Noise Figure Fssb is corresponding with the value of Conversion Loss L_c. The LO signal must be clean of noise and spurious at the frequencies $f_{LO} \pm f_{IF.}$

Electrical Characteristics (cont)

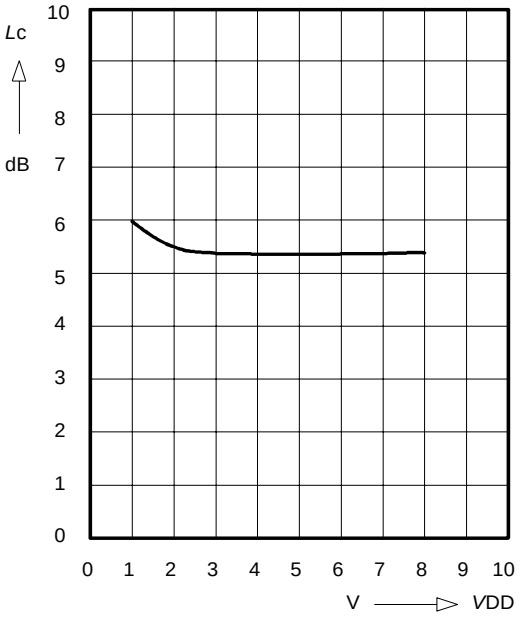
Operating Current *I*op = f (*P*LO)
*V*DD = 3V
*f*LO = Parameter



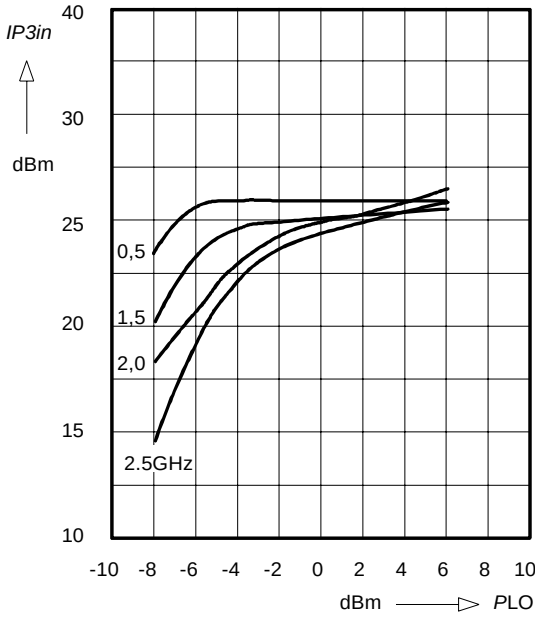
Conversion Loss *L*c = f (PLO)
*V*DD = 3V; fIF = 120MHz
*f*LO = Parameter



Conversion Loss *L*c = f (*V*DD)
*P*LO = 0dBm
*f*LO = 1500MHz; *f*IF = 120MHz

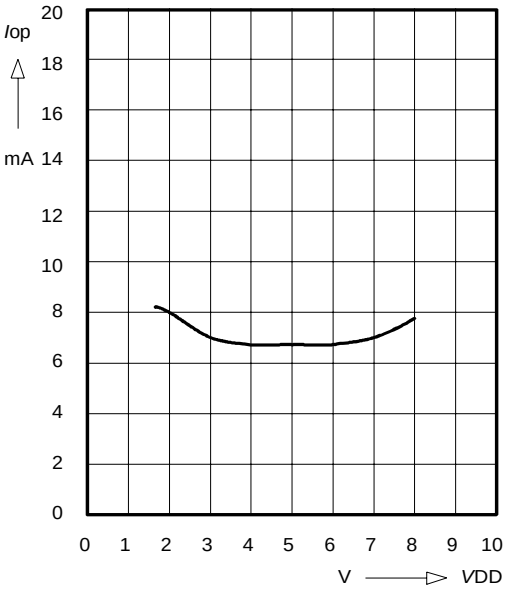


Third Order IP3 *IP3in* = f (PLO)
*P*in = 2 x -3dBm; fIF = 40/45MHz
*V*DD = 3V; *f*LO = Parameter;

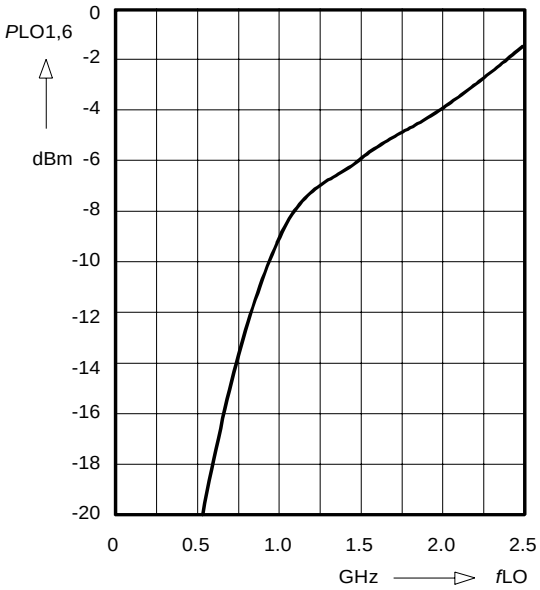


Electrical Characteristics (cont)

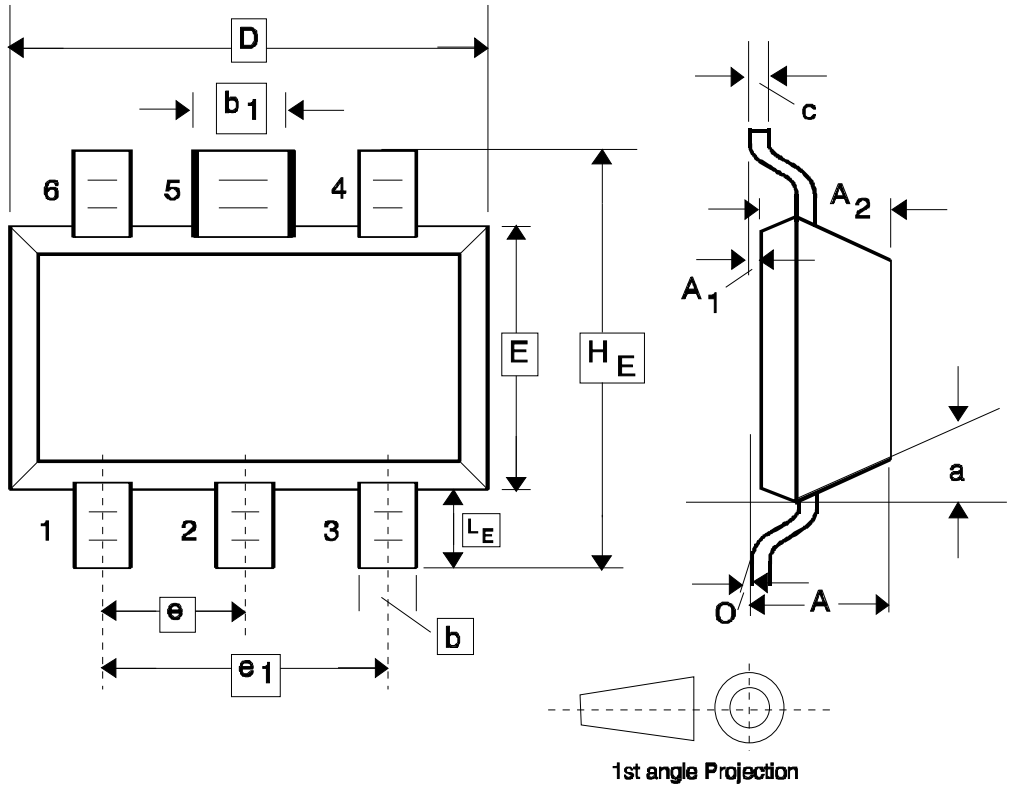
Operating Current $I_{op} = f(V_{DD})$
P_{LO} = 0dBm
f_{LO} = 1500MHz



LO-Leakage at Port 1, 6 $P_{LO1,6} = f(f_{LO})$
P_{LO} = 0dBm
V_{DD} = 3V



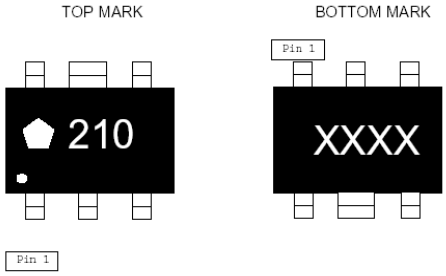
Semiconductor Device Outline MW-6



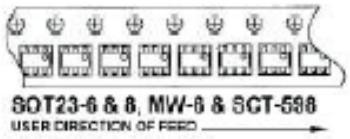
Dim.	min.	nom.	max.	Gradient	Remark
A			1.1		
A_1			0.1		
A_2			1.0		
b		0.3			
b_1		0.6			
c	0.08		0.15		
D	2.8		3.0		
E	1.2		1.4		
|e|		0.95			
$\|e_1\|$		1.9			
H_E			2.6		
L_E			0.6		
a				max 10°	1
q				2°...30°	

1. Applicable on all case top sides

Part Marking



Part Orientation on Reel



Ordering Information

Type	Marking	Ordering code (tape and reel)	Package [1)]
CMY210	210	CMY210	MW-6

Additional Information

This part is compliant with RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

ESD: **E**lectro**s**tatic **d**ischarge sensitive device. Observe handling Precautions.

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