P/N: TS32M7MAR00IS1
TS64M7MAR00IS1

SATA III 6Gb/s mSATA SSD

Transcend mSATA Solid State Drives (SSDs) with high performance and quality Flash Memory assembled on a printed circuit board. These devices feature cutting-edge technology to enhance product life and data retention. It is designed specifically for various applications, such as Ultrabooks, industrial PCs, vehicle PCs and road surveillance recording.

- Power Supply: 3.3V±5%
- Fully compatible with devices and OS that support the SATA III 6.0Gb/s standard
- Non-volatile Flash Memory for outstanding data retention
- Supports Trim and NCQ command
- Compliant with JEDEC MO-300

Features

- RoHS compliant
- Advanced Global Wear-Leveling and Block management for reliability
- Built-in ECC (Error Correction Code) functionality
- Features a DDR3 DRAM Cache
- Supports Advanced Garbage Collection
- Supports Enhanced S.M.A.R.T. function
- Power Shield to prevent data loss in the event of a sudden power outage
- Supports partial and slumber mode
- Supports Security Command
- Supports DevSleep mode
- Supports Hardware Purge and Hardware Write Protect (Optional)
- Supports Transcend SSD Scope Pro (Optional)
- Real time full drive encryption with Advanced Encryption Standard (AES) (Optional)

Specifications

Physical Specification			
Form Factor		MO-300	
Storage Capacities		16GB to 1TB	
Dimensions	**Length**	50.8 ± 0.15 mm	1.175 ± 0.006 inch
	Width	29.85 ± 0.15 mm	2.000 ± 0.006 inch
	Height	Max 4.85 mm	Max 0.111 inch
Input Voltage		3.3V ± 5%	
Weight		8g	
Connector		PCI Express Mini Card Connector	

Environmental Specifications		
Operating Temperature		0 ℃to 70 ℃
Storage Temperature		-40 ℃to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Performance								
CAPACITY	**ATTO**		**CrystalDiskMark**				**IOMeter**	
	Max Read *	**Max Write ***	**Sequential Read ****	**Sequential Write ****	**Random Read (4KB QD32) ****	**Random Write (4KB QD32) ****	**IOPS Random Read (4KB QD32) *****	**IOPS Random Write (4KB QD32) *****
32GB	280	50	280	50	110	55	26K	13K
64GB	560	100	520	100	200	100	50K	25K

Note: Maximum transfer speed recorded

***25 °C, test on ASUS P8Z68-M PRO, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility ATTO (version 2.41), unit MB/s**

****25 °C, test on ASUS P8Z68-M PRO, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility CrystalDiskMark (version 3.0.1), copied file 1000MB, unit MB/s**

*****25 °C, test on ASUS P8Z68-M PRO, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility IOmeter2006 with 4K file size and queue depth of 32, unit IOPs**

******The recorded performance is obtained while the SSD is not operating as an OS disk**

Actual Capacity				
CAPACITY	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
32GB	62,533,296	16,383	16	63
64GB	125,045,424	16,383	16	63

Power Consumption		
Input Voltage		3.3V ± 5%
CAPACITY / Power Consumption		**Average (mA)**
32GB	**Max Read**	190
	Max Write	200
	Idle	85
64GB	**Max Read**	225
	Max Write	245
	Idle	85

*Tested with IOmeter running sequential reads/writes and idle mode

Reliability			
Data Reliability	Supports BCH ECC 42 bit per 1024 byte		
MTBF	1,500,000 hours		
	Capacity	* TBW	** TBW (Base on JEDEC Standard)
	32GB	90TB	45TB
	64GB	180TB	90TB
DWPD (Drive Writes Per Day for 3years)	2.2 DWPD		

*Tested under burn-in tool, TBW value may vary due to host environment.

**Tested under JESD218A endurance test method and JESD219A endurance workloads specification.

Vibration	
Operating	3.0G, 5 - 800Hz
Non-Operating	5.0G, 5 - 800Hz

Reference to IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

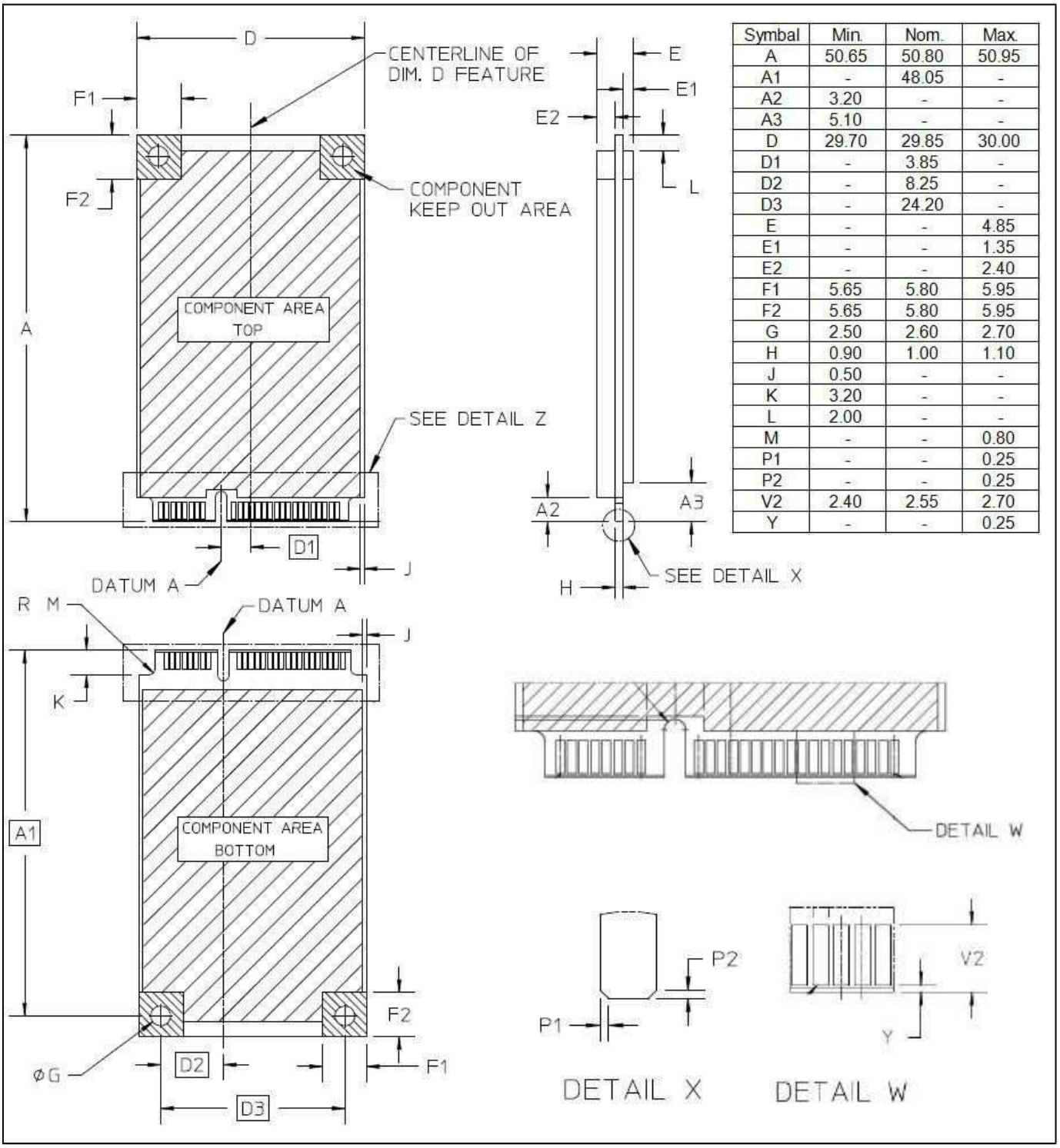
Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

Reference to IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500G, 0.5ms, 3 times/dir., total 18 times.

Regulations	
Compliance	CE, FCC and BSMI

Package Dimensions

The figure below illustrates the Transcend mSATA Solid State Disk product. All dimensions are in mm.



Symbal	Min.	Nom.	Max.
A	50.65	50.80	50.95
A1	-	48.05	-
A2	3.20	-	-
A3	5.10	-	-
D	29.70	29.85	30.00
D1	-	3.85	-
D2	-	8.25	-
D3	-	24.20	-
E	-	-	4.85
E1	-	-	1.35
E2	-	-	2.40
F1	5.65	5.80	5.95
F2	5.65	5.80	5.95
G	2.50	2.60	2.70
H	0.90	1.00	1.10
J	0.50	-	-
K	3.20	-	-
L	2.00	-	-
M	-	-	0.80
P1	-	-	0.25
P2	-	-	0.25
V2	2.40	2.55	2.70
Y	-	-	0.25

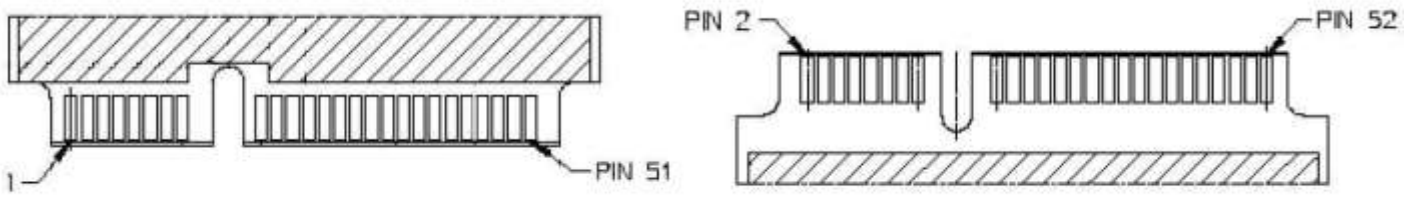
Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name
01	NC	02	3.3V
03	NC	04	GND
05	NC	06	NC
07	NC	08	NC
09	GND	10	NC
11	NC	12	NC
13	NC	14	NC
15	GND	16	NC
17	NC	18	GND
19	NC	20	NC
21	GND	22	NC
23	TX+	24	3.3V
25	TX-	26	GND
27	GND	28	NC
29	GND	30	NC
31	RX-	32	NC
33	RX+	34	GND
35	GND	36	NC
37	GND	38	NC
39	3.3V	40	GND
41	3.3V	42	NC
43	NC	44	DEVSLP
45	NC	46	NC
47	NC	48	NC
49	DAS/DSS*	50	GND
51	Presence Detection**	52	3.3V

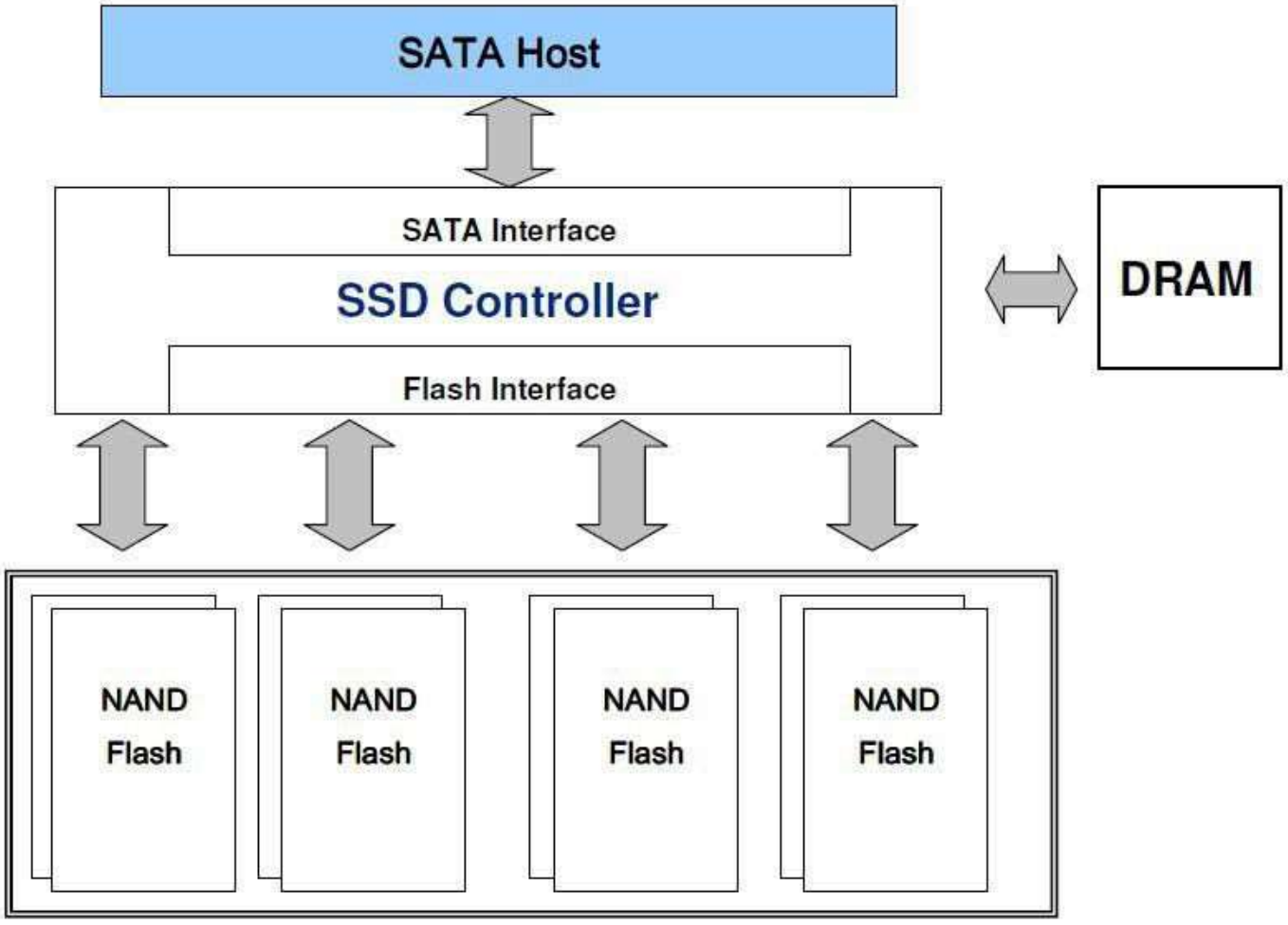
* Device Activity Signal / Disable Staggered Spin-up

** Connect to GND internally

Pin Layout



Block Diagram



Features

- **Global Wear Leveling – Advanced algorithms to enhance wear-leveling efficiency**

Gloďal ‖ear le|eliŶg eŶsures e|erLJ ďloÐk has aŶ e|eŶ erase ÐouŶt. BLJ eŶsuriŶg all spare ďloÐks iŶ the SSD's flash Ðhips are managed in a single pool, each block can then have an even erase count. This helps to extend the lifespan of a SSD and to provide the best possible endurance.

There are three main processes in global wear -leveling:

(1) Record the block erase count and save this in the wear-leveling table.

(2) Finds the static-block and saves this in the wear-leveling pointer.

(3) Checks the erase count when a block is pulled from the pool of spare blocks. If the erased block count is larger than the Wear Count (WEARCNT), then the static blocks are leveraged against the over-countblocks.

- **ECC Algorithm**

The controller uses a BCH 42 Bit ECC algorithm per 1024 bytes depending on the structure of the flash. BCH42 may correct up to 42 random bit errors within 1024 data bytes. With the help of BCH42 ECC, the endurance of the Transcend SSD is greatly improved.

- **Bad Block Management**

When the flash encounters an ECC, program or erase failure, the controller will mark the block as a bad block to prevent use of this block and cause data loss in the future.

- **Advanced Garbage Collection**

TraŶsÐeŶd's Garďage ColleÐtioŶ ŵeÐhaŶisŵ iŵpro|es SSD performance. Advanced Garbage Collection can efficiently iŵpro|e ŵeŵorLJ ŵaŶageŵeŶt to eŶsure staďle SSD perforŵaŶÐe. TraŶsÐeŶd's ad|aŶÐed flash ŵaŶageŵeŶt ÐaŶ ŵaiŶtaiŶ the dri|e's high perforŵaŶÐe e|eŶ after aŶ edžteŶded operatiŶg tiŵe.

- **Enhanced S.M.A.R.T. function**

TraŶsÐeŶd's SSDs support the iŶŶo|ati|e S.M.A.R.T. ÐoŵŵaŶd (Self-Monitoring, Analysis, and Reporting Technology) which allows users to evaluate the health status of their SSD efficiently.

- **Hardware Purge and Hardware Write Protect (Optional)**

The SSDs have optional features such as hardware trigger for quick data erase and write protection. These features may be enabled by simply connecting a switch to the designated pins.

- **StaticDataRefresh Technology**

Normally, the ECC engine corrections take place without affecting normal host operations. Over time, the number of bit errors accumulated in the read transaction exceeds the correcting capacity of the ECC engine, which results in corrupted data being sent to the host. To prevent this, the controller monitors the bit error levels during each read operation; when the number of bit errors reaches the preset threshold value, the controller automatically performs a data refresh to restore the ÐorreÐt Ðharge le|els iŶ the Ðell. IŵpleŵeŶtatioŶ of StatiÐDataRefresh Technology reinstates the data to its original, error-free state, aŶd heŶÐe, leŶgths the data's lifespaŶ.

ATA Command Register

This table and the following paragraphs summarize the ATA command set.

Command Table

Support ATA/ATAPI Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
Initialize Drive Parameters	91h	Non-data
READ DMA	C8h	DMA
READ LOG Ext	2Fh	PIO data-In
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	Cah	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Mode Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read LOG	B0h	PIO data-In
SMART Read Data	B0h	PIO data-In
SMART Read THRESHOLD	B0h	PIO data-In
SMART Return Status	B0h	Non-data
SMART SAVE ATTRIBUTE VALUES	B0h	Non-data
SMART WRITE LOG	B0h	PIO data-out
Host Protected Area Feature Set		

Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	Eah	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Other		
Data Set Management	06h	DMA
SEEK	70h	Non-data

SMART Data Structure

BYTE	F / V	Description
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-397	F	Reserved
398-399	V	Reserved
400-406	V	TS6500
407-415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418-419	V	Number of spare block
420-423	V	Average Erase Count
424-510	X	Vendor specific
511	V	Data structure checksum

F = content (byte) is fixed and does not change.

V= content (byte) is variable and may change depending on the state of the device or the commands executed by the device.

X= content (byte) is vendor specific and may be fixed or variable.

R= content (byte) is reserved and shall be zero.

SMART Attributes

The following table shows the vendor specific data in byte 2 to 361 of the 512-byte SMART data

Attribute ID (hex)	Raw Attribute Value							Attribute Name
01	MSB	00	00	00	00	00	00	Read Error Rate
05	LSB	MSB	00	00	00	00	00	Reallocated sectors count
09	LSB	-	-	MSB	00	00	00	Power-on hours
0C	LSB	-	-	MSB	00	00	00	Power Cycle Count
A0	LSB	-	-	MSB	00	00	00	Uncorrectable sectors count when read/write
A1	LSB	MSB	00	00	00	00	00	Number of valid spare blocks
A3	LSB	MSB	00	00	00	00	00	Number of initial invalid blocks
A4	LSB	-	-	MSB	00	00	00	Total erase count
A5	LSB	-	-	MSB	00	00	00	Maximum erase count
A6	LSB	-	-	MSB	00	00	00	Minimum erase count
A7	LSB	-	-	MSB	00	00	00	Average erase count
A8	LSB	-	-	MSB	00	00	00	Max erase count of spec
A9	LSB	-	-	MSB	00	00	00	Remain Life (percentage)
AF	LSB	-	-	MSB	00	00	00	Program fail count in worst die
B0	LSB	MSB	00	00	00	00	00	Erase fail count in worst die
B1	LSB	-	-	MSB	00	00	00	Total wear level count
B2	LSB	MSB	00	00	00	00	00	Runtime invalid block count
B5	LSB	-	-	MSB	00	00	00	Total program fail count
B6	LSB	MSB	00	00	00	00	00	Total erase fail count
C0	LSB	MSB	00	00	00	00	00	Power-off retract Count
C2	MSB	00	00	00	00	00	00	Controlled temperature
C3	LSB	-	-	MSB	00	00	00	Hardware ECC recovered
C4	LSB	-	-	MSB	00	00	00	Reallocation event count
C5	LSB	MSB	00	00	00	00	00	Current Pending Sector Count
C6	LSB	-	-	MSB	00	00	00	Uncorrectable error count off-line
C7	LSB	MSB	00	00	00	00	00	Ultra DMA CRC Error Count
E8	LSB	MSB	00	00	00	00	00	Available reserved space
F1	LSB	-	-	-	-	-	MSB	Total LBA written (each write unit = 32MB)
F2	LSB	-	-	-	-	-	MSB	Total LBA read (each read unit = 32MB)
F5	LSB	-	-	-	-	-	MSB	Flash write sector count

Revision History(D)		
Version	**Date**	**Modification Content**
V1.0	**2017/03/03**	**Initial Release**