

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MH138FK

3-to-8 Line Decoder

The TC7MH138FK is an advanced high speed CMOS 3-to-8 decoder fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

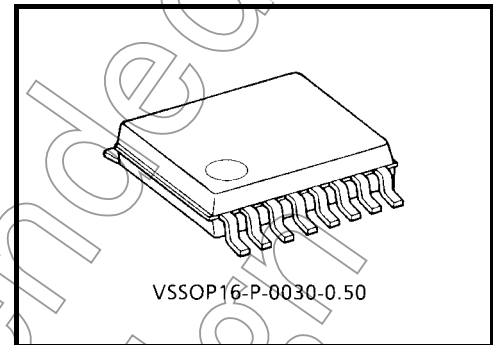
When the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs ($\bar{Y}0 - \bar{Y}7$) will go low.

When enable input G1 is held low or either $\bar{G}2A$ or $\bar{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\bar{G}2A$, and $\bar{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage.

This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

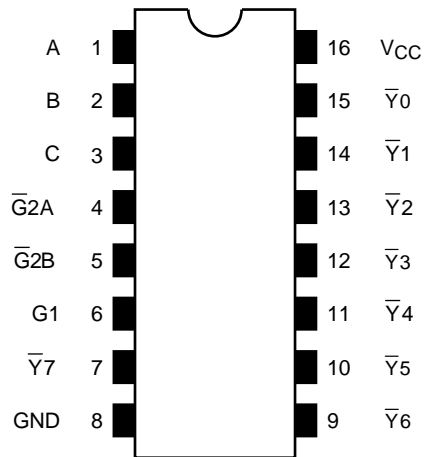


Weight: 0.02 g (typ.)

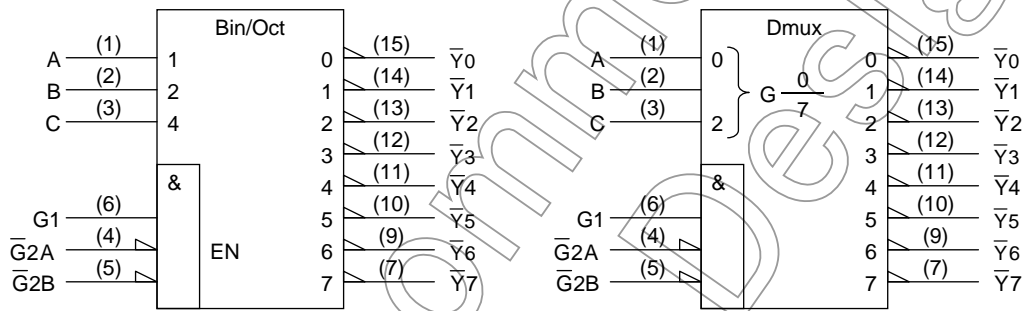
Features

- High speed: $t_{pd} = 5.7$ ns (typ.) ($V_{CC} = 5$ V)
- Low power dissipation: $I_{CC} = 4$ μ A (max) ($T_a = 25^\circ\text{C}$)
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 2\sim 5.5$ V
- Pin and function compatible with 74ALS138

Pin Assignment (top view)



IEC Logic Symbol

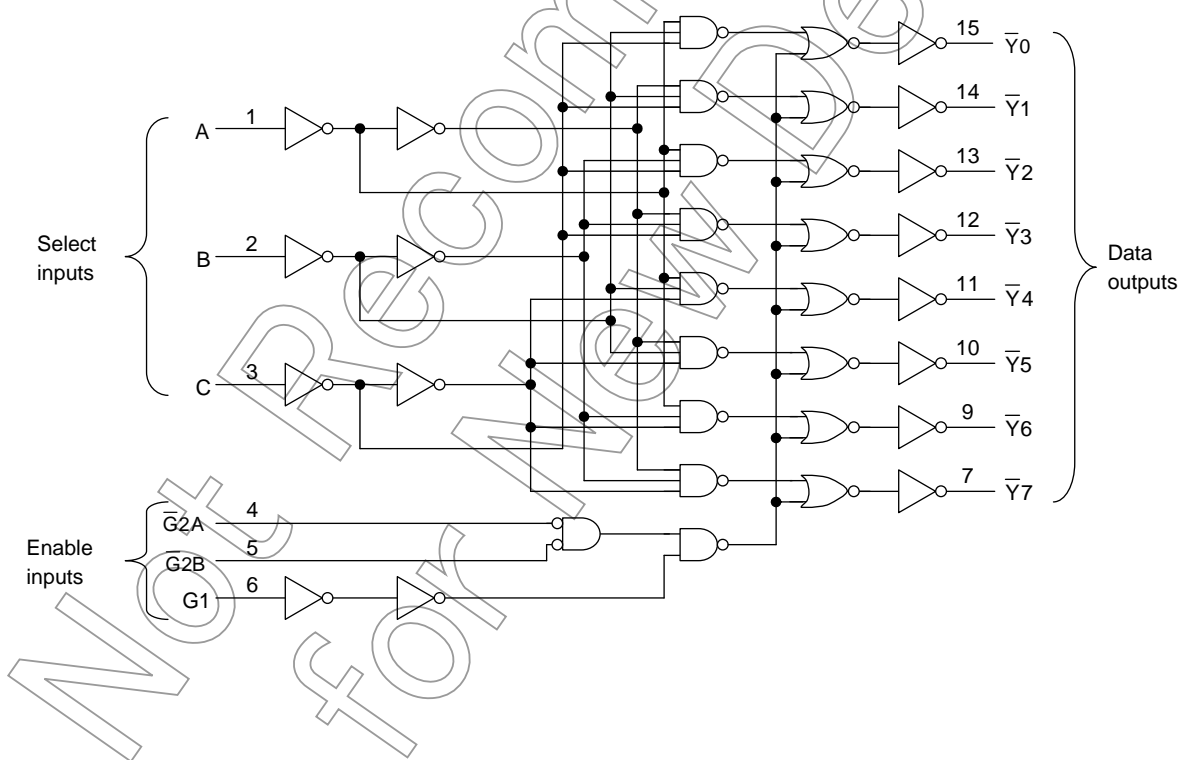


Truth Table

Inputs						Outputs								Selected Output
Enable			Select			\bar{Y}_0	\bar{Y}_1	\bar{Y}_2	\bar{Y}_3	\bar{Y}_4	\bar{Y}_5	\bar{Y}_6	\bar{Y}_7	
G1	$\bar{G}2A$	$\bar{G}2B$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	None
X	H	X	X	X	X	H	H	H	H	H	H	H	H	None
X	X	H	X	X	X	H	H	H	H	H	H	H	H	None
H	L	L	L	L	L	L	H	H	H	H	H	H	H	\bar{Y}_0
H	L	L	L	L	H	H	L	H	H	H	H	H	H	\bar{Y}_1
H	L	L	L	H	L	H	H	L	H	H	H	H	H	\bar{Y}_2
H	L	L	L	H	H	H	H	H	L	H	H	H	H	\bar{Y}_3
H	L	L	H	L	L	H	H	H	H	L	H	H	H	\bar{Y}_4
H	L	L	H	L	H	H	H	H	H	H	L	H	H	\bar{Y}_5
H	L	L	H	H	L	H	H	H	H	H	H	L	H	\bar{Y}_6
H	L	L	H	H	H	H	H	H	H	H	H	H	L	\bar{Y}_7

X: Don't care

Logic Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5~7.0	V
DC input voltage	V_{IN}	-0.5~7.0	V
DC output voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC} /ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~5.5	V
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~100 ($V_{CC} = 3.3 \pm 0.3$ V)	ns/V
		0~20 ($V_{CC} = 5 \pm 0.5$ V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit		
			V_{CC} (V)	Min	Typ.	Max	Min		Max	
Input voltage	High level V_{IH}	—	2.0	1.50	—	—	1.50	—	V	
			3.0~5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—		
Low level V_{IL}	—	2.0	—	—	0.50	—	0.50			
		3.0~5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$			
Output voltage	High level V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			4.5	4.4	4.5	—	4.4	—		
			$I_{OH} = -4 \text{ mA}$	3.0	2.58	—	—	2.48	—	
	Low level V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu\text{A}$	2.0	—	0	0.1	—	0.1	
				3.0	—	0	0.1	—	0.1	
			$I_{OL} = 4 \text{ mA}$	3.0	—	—	0.36	—	0.44	
			$I_{OL} = 8 \text{ mA}$	4.5	—	—	0.36	—	0.44	
Input leakage current	I_{IN}	$V_{IN} = 5.5 \text{ V}$ or GND	0~5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	μA	

AC Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

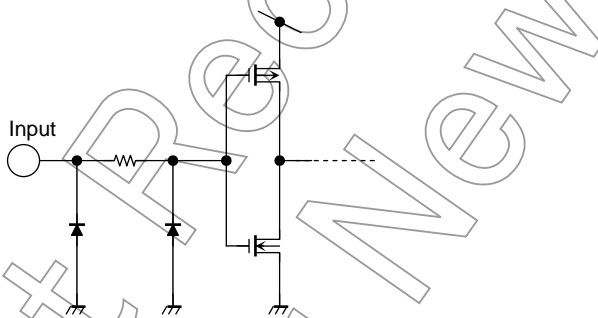
Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40~85°C		Unit
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (A, B, C- \bar{Y})	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	8.2	11.4	1.0	13.5	ns
				50	—	10.0	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	5.7	8.1	1.0	9.5	
				50	—	7.2	10.1	1.0	11.5	
Propagation delay time (G1- \bar{Y})	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	8.1	12.8	1.0	15.0	ns
				50	—	10.6	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.6	8.1	1.0	9.5	
				50	—	7.1	10.1	1.0	11.5	
Propagation delay time ($\bar{G}2 - \bar{Y}$)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	8.2	11.4	1.0	13.5	ns
				50	—	10.7	14.9	1.0	17.0	
			5.0 ± 0.5	15	—	5.8	8.1	1.0	9.5	
				50	—	7.3	10.1	1.0	11.5	
Input capacitance	C _{IN}	—	—	—	4	10	—	10	pF	
Power dissipation capacitance	C _{PD}	—	(Note)	—	34	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

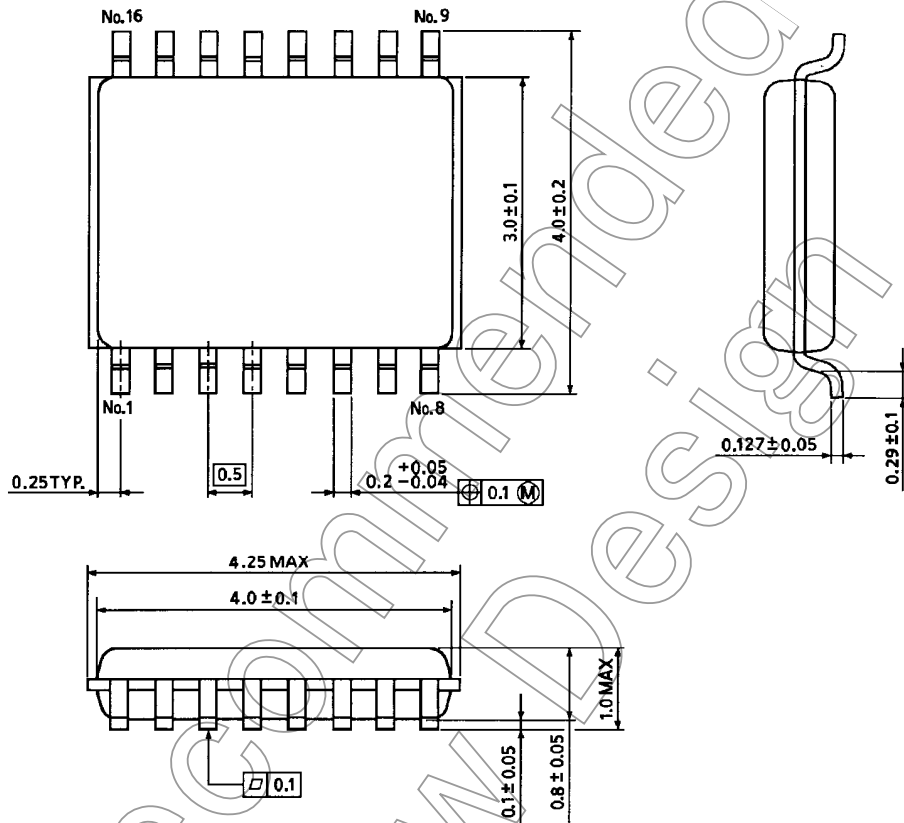
Input Equivalent Circuit



Package Dimensions

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)

Not Recommended for New Designs

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