

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC74F, TC74VHC74FK

## Dual D-Type Flip-Flop with Preset and Clear

The TC74VHC74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

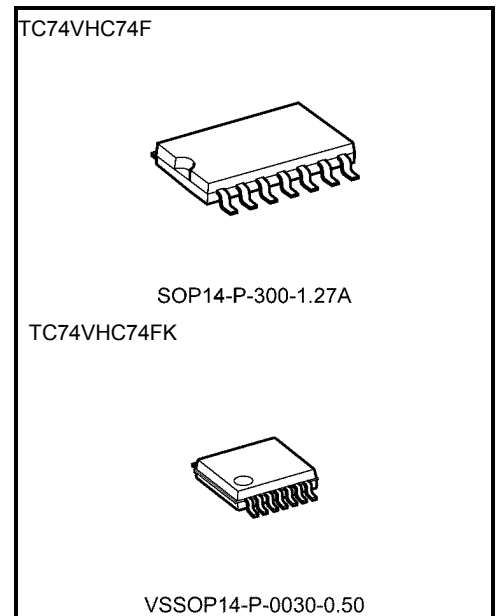
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{CLR}$  and  $\overline{PR}$  are independent of the CK and are accomplished by setting the appropriate input low.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High speed:  $f_{max} = 170$  MHz (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 2$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC(opr)} = 2$  V to 5.5 V
- Pin and function compatible with 74ALS74



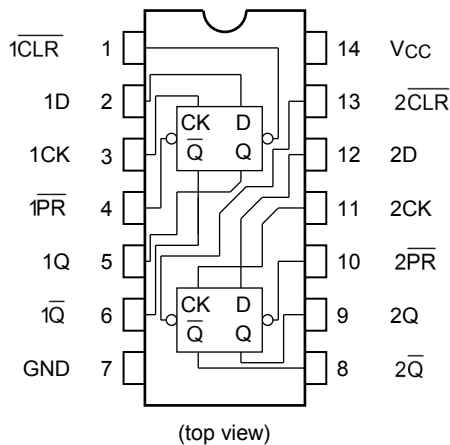
Weight

SOP14-P-300-1.27A : 0.18 g (typ.)

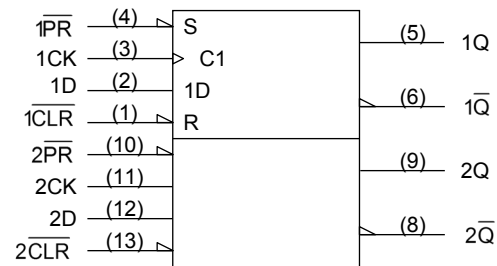
VSSOP14-P-0030-0.50 : 0.02 g (typ.)

Start of commercial production  
1991-05

### Pin Assignment



### IEC Logic Symbol



### Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q <sup>̄</sup>	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q <sub>n</sub>	Q <sub>n</sub> <sup>̄</sup>	No Change

X: Don't care

### Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	-20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±50	mA
Power dissipation	P <sub>D</sub>	180	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2.0 to 5.5	V
Input voltage	V <sub>IN</sub>	0 to 5.5	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V <sub>CC</sub> = 3.3 ± 0.3 V) 0 to 20 (V <sub>CC</sub> = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either V<sub>CC</sub> or GND.

### Electrical Characteristics

#### DC Characteristics

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V <sub>IH</sub>	—	2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V	
Low-level input voltage	V <sub>IL</sub>	—	2.0 3.0 to 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I <sub>OH</sub> = -4 mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
			I <sub>OH</sub> = -8 mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I <sub>OL</sub> = 4 mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
			I <sub>OL</sub> = 8 mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	2.0	—	20.0	μA	

### Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Unit	
			VCC (V)	Limit		
Minimum pulse width (CK)	$t_w(L)$	—	3.3 ± 0.3	6.0	ns	
	$t_w(H)$		5.0 ± 0.5	5.0		
Minimum pulse width ( $\overline{CLR}$ , $\overline{PR}$ )	$t_w(L)$	—	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
Minimum set-up time	$t_s$	—	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
Minimum hold time	$t_h$	—	3.3 ± 0.3 5.0 ± 0.5	0.5 0.5	0.5 0.5	ns
Minimum removal time ( $\overline{CLR}$ , $\overline{PR}$ )	$t_{rem}$	—	3.3 ± 0.3	5.0	5.0	ns
			5.0 ± 0.5	3.0	3.0	

### AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

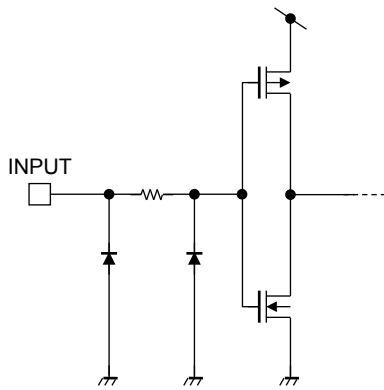
Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			VCC (V)	CL (pF)	Min	Typ.	Max		Min	Max
Propagation delay time (CK-Q, $\overline{Q}$ )	$t_{pLH}$ $t_{pHL}$	—	3.3 ± 0.3	15	—	6.7	11.9	1.0	14.0	ns
				50	—	9.2	15.4	1.0	17.5	
			5.0 ± 0.5	15	—	4.6	7.3	1.0	8.5	
				50	—	6.1	9.3	1.0	10.5	
Propagation delay time ( $\overline{CLR}$ , $\overline{PR}$ -Q, $\overline{Q}$ )	$t_{pLH}$ $t_{pHL}$	—	3.3 ± 0.3	15	—	7.6	12.3	1.0	14.5	ns
				50	—	10.1	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	4.8	7.7	1.0	9.0	
				50	—	6.3	9.7	1.0	11.0	
Maximum clock frequency	$f_{max}$	—	3.3 ± 0.3	15	80	125	—	70	—	MHz
				50	50	75	—	45	—	
			5.0 ± 0.5	15	130	170	—	110	—	
				50	90	115	—	75	—	
Input capacitance	$C_{IN}$	—	—	4	10	—	10	pF		
Power dissipation capacitance	$C_{PD}$	(Note)	—	25	—	—	—	pF		

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

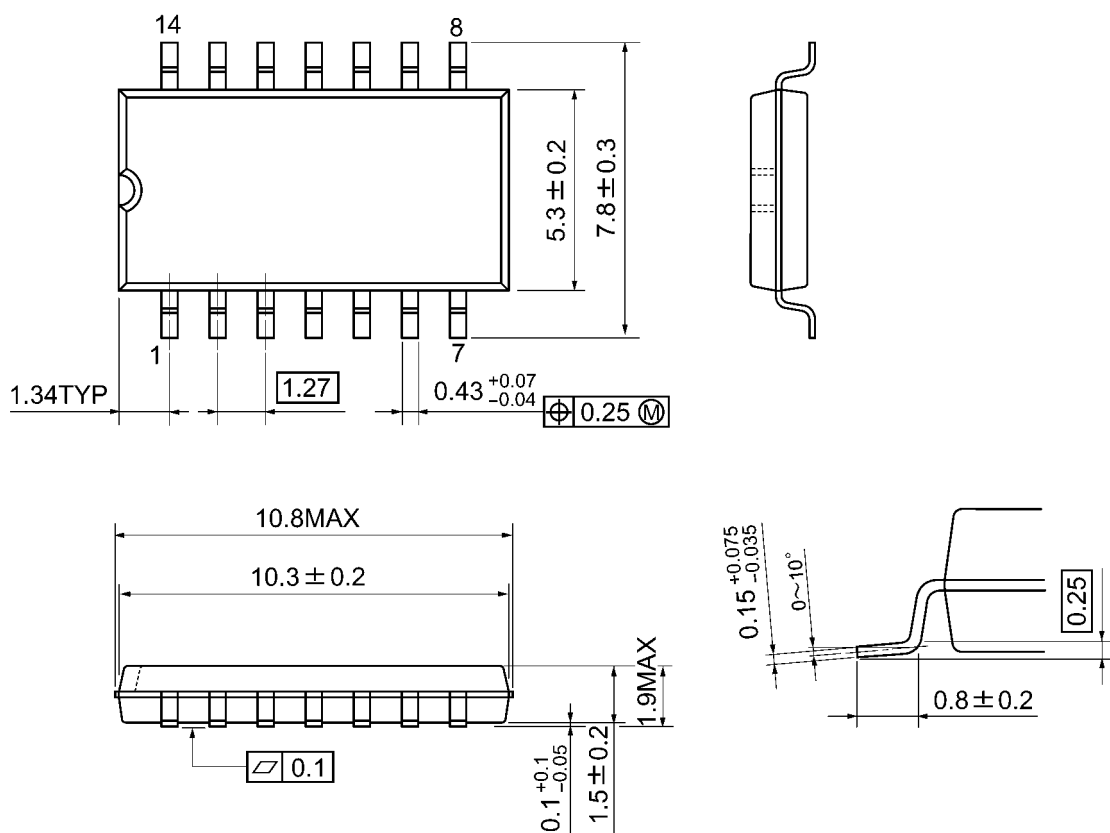
### Input Equivalent Circuit



### Package Dimensions

SOP14-P-300-1.27A

Unit: mm

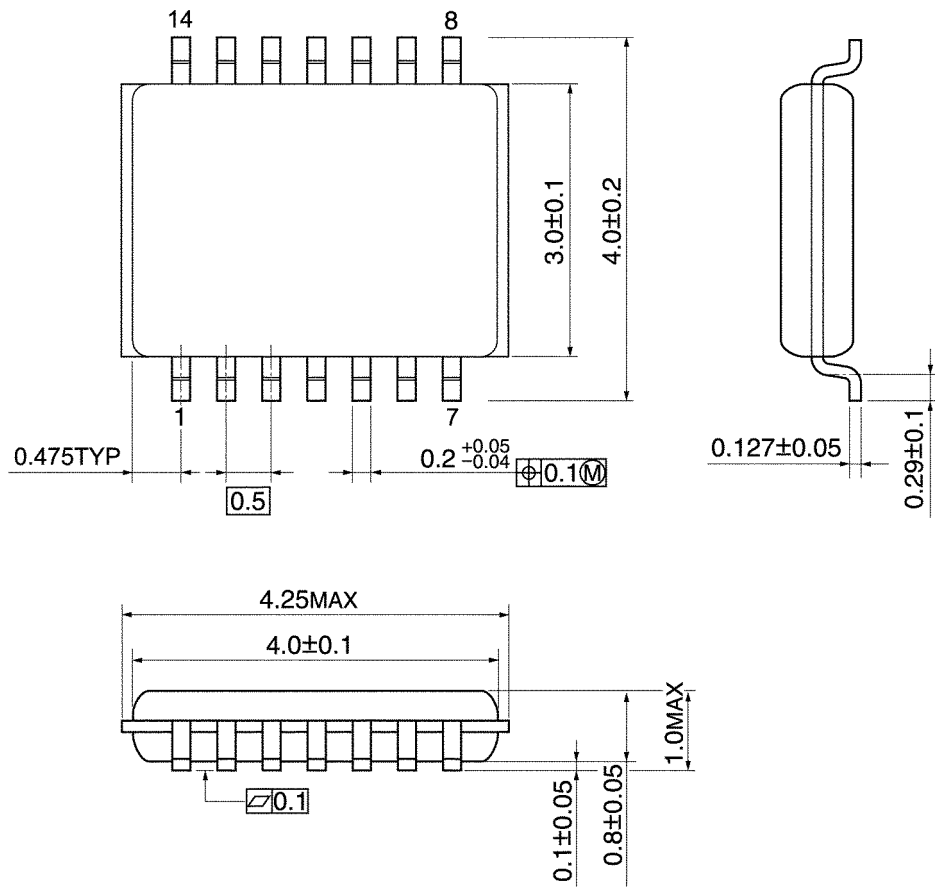


Weight: 0.18 g (typ.)

### Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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