

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC540F, TC74VHC540FK

TC74VHC541F, TC74VHC541FK

Octal Bus Buffer

TC74VHC540F/FK Inverted, 3-State Outputs
 TC74VHC541F/FK Non-Inverted, 3-State Outputs

The TC74VHC540/TC74VHC541 are advanced high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

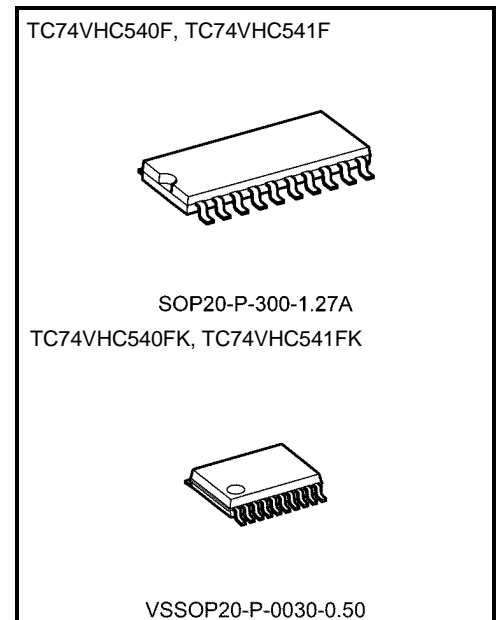
The TC74VHC540 is an inverting type, and the TC74VHC541 is a non-inverting type.

When either $\bar{G}1$ or $\bar{G}2$ are high, the terminal outputs are in the high-impedance state.z

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High speed: $t_{pd} = 3.7 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 4 \text{ } \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (\text{opr}) = 2 \text{ V to } 5.5 \text{ V}$
- Low noise: $V_{OLP} = 1.0 \text{ V (max)}$
- Pin and function compatible with 74ALS540/541

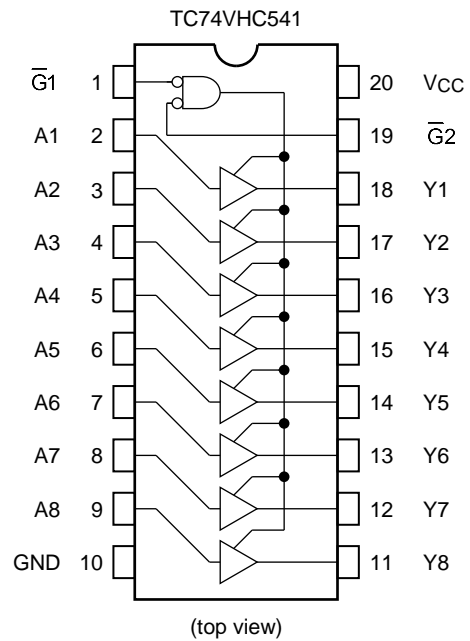
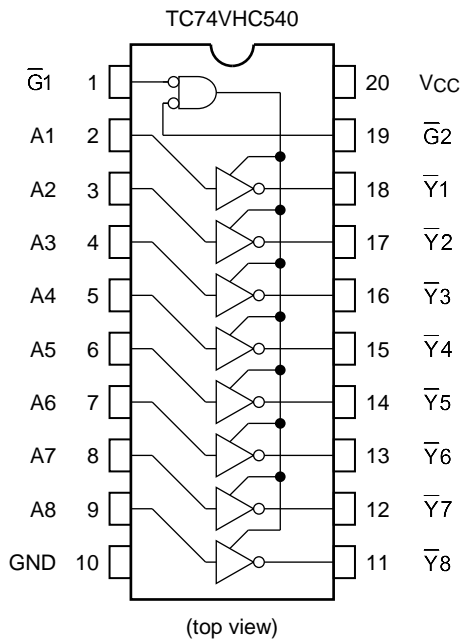


Weight

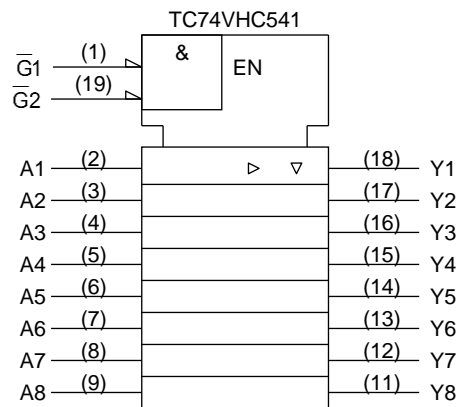
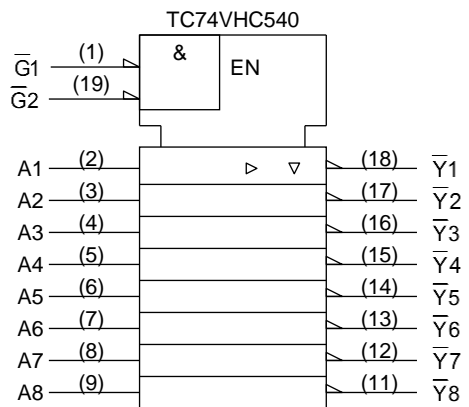
SOP20-P-300-1.27A : 0.22 g (typ.)
 VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Start of commercial production
 1991-05

Pin Assignment



IEC Logic Symbol



Truth Table

Inputs			Outputs	
$\bar{G}1$	$\bar{G}2$	A_n	Y_n	\bar{Y}_n
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

X: Don't care

Z: High impedance

Y_n : TC74VHC541

\bar{Y}_n : TC74VHC540

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	-20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	±25	mA
DC V _{CC} /ground current	I _{CC}	±75	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
 Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
 Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V _{CC} = 3.3 ± 0.3 V) 0 to 20 (V _{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device..
 Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V
Low-level input voltage	V _{IL}	—		2.0 3.0 to 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I _{OH} = -4 mA	3.0	2.58	—	—	2.48	—	
			I _{OH} = -8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
			I _{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit			
		VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max				
Propagation delay time (TC74VHC540)	t_{pLH}	—	3.3 ± 0.3	15	—	4.8	7.0	1.0	8.5	ns		
				50	—	7.3	10.5	1.0	12.0			
	t_{pHL}		5.0 ± 0.5	15	—	3.7	5.0	1.0	6.0			
				50	—	5.2	7.0	1.0	8.0			
Propagation delay time (TC74VHC541)	t_{pLH}	—	3.3 ± 0.3	15	—	5.0	7.0	1.0	8.5	ns		
				50	—	7.5	10.5	1.0	12.0			
	t_{pHL}		5.0 ± 0.5	15	—	3.5	5.0	1.0	6.0			
				50	—	5.0	7.0	1.0	8.0			
3-state output enable time	t_{pZL}	$R_L = 1 \text{ k}\Omega$	3.3 ± 0.3	15	—	6.8	10.5	1.0	12.5	ns		
				50	—	9.3	14.0	1.0	16.0			
	t_{pZH}		5.0 ± 0.5	15	—	4.7	7.2	1.0	8.5			
				50	—	6.2	9.2	1.0	10.5			
3-state output disable time	t_{pLZ}	$R_L = 1 \text{ k}\Omega$	3.3 ± 0.3	50	—	11.2	15.4	1.0	17.5	ns		
				t_{pHZ}	5.0 ± 0.5	50	—	6.0	8.8		1.0	10.0
Output to output skew	t_{osHL}		(Note 1)	3.3 ± 0.3		50	—	—	1.5		—	1.5
					t_{osLH}	5.0 ± 0.5	50	—	—		1.0	—
Input capacitance	C_{IN}	—		—	4		10	—	10	pF		
Output capacitance	C_{OUT}	—		—	6	—	—	—	pF			
Power dissipation capacitance (Note 2)	CPD	TC74VHC540			—	17	—	—	—	pF		
		TC74VHC541			—	18	—	—	—			

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

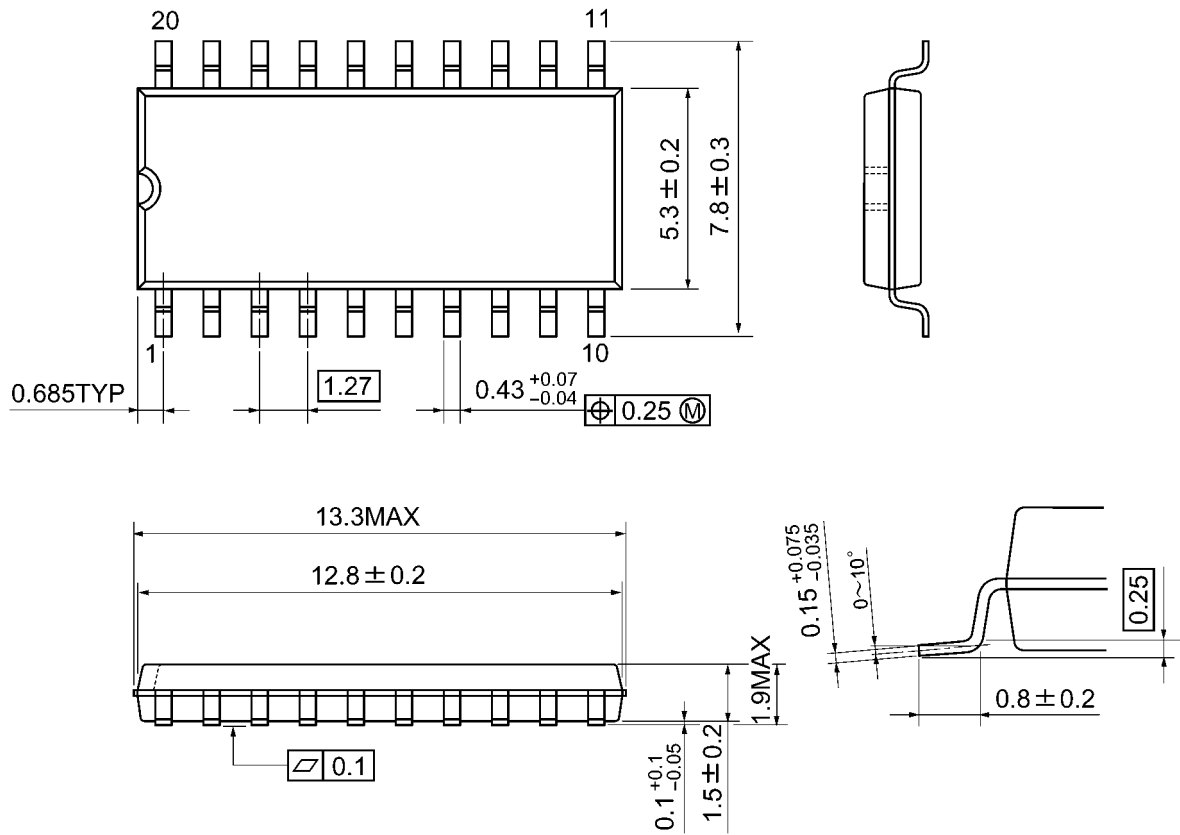
Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			VCC (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50 \text{ pF}$	5.0	0.7	1.0	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50 \text{ pF}$	5.0	-0.7	-1.0	V
Minimum high level dynamic input voltage	V_{IHD}	$C_L = 50 \text{ pF}$	5.0	—	3.5	V
Maximum low level dynamic input voltage	V_{ILD}	$C_L = 50 \text{ pF}$	5.0	—	1.5	V

Package Dimensions

SOP20-P-300-1.27A

Unit: mm

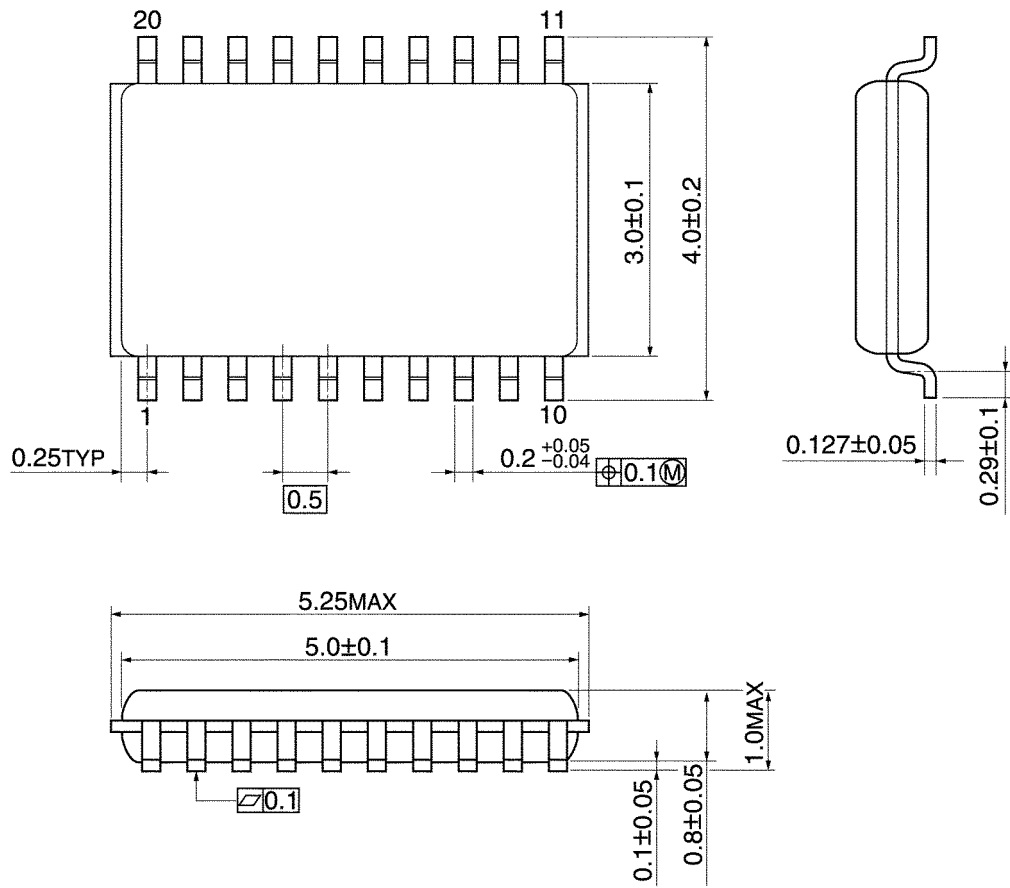


Weight: 0.22 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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