

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC240F, TC74VHC240FK TC74VHC244F, TC74VHC244FK

Octal Bus Buffer TC74VHC240F/FK

Inverted, 3-State Outputs

TC74VHC244F/FK

Non-Inverted, 3-State Outputs

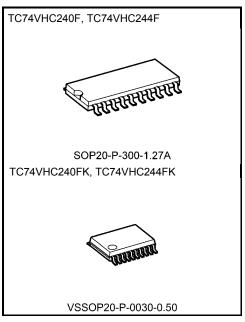
The TC74VHC240 and 244 are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate  $\rm C^2MOS$  technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The 74VHC240 is an inverting 3-state buffer having two active-low output enables. The TC74VHC244 is a non-inverting 3-state buffer, and has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.



Weight

SOP20-P-300-1.27A : 0.22 g (typ.) VSSOP20-P-0030-0.50 : 0.03 g (typ.)

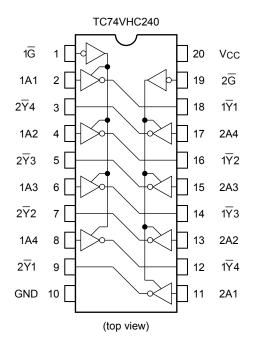
#### **Features**

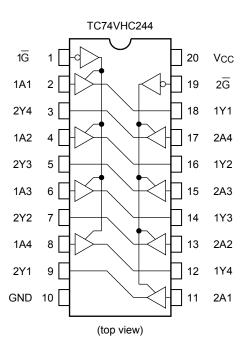
- High speed:  $t_{pd} = 3.9 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu A \text{ (max)}$  at  $T_a = 25 \text{°C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: VCC (opr) = 2 to 5.5 V
- Low noise: VOLP = 0.8 V (max)
- Pin and function compatible with 74ALS240/244

Start of commercial production 1991-05

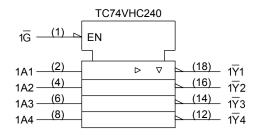


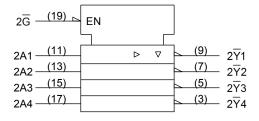
#### **Pin Assignment**

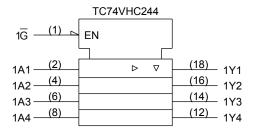


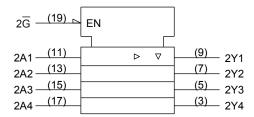


## **IEC Logic Symbol**









#### **Truth Table**

Inputs		Outputs			
G	An	Yn	$\overline{Y}_{n}$		
L	L	L	Н		
L	Н	Н	L		
Н	Х	Z	Z		

X: Don't care

Z: High impedance

Yn: TC74VHC244

₹<sub>n</sub>: TC74VHC240

2019-01-31



### **Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	Vcc	−0.5 to 7.0	V
DC input voltage	VIN	−0.5 to 7.0	V
DC output voltage	Vout	-0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	lıĸ	-20	mA
Output diode current	Іок	±20	mA
DC output current	lout	±25	mA
DC Vcc/ground current	Icc	±75	mA
Power dissipation	PD	180	mW
Storage temperature	T <sub>stg</sub>	–65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

#### **Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	Vcc	2.0 to 5.5	V
Input voltage	VIN	0 to 5.5	V
Output voltage	Vout	0 to VCC	V
Operating temperature	Topr	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V <sub>CC</sub> = $3.3 \pm 0.3$ V) 0 to 20 (V <sub>CC</sub> = $5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.



#### **Electrical Characteristics**

#### **DC Characteristics**

Characteristics	Symbol	-	Test Condition		Ta = 25°C		Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	
High-level input voltage	VIH	_		2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7			1.50 V <sub>CC</sub> × 0.7		V
Low-level input voltage	VIL	_		2.0 3.0 to 5.5			0.50 V <sub>CC</sub> × 0.3		0.50 V <sub>CC</sub> × 0.3	V
	VIN = VIH or VII	Ι <sub>ΟΗ</sub> = -50 μΑ	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V	
		- VIH OI VIL	$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94	_	_	2.48 3.80		
Low-level output voltage	V <sub>OL</sub>	VIN = VIH or VIL	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1	_ 	0.1 0.1 0.1	V
			$I_{OL} = 8 \text{ mA}$	4.5			0.36	_	0.44	
3-state output off- state current	loz	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	_	_	±0.25	_	±2.50	μА
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5	_		±0.1		±1.0	μА
Quiescent supply current	Icc	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	_		4.0	—	40.0	μА



# AC Characteristics (input: tr = tf = 3 ns)

Characteristics Symbol		Tes	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
511di dotoniodo			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Тур.	Max	Min	Max	<b>5</b> 1t
			3.3 ± 0.3	15	_	5.3	7.5	1.0	9.0	
Propagation delay time	tpLH			50	_	7.8	11.0	1.0	12.5	
(TC74VHC240)	tpHL	_	5.0 ± 0.5	15	_	3.6	5.5	1.0	6.5	ns
			5.0 ± 0.5	50	_	5.1	7.5	1.0	8.5	
			3.3 ± 0.3	15	_	5.8	8.4	1.0	10.0	
Propagation delay time	tpLH		3.3 ± 0.3	50	_	8.3	11.9	1.0	13.5	ne
(TC74VHC244)	tpHL	_	5.0 ± 0.5	15	_	3.9	5.5	1.0	6.5	ns
			5.0 ± 0.5	50	_	5.4	7.5	1.0	8.5	
	t <sub>P</sub> ZL	$R_L = 1 \text{ k}\Omega$	3.3 ± 0.3	15	_	6.6	10.6	1.0	12.5	- ns
3-state output enable				50	_	9.1	14.1	1.0	16.0	
	tpZH		5.0 ± 0.5	15	_	4.7	7.3	1.0	8.5	
				50	_	6.2	9.3	1.0	10.5	
3-state output disable	t <sub>pLZ</sub>	$R_{l} = 1 k\Omega$	$3.3 \pm 0.3$	50	_	10.3	14.0	1.0	16.0	ns
time	$t_{pHZ}$	KT = 1 K75	$5.0 \pm 0.5$	50	_	6.7	9.2	1.0	10.5	115
Output to output skew	t <sub>osLH</sub>	(Note 1)	$3.3 \pm 0.3$	50	_	_	1.5	_	1.5	ns
Output to output skew	t <sub>osHL</sub>	(Note 1)	$5.0 \pm 0.5$	50	_	_	1.0	_	1.0	115
Input capacitance	C <sub>IN</sub>				_	4	10	_	10	pF
Output capacitance	Cout		_			6	_	_		pF
Power dissipation	0	TC74VHC240		_	17	_	_	_	pF	
capacitance (Note 2)			244			19	_			

Note 1: Parameter guaranteed by design.

tosLH = |tpLHm - tpLHn|, tosHL = |tpHLm - tpHLn|

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

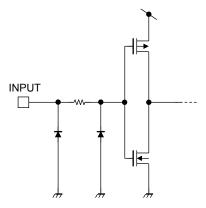
ICC (opr) = CPD·VCC·fIN + ICC / 8 (per bit)

#### Noise Characteristics (input: tr = tf = 3 ns)

Characteristics	Ol	Test Condition	Ta =	l lait		
Characteristics	Symbol		Vcc (V)	Тур.	Limit	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.5	-0.8	٧
Minimum high level dynamic input voltage	VIHD	C <sub>L</sub> = 50 pF	5.0	_	3.5	٧
Maximum low level dynamic input voltage	VILD	C <sub>L</sub> = 50 pF	5.0	_	1.5	V



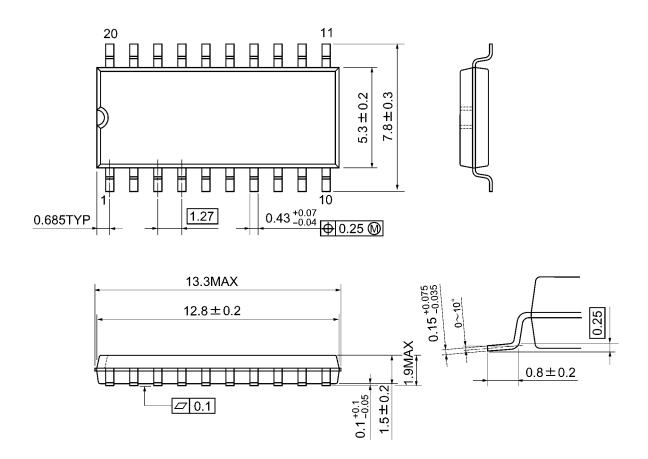
# **Input Equivalent Circuit**





# **Package Dimensions**

SOP20-P-300-1.27A Unit: mm



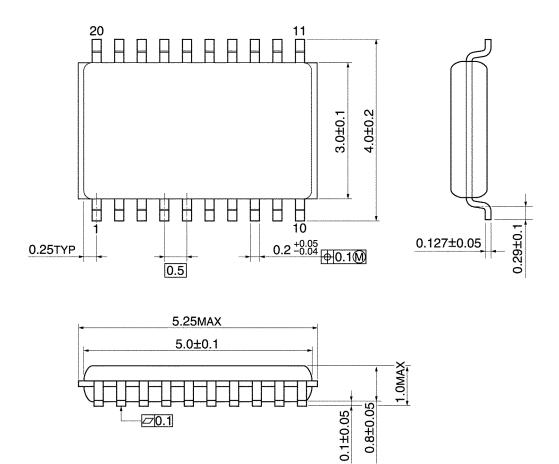
Weight: 0.22 g (typ.)

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# **Package Dimensions**

VSSOP20-P-0030-0.50 Unit: mm



Weight: 0.03 g (typ.)



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