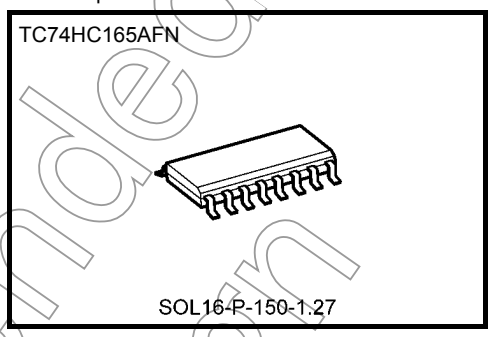
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC165AFN

8-Bit Shift Register (P-IN, S-OUT)

Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight
SOL16-P-150-1.27 : 0.13 g (typ.)

The TC74HC165A is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock inputs. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight frip-frops perform serial shifting with each clock pulse.

When the SHIFT/$\overline{\text{LOAD}}$ input is held low, the parallel data is loaded asynchronously into the register at positive going transition of the clock pulse.

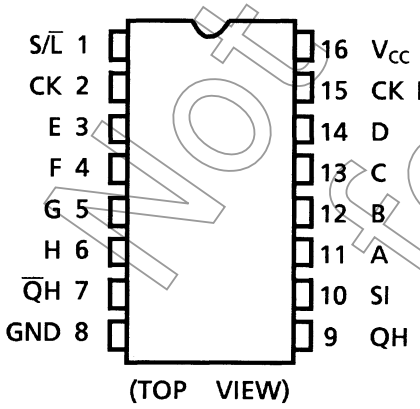
The CK-INH input should be shifted high only when the CK input is held high.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

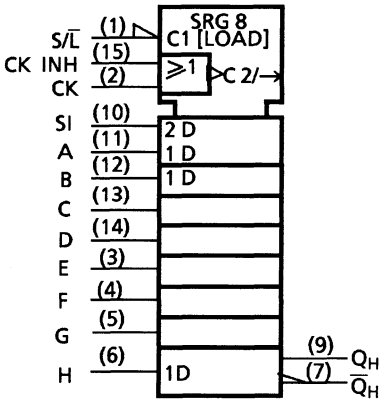
Features

- High speed: f_{max} = 56 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS165

Pin Assignment



IEC Logic Symbol



Truth Table

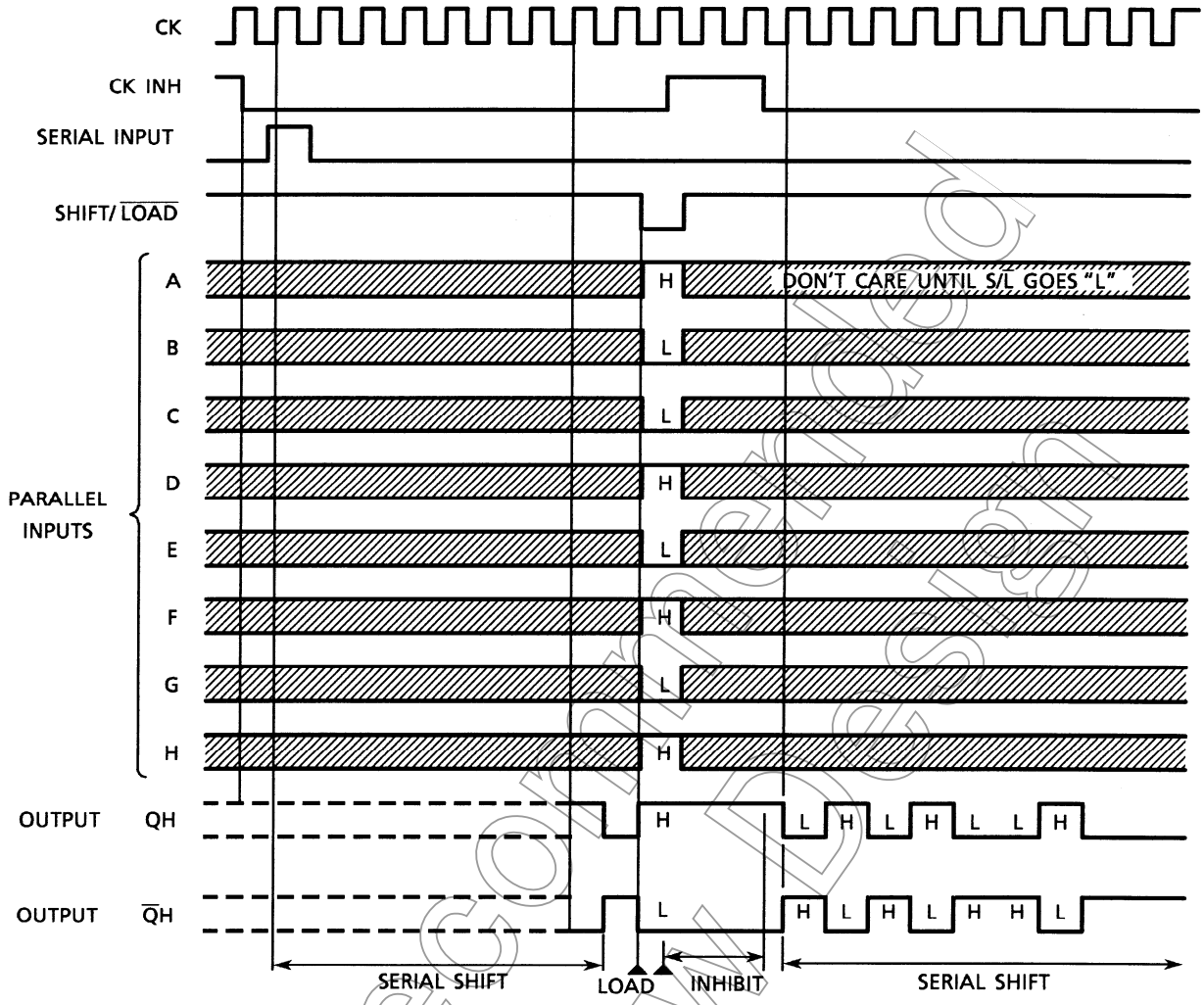
Inputs					Internal Outputs		Outputs	
SHIFT/$\overline{\text{LOAD}}$	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A·····H	QA	QB	QH	$\overline{\text{QH}}$
L	X	X	X	a·····h	a	b	h	$\overline{\text{h}}$
H	L	↑	H	X	H	QAn	QGn	$\overline{\text{QGn}}$
H	L	↑	L	X	L	QAn	QGn	$\overline{\text{QGn}}$
H	↑	L	H	X	H	QAn	QGn	$\overline{\text{QGn}}$
H	↑	L	L	X	L	QAn	QGn	$\overline{\text{QGn}}$
H	X	H	X	X	No Change			
H	H	X	X	X	No Change			

X: Don't care

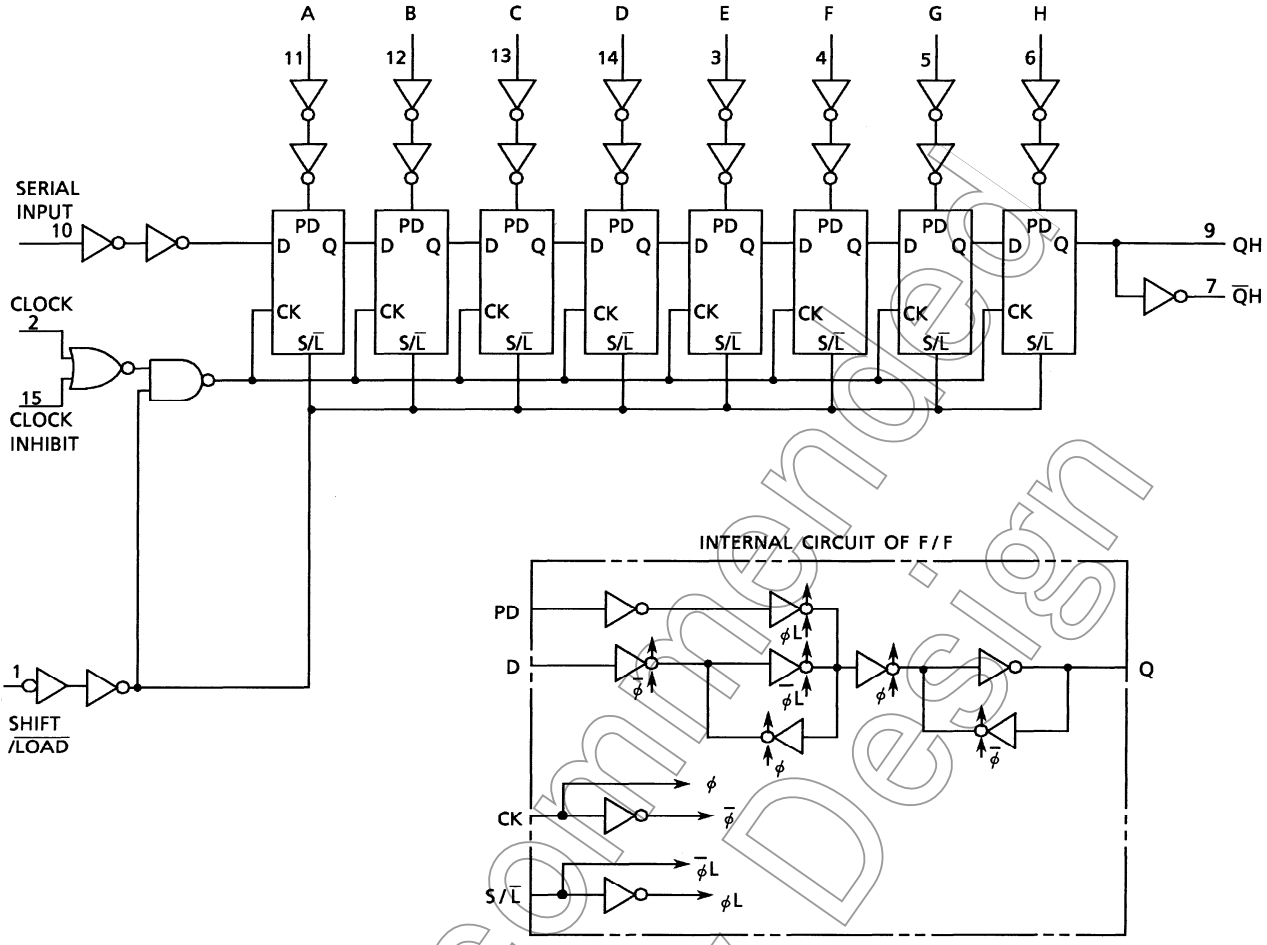
a·····h: The level of steady state input voltage at inputs A through H respectively

QAn~QGn: The level of QA~QG, respectively, before the most recent positive transition of the CK.

Timing Chart



System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
				V_{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK, CK INH)	$t_{W(H)}$ $t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($S/\overline{L}$)	$t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (PI- $S/\overline{L}$)	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (SI-CK, CK INH)	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ($S/\overline{L}$ -CK, CK INH)	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time (PI- $S/\overline{L}$)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time (SI-CK, CK INH)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time ($S/\overline{L}$ -CK, CK INH)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time (CK INH-CK) (CK-CK INH)	t_{rem}	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Clock frequency	f	—	2.0	—	7	6	MHz
			4.5	—	30	24	
			6.0	—	41	28	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (CK, CK INH-QH, $\overline{Q}$H)	t_{pLH} t_{pHL}	—	—	15	25	ns
Propagation delay time ($S/\overline{L}$ -QH, $\overline{Q}$H)	t_{pLH} t_{pHL}	—	—	15	25	ns
Propagation delay time (H-QH, $\overline{Q}$H)	t_{pLH} t_{pHL}	—	—	14	26	ns
Maximum clock frequency	f_{max}	—	35	56	—	MHz

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	25	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CK, CK INH-QH, $\overline{Q}$H)	t_{pLH} t_{pHL}	—	2.0	—	55	150	—	190	ns
			4.5	—	18	30	—	38	
			6.0	—	15	26	—	33	
Propagation delay time (S/$\overline{L}$ -QH, $\overline{Q}$H)	t_{pLH} t_{pHL}	—	2.0	—	60	165	—	205	ns
			4.5	—	19	33	—	41	
			6.0	—	16	28	—	35	
Propagation delay time (H-QH, $\overline{Q}$H)	t_{pHL}	—	2.0	—	52	135	—	170	ns
			4.5	—	17	27	—	34	
			6.0	—	14	23	—	29	
Maximum clock frequency	f_{max}	—	2.0	7	14	—	6	—	MHz
			4.5	30	46	—	24	—	
			6.0	41	65	—	28	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—		—	55	—	—	—	pF

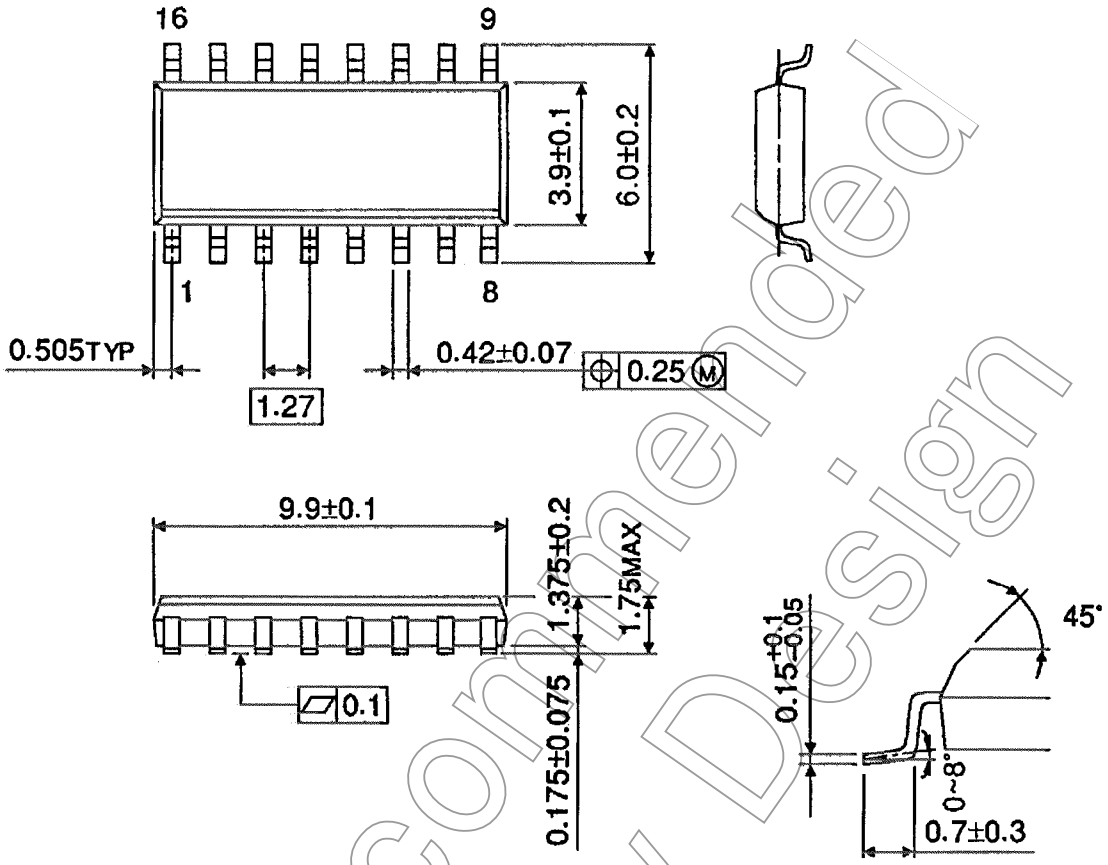
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions (Note)

SOL16-P-150-1.27 Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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