

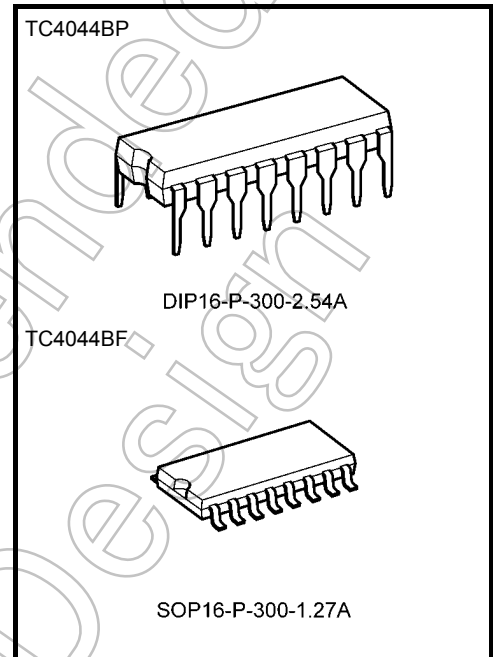
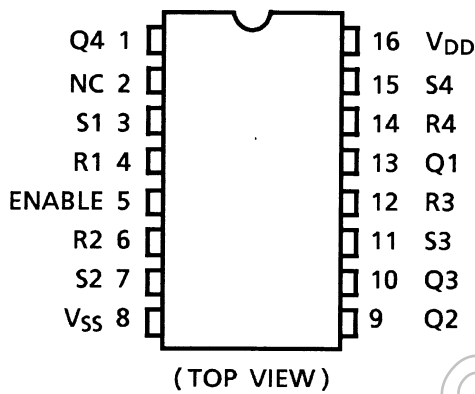
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4044BP, TC4044BF

TC4044B Quad 3-State R/S Latch
(quad NAND R/S latch)

TC4044B the latches composed by four independent R/S flip-flop circuits. TC4044B fabricated with NAND gates is suitable for data processing of four bits configuration. Four output lines can have high impedance regardless of the contents of latches by means of common ENABLE input to make connection to the bus lines easy.

Pin Assignment



Weight
 DIP16-P-300-2.54A : 1.00 g (typ.)
 SOP16-P-300-1.27A : 0.18 g (typ.)

Truth Table

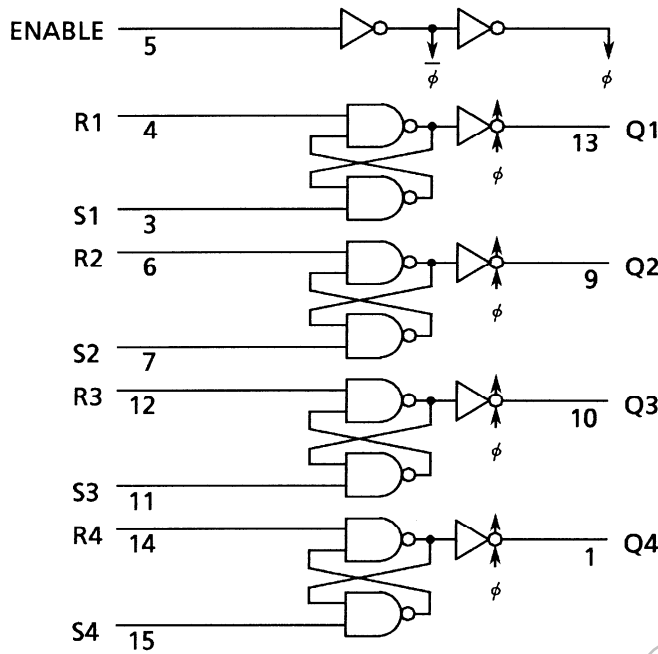
R	S	E	Q
*	*	L	HZ
L	L	H	L
L	H	H	L
H	L	H	H
H	H	H	No Change

*: Don't care

HZ: High impedance

Start of commercial production
1978-04

Logic Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	$V_{SS} - 0.5$ to $V_{SS} + 20$	V
Input voltage	V_{IN}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Output voltage	V_{OUT}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
DC input current	I_{IN}	± 10	mA
Power dissipation	P_D	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T_{opr}	-40 to 85	$^{\circ}C$
Storage temperature range	T_{stg}	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges ($V_{SS} = 0$ V) (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	V_{DD}	—	3	—	18	V
Input voltage	V_{IN}	—	0	—	V_{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{DD} or V_{SS} .

Static Electrical Characteristics (V_{SS} = 0 V)

Characteristics	Sym- bol	Test Condition	V _{DD} (V)	-40°C		25°C			85°C		Unit	
				Min	Max	Min	Typ.	Max	Min	Max		
High-level output voltage	V _{OH}	I _{OUT} < 1 μA V _{IN} = V _{SS} , V _{DD}	5	4.95	—	4.95	5.00	—	4.95	—	V	
			10	9.95	—	9.95	10.00	—	9.95	—		
			15	14.95	—	14.95	15.00	—	14.95	—		
Low-level output voltage	V _{OL}	I _{OUT} < 1 μA V _{IN} = V _{SS} , V _{DD}	5	—	0.05	—	0.00	0.05	—	0.05	V	
			10	—	0.05	—	0.00	0.05	—	0.05		
			15	—	0.05	—	0.00	0.05	—	0.05		
Output high current	I _{OH}	V _{OH} = 4.6 V V _{OH} = 2.5 V V _{OH} = 9.5 V V _{OH} = 13.5 V V _{IN} = V _{SS} , V _{DD}	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA	
			5	-2.50	—	-2.10	-4.0	—	-1.70	—		
			10	-1.50	—	-1.30	-2.2	—	-1.10	—		
			15	-4.00	—	-3.40	-9.0	—	-2.80	—		
			—	—	—	—	—	—	—	—		—
Output low current	I _{OL}	V _{OL} = 0.4 V V _{OL} = 0.5 V V _{OL} = 1.5 V V _{IN} = V _{SS} , V _{DD}	5	0.61	—	0.51	1.2	—	0.42	—	mA	
			10	1.50	—	1.3	3.2	—	1.10	—		
			15	4.00	—	3.4	12.0	—	2.80	—		
			—	—	—	—	—	—	—	—		—
			—	—	—	—	—	—	—	—		—
Input high voltage	V _{IH}	V _{OUT} = 0.5 V, 4.5 V V _{OUT} = 1.0 V, 9.0 V V _{OUT} = 1.5 V, 13.5 V I _{OUT} < 1 μA	5	3.5	—	3.5	2.75	—	3.5	—	V	
			10	7.0	—	7.0	5.50	—	7.0	—		
			15	11.0	—	11.0	8.25	—	11.0	—		
			—	—	—	—	—	—	—	—		—
Input low voltage	V _{IL}	V _{OUT} = 0.5 V, 4.5 V V _{OUT} = 1.0 V, 9.0 V V _{OUT} = 1.5 V, 13.5 V I _{OUT} < 1 μA	5	—	1.5	—	2.25	1.5	—	1.5	V	
			10	—	3.0	—	4.50	3.0	—	3.0		
			15	—	4.0	—	6.75	4.0	—	4.0		
			—	—	—	—	—	—	—	—		—
Input current	"H" level	I _{IH}	V _{IH} = 18 V	18	—	0.1	—	10 ⁻⁵	0.1	—	1.0	μA
	"L" level	I _{IL}	V _{IL} = 0 V	18	—	-0.1	—	-10 ⁻⁵	-0.1	—	-1.0	
3-state output leakage current	"H" level	I _{DH}	V _{OH} = 18 V	18	—	0.4	—	10 ⁻⁴	0.4	—	12	μA
	"L" level	I _{DL}	V _{OL} = 0 V	18	—	-0.4	—	-10 ⁻⁴	-0.4	—	-12	
Quiescent supply current	I _{DD}	V _{IN} = V _{SS} , V _{DD} (Note)	5	—	1	—	0.002	1	—	30	μA	
			10	—	2	—	0.004	2	—	60		
			15	—	4	—	0.008	4	—	120		

Note: All valid input combinations.

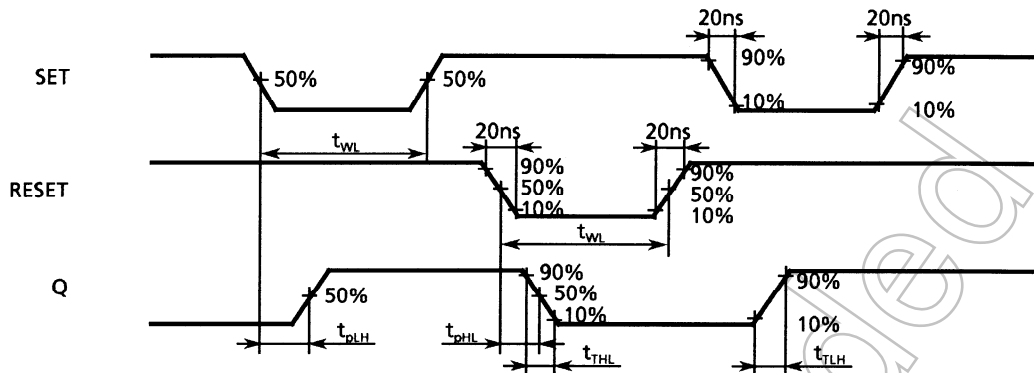
Dynamic Electrical Characteristics (Ta = 25°C, VSS = 0 V, CL = 50 pF)

Characteristics	Symbol	Test Condition	VDD (V)	Min	Typ.	Max	Unit
Output transition time (low to high)	t _{TLH}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output transition time (high to low)	t _{THL}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Propagation delay time (SET, RESET-Q)	t _{pLH} t _{pHL}	—	5	—	90	300	ns
			10	—	45	140	
			15	—	35	100	
3-state propagation delay time (ENABLE-Q)	t _{pHZ} t _{pLZ}	R _L = 1 kΩ	5	—	55	180	ns
			10	—	35	100	
			15	—	30	70	
3-state propagation delay time (ENABLE-Q)	t _{pZH} t _{pZL}	R _L = 1 kΩ	5	—	55	180	ns
			10	—	30	100	
			15	—	25	70	
Min pulse width (SET, RESET)	t _{WL}	—	5	—	25	160	ns
			10	—	20	80	
			15	—	20	40	
Input capacitance	C _{IN}	—	—	5	7.5	pF	

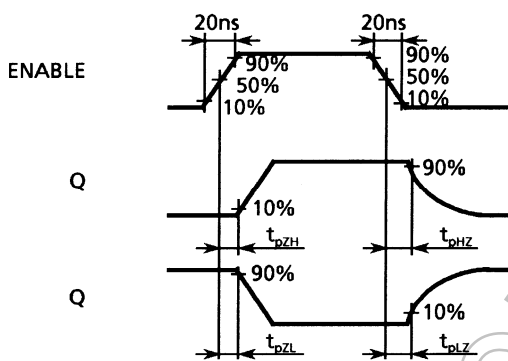
Not Recommended for New Design

Waveforms for Measurement of Dynamic Characteristics

Waveform 1



Waveform 2

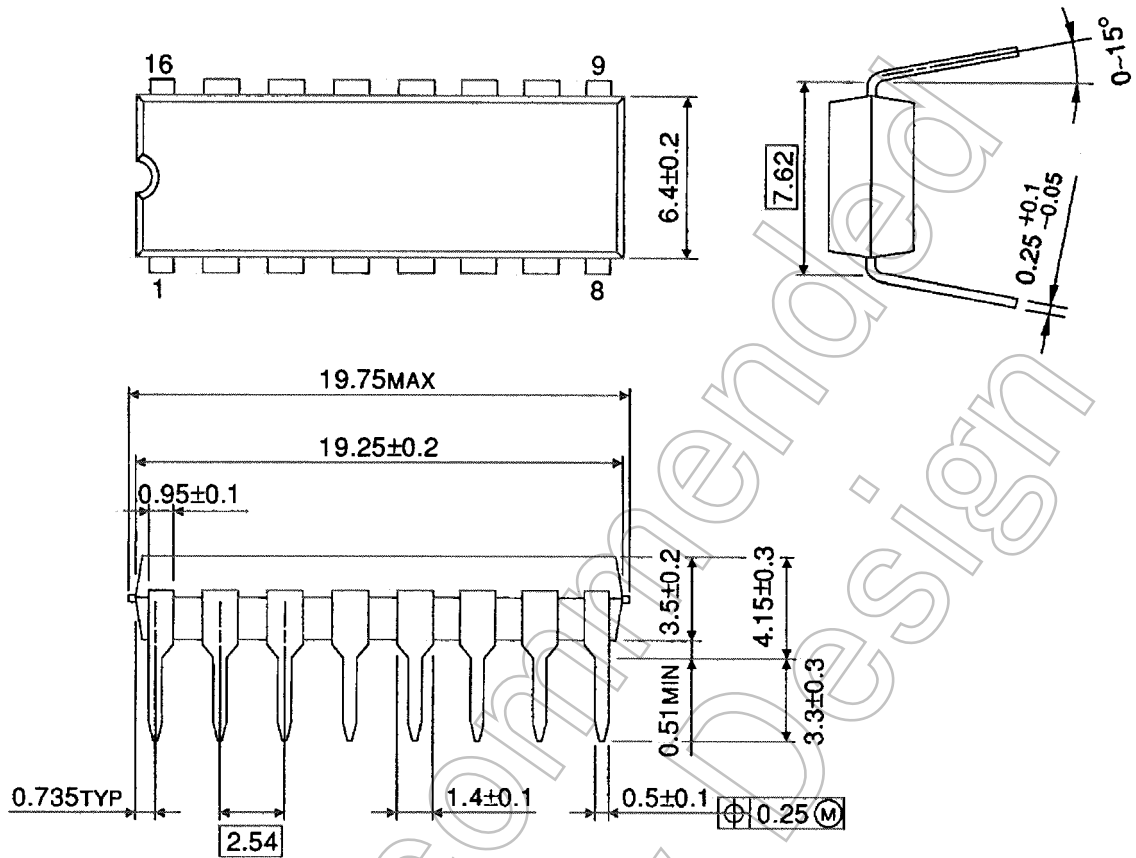


Not Recommended for New Design

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

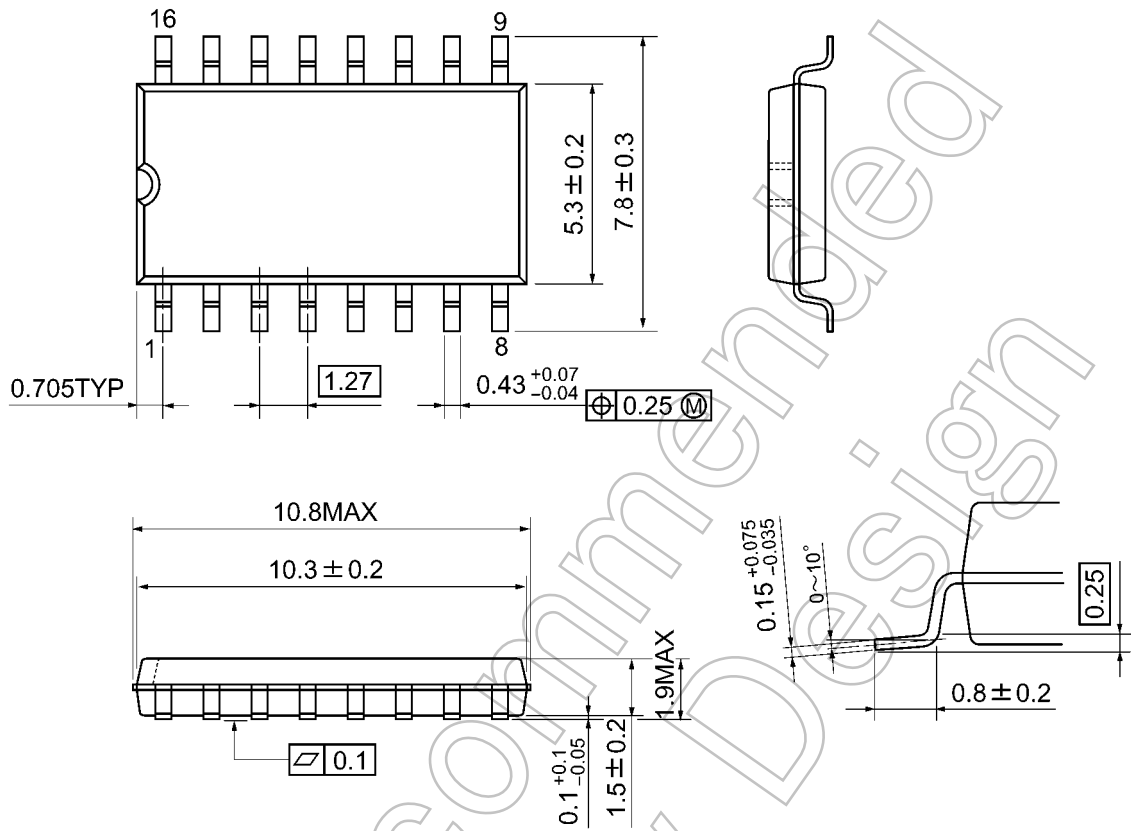


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Not Recommended for New Design

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