TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM12GZ47, SM12JZ47, SM12GZ47A, SM12JZ47A

AC POWER CONTROL APPLICATIONS

Repetitive Peak off-State Voltage : VDRM = 400V, 600V
 R.M.S On-State Current : IT (RMS) = 12A

• High Commutating (dv / dt)

• Isolation Voltage : $V_{Isol} = 1500V AC$

ABSOLUTE MAXIMUM RATINGS

CHARACTERI	STIC	SYMBOL	RATING	THAU
Repetitive Peak Off-State Voltage and	SM12GZ47 SM12GZ47A	V _{DRM}	400	
Repetitive Peak Reverse Voltage	SM12JZ47 SM12JZ47A	V DRM	600	
R. M. S. On-state Curre (Full Sine Waveform TC		I _{T (RMS)}	12	> A
Peak One Cylce Surge Current (Non-Repetitive		I _{TSM}	120 (50Hz) 132 (60Hz)	A
I ² t Limit Value		I ² t	72	A^2 s
Critical Rate of Rise of C Current	On-State (Note 1)	di / dt	50	A / µs
Peak Gate Power Dissip	ation	PGM	5	\ w
Average Gate Power Dis	ssipation	PG (AV)	0.5	W
Peak Gate Voltage		VĘGM	10	
Peak Gate Current		I _{GM}	(27)	\rightarrow A
Junction Temperature /) 	-40~125))	°C
Storage Temperature Ra	ange	T _{stg}	-40~125	°C
Isolation Voltage (AC, t	= 1min.)	V _{Isol}	1500	V

10.3MAX. 63.2±0.2

0.75±0.15

1. T1

2. T2

3. GATE

JEDEC

JEITA

TOSHIBA

13-10H1A

Unit: mm

Weight: 1.7 g (typ.)

Note 1: di / dt test condition

V_{DRM} = 0.5 × Rated

I_{TM}≤ 17A

t_{gw} ≥ 10µs

t_{ar}≤ 250ns∕

igp = 1GT × 2.0

Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

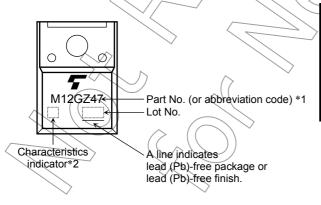
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



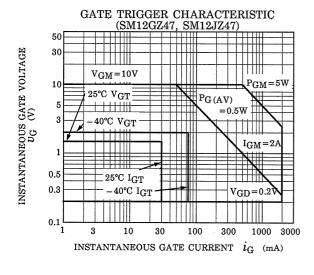
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

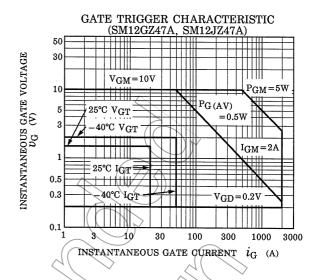
CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT		
Repetitive Peak	epetitive Peak Off-State Current I _{DRM} V _{DRM} = Rated			_	_	20	μA			
Gate Trigger Voltage		I	V _{GT}	V _D = 12V, R _L = 20Ω	T2 (+) , Gate (+)	_	_	1.5	· V	
		II			T2 (+) , Gate (-) <	//	_	1.5		
		III			T2 (-) , Gate (-)		_	1.5		
		IV			T2 (-) , Gate (+)	J)) >-	1		
						T2 (+), Gate (+)	\rightarrow	_	30	
		SM12GZ47 SM12JZ47	II		V _D = 12V, R _L = 20Ω	T2 (+), Gate (-)	\rightarrow	_	30	mA
	SM12		III			T2 (-) , Gate (-)	\ 	_	30	
Gate Trigger			IV	I _{GT}		T2 (-) , Gate (+)	_	_	_	
		SM12GZ47A SM12JZ47A	I	- 101		T2 (+), Gate (+)	_		20	
			II			T2 (+) , Gate (-)		4	20	
	SM12		III			T2 (-) , Gate (-)	-6	5-/	> 20	
			IV			T2 (-) , Gate (+)	\(\)	<u> </u>) —	
Peak On-State Voltage		V_{TM}	I _{TM} = 17A		X		1.5	V		
Gate Non-Trigger Voltage		$V_{\sf GD}$	V _D = Rated, Tc = 125°C		0.2	> _	-	V		
Holding Current		lΗ	$V_D = 12V$, $I_{TM} = 1A$			_	50	mA		
Thermal Resistance		R _{th (j-c)}	Junction to Case, AC			_	3.0	°C/W		
Critical Rate of Rise of Off-State		SM12GZ47 SM12JZ47		dv / dt	V _{DRM} = Rated, T _f = 125°C			300	1	· V / μs
Voltage	SM12GZ47 SM12JZ47		dvidi	Exponential Rise		_	200	_	ν / μο	
Rise of Off-State Voltage at		SM12GZ47 SM12JZ47		(dv \(\)dt) c	V _{DRM} = 400V, T _i = 125°C		10	_	_	V / 110
		SM12GZ47 SM12JZ47		(dv /dt) c	(di / dt) c = -6.5A / ms		4	_	_	V / μs

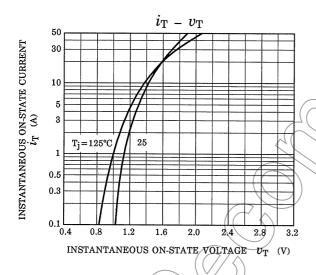
MARKING

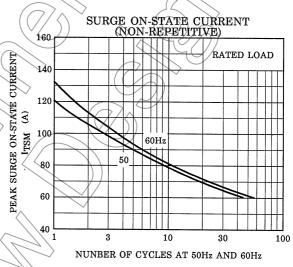


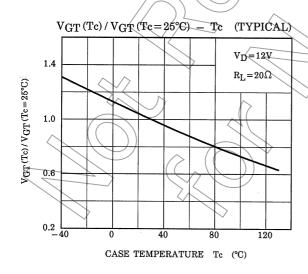
	Part No. (or abbreviation code)	Part No.
*1	M12GZ47	SM12GZ47, SM12GZ47A
	M12JZ47	SM12JZ47, SM12JZ47A
*2	Nothing	SM12GZ47, SM12JZ47
	A	SM12GZ47A, SM12JZ47A

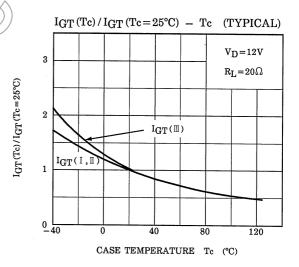


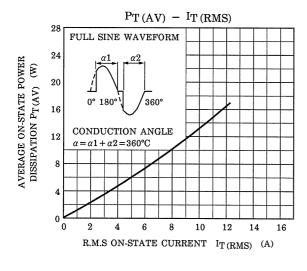


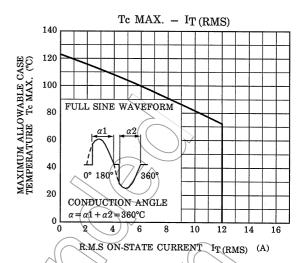


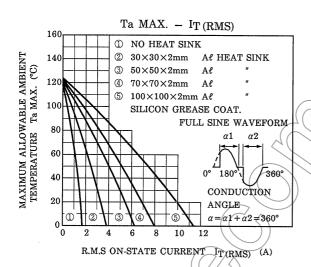


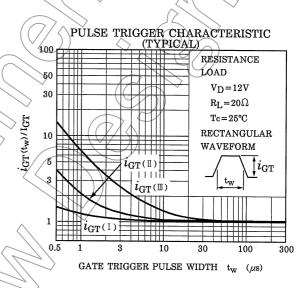


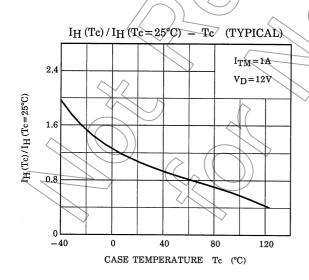


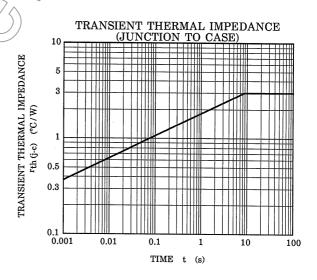














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