Unit: mm

**ANODE** N.C. CATHODE

TD-236MOD

SC-59 1-3G1B

TOSHIBA Diode Silicon Epitaxial Schottky Planar Type

# **1SS344**

# Ultra High Speed Switching Application

 $V_{F(3)} = 0.50V \text{ (typ.)}$ 

Low forward voltage Fast reverse recovery time  $: t_{rr} = 20 \text{ns}$  (typ.)

High average forward current  $: I_O = 0.5A \text{ (max)}$ 

# Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	$V_{RM}$	25	V
Reverse voltage	V <sub>R</sub>	20	$(\nearrow \land \land)$
Maximum (peak) forward current	I <sub>FM</sub>	1500	mA
Average forward current	Io	500	mΑ
Surge current (10ms)	I <sub>FSM</sub>	5	, <b>A</b>
Power dissipation	Р	200	mW
Junction temperature	Tj	125	°C
Storage temperature	T <sub>stg</sub>	-55~125	/°C
Operating Temperature	T <sub>opr</sub>	-40~100	<<°¢

Weight: 0.012g (typ.)

S-MINI

**JEDEC** 

TOSHIBA

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Note: Using continuously under heavy loads (e.g.) the application of high temperature/current/voltage and the significant change in

temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

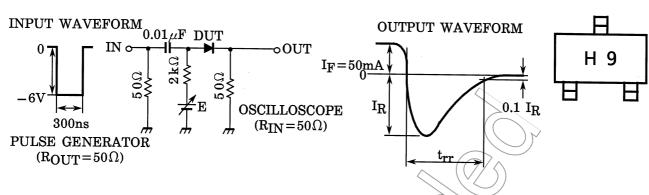
### Electrical Characteristics (Ta = 25°C)

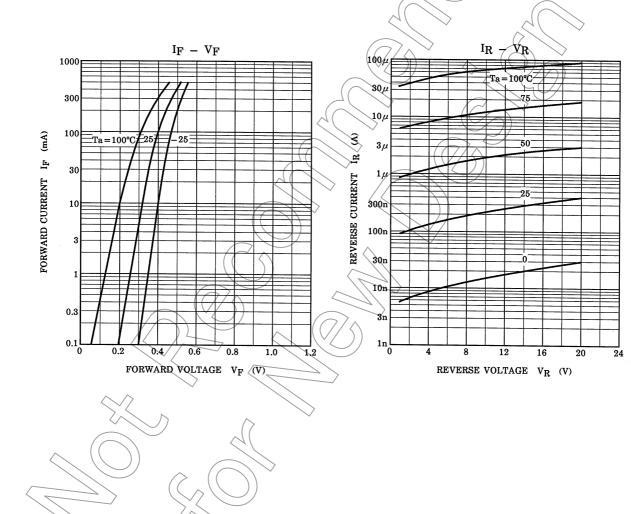
Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
	V <sub>F</sub> (†)	_	I <sub>F</sub> = 10mA	_	0.30	_	
Forward voltage	VF (2)	_	I <sub>F</sub> = 100mA	_	0.38	_	V
	VF (3)	_	I <sub>F</sub> = 500mA	_	0.50	0.55	
Reverse current	(IR (1)	_	V <sub>R</sub> = 10V	_	_	20	
Trevelse-Current	IR (2)	_	V <sub>R</sub> = 20V	1	_	100	μA
Total capacitance	√ C <sub>T</sub>	_	V <sub>R</sub> = 0, f = 1MHz	_	120	_	pF
Reverse recovery time	t <sub>rr</sub>	_	I <sub>F</sub> = 50mA, (Fig.1)	-	20	_	ns

# Fig.1 Reverse Recovery Time (t<sub>rr</sub>)

# **Test Circuit**

# Marking





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