

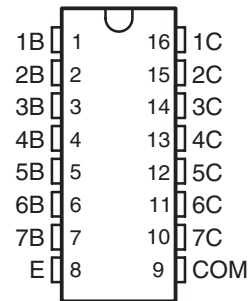
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

 Check for Samples: [ULN2002A](#), [ULN2003A](#), [ULN2003AI](#), [ULN2004A](#), [ULQ2003A](#), [ULQ2004A](#)

FEATURES

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

ULN2002A . . . N PACKAGE
 ULN2003A . . . D, N, NS, OR PW PACKAGE
 ULN2004A . . . D, N, OR NS PACKAGE
 ULQ2003A, ULQ2004A . . . D OR N PACKAGE
 (TOP VIEW)



DESCRIPTION

The ULN2002A, ULN2003A, ULN2003AI, ULN2004A, ULQ2003A, and ULQ2004A are high-voltage high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions of the ULN2003A and ULN2004A, see the [SN75468](#) and [SN75469](#), respectively.

The ULN2002A is designed specifically for use with 14-V to 25-V PMOS devices. Each input of this device has a Zener diode and resistor in series to control the input current to a safe limit. The ULN2003A and ULQ2003A have a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A and ULQ2004A have a 10.5-k Ω series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULN/ULQ2004A is below that of the ULN/ULQ2003A, and the required voltage is less than that required by the ULN2002A.



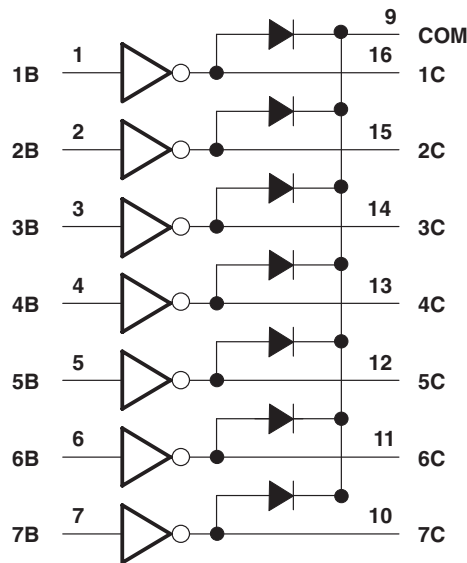
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ORDERING INFORMATION⁽¹⁾

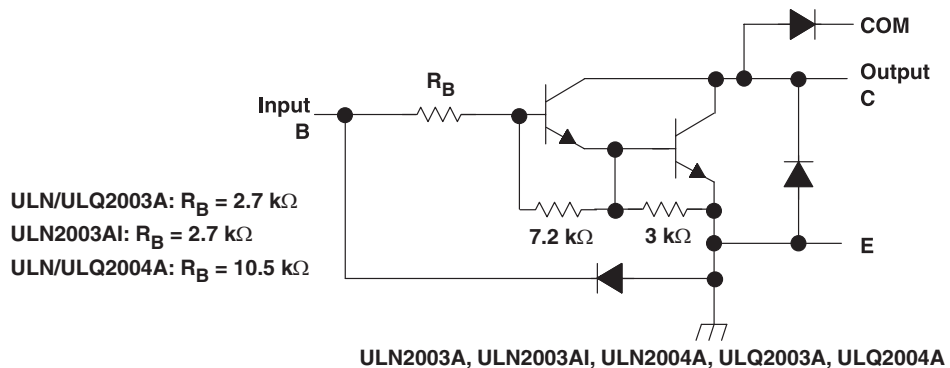
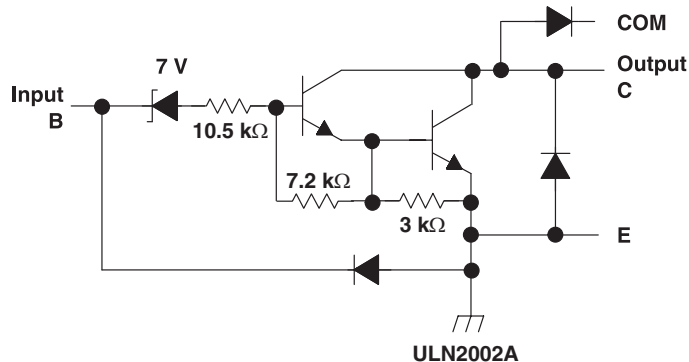
| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –20°C to 70°C | PDIP – N | Tube of 25 | ULN2002AN | ULN2002AN |
| | | | ULN2003AN | ULN2003AN |
| | | | ULN2004AN | ULN2004AN |
| | SOIC – D | Tube of 40 | ULN2003AD | ULN2003A |
| | | | ULN2003ADR | |
| | | Reel of 2500 | ULN2003ADRG3 | ULN2004A |
| | | | ULN2004AD | |
| | | Reel of 2500 | ULN2004ADRG3 | |
| | SOP – NS | Reel of 2000 | ULN2003ANSR | ULN2003A |
| | | | ULN2004ANSR | ULN2004A |
| TSSOP – PW | Tube of 90 | ULN2003APW | UN2003A | |
| | Reel of 2000 | ULN2003APWR | | |
| –40°C to 85°C | PDIP – N | Tube of 25 | ULQ2003AN | ULQ2003A |
| | | | ULQ2004AN | ULQ2004AN |
| | SOIC – D | Tube of 40 | ULQ2003AD | ULQ2003A |
| | | | ULQ2003ADR | |
| | | Reel of 2500 | ULQ2004AD | ULQ2004A |
| | | | ULQ2004ADR | |
| –40°C to 105°C | SOP – NS | Reel of 2000 | ULN2003AINSR | ULN2003AI |
| | PDIP – N | Tube of 425 | ULN2003AIN | ULN2003AIN |
| | SOIC – D | Tube of 40 | ULN2003AID | ULN2003AI |
| | | Reel of 2500 | ULN2003AIDR | |
| | TSSOP – PW | Reel of 2500 | ULN2003AIPWR | UN2003AI |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

LOGIC DIAGRAM



SCHEMATICS (EACH DARLINGTON PAIR)



ULN/ULQ2003A: $R_B = 2.7 \text{ k}\Omega$
 ULN2003AI: $R_B = 2.7 \text{ k}\Omega$
 ULN/ULQ2004A: $R_B = 10.5 \text{ k}\Omega$

All resistor values shown are nominal.

The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

at 25°C free-air temperature (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|------------------|--|-----------------------------|------|--------|------|
| V _{CC} | Collector-emitter voltage | | 50 | V | |
| | Clamp diode reverse voltage ⁽²⁾ | | 50 | V | |
| V _I | Input voltage ⁽²⁾ | | 30 | V | |
| | Peak collector current | See Figure 14 and Figure 15 | | 500 mA | |
| I _{OK} | Output clamp current | | 500 | mA | |
| | Total emitter-terminal current | | –2.5 | A | |
| T _A | Operating free-air temperature range | ULN200xA | –20 | 70 | °C |
| | | ULN200xAI | –40 | 105 | |
| | | ULQ200xA | –40 | 85 | |
| | | ULQ200xAI | –40 | 105 | |
| θ _{JA} | Package thermal impedance ^{(3) (4)} | D package | | 73 | °C/W |
| | | N package | | 67 | |
| | | NS package | | 64 | |
| | | PW package | | 108 | |
| θ _{JC} | Package thermal impedance ^{(5) (6)} | D package | | 36 | |
| | | N package | | 54 | |
| T _J | Operating virtual junction temperature | | 150 | °C | |
| | Lead temperature for 1.6 mm (1/16 inch) from case for 10 seconds | | 260 | °C | |
| T _{stg} | Storage temperature range | –65 | 150 | °C | |

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
- Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- The package thermal impedance is calculated in accordance with JESD 51-7.
- Maximum power dissipation is a function of T_J(max), θ_{JC}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/θ_{JC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- The package thermal impedance is calculated in accordance with MIL-STD-883.

ELECTRICAL CHARACTERISTICS

T_A = 25°C

| PARAMETER | TEST FIGURE | TEST CONDITIONS | ULN2002A | | | UNIT |
|----------------------|-------------|---|----------|------|------|------|
| | | | MIN | TYP | MAX | |
| V _{I(on)} | Figure 6 | V _{CE} = 2 V, I _C = 300 mA | | 13 | | V |
| V _{CE(sat)} | Figure 4 | I _I = 250 μA, I _C = 100 mA | | 0.9 | 1.1 | V |
| | | I _I = 350 μA, I _C = 200 mA | | 1 | 1.3 | |
| | | I _I = 500 μA, I _C = 350 mA | | 1.2 | 1.6 | |
| V _F | Figure 7 | I _F = 350 mA | | 1.7 | 2 | V |
| I _{CEX} | Figure 1 | V _{CE} = 50 V, I _I = 0 | | 50 | | μA |
| | Figure 2 | V _{CE} = 50 V, T _A = 70°C, I _I = 0, V _I = 6 V | | 100 | 500 | |
| I _{I(off)} | Figure 2 | V _{CE} = 50 V, I _C = 500 μA | 50 | 65 | | μA |
| I _I | Figure 3 | V _I = 17 V | | 0.82 | 1.25 | mA |
| I _R | Figure 6 | V _R = 50 V, T _A = 70°C | | 100 | | μA |
| | | | | 50 | | |
| C _i | | V _I = 0, f = 1 MHz | | 25 | | pF |

ELECTRICAL CHARACTERISTICS
 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST FIGURE | TEST CONDITIONS | | ULN2003A | | | ULN2004A | | | UNIT |
|---|-------------|---|--------------------------|----------|------|-----|----------|------|---------------|---------------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{I(\text{on})}$ On-state input voltage | Figure 6 | $V_{CE} = 2\text{ V}$ | $I_C = 125\text{ mA}$ | | | | | | 5 | V |
| | | | $I_C = 200\text{ mA}$ | | | | | | 2.4 | |
| | | | $I_C = 250\text{ mA}$ | | | | | | 2.7 | |
| | | | $I_C = 275\text{ mA}$ | | | | | | 7 | |
| | | | $I_C = 300\text{ mA}$ | | | | | | 3 | |
| | | | $I_C = 350\text{ mA}$ | | | | | | | |
| $V_{CE(\text{sat})}$ Collector-emitter saturation voltage | Figure 5 | $I_I = 250\ \mu\text{A}$, $I_C = 100\text{ mA}$ | | 0.9 | 1.1 | | 0.9 | 1.1 | V | |
| | | $I_I = 350\ \mu\text{A}$, $I_C = 200\text{ mA}$ | | 1 | 1.3 | | 1 | 1.3 | | |
| | | $I_I = 500\ \mu\text{A}$, $I_C = 350\text{ mA}$ | | 1.2 | 1.6 | | 1.2 | 1.6 | | |
| I_{CEX} Collector cutoff current | Figure 1 | $V_{CE} = 50\text{ V}$, $I_I = 0$ | | | | | | 50 | μA | |
| | Figure 2 | $V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$ | $I_I = 0$ | | | | | 100 | | |
| V_F Clamp forward voltage | Figure 8 | $I_F = 350\text{ mA}$ | | | 1.7 | 2 | | 1.7 | 2 | V |
| $I_{I(\text{off})}$ Off-state input current | Figure 3 | $V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$ | $I_C = 500\ \mu\text{A}$ | 50 | 65 | | 50 | 65 | | μA |
| I_I Input current | Figure 4 | $V_I = 3.85\text{ V}$ | | 0.93 | 1.35 | | | | | mA |
| | | $V_I = 5\text{ V}$ | | | | | 0.35 | 0.5 | | |
| | | $V_I = 12\text{ V}$ | | | | | 1 | 1.45 | | |
| I_R Clamp reverse current | Figure 7 | $V_R = 50\text{ V}$ | | | | | | 50 | | μA |
| | | | $T_A = 70^\circ\text{C}$ | | | | | | 100 | |
| C_i Input capacitance | | $V_I = 0$, $f = 1\text{ MHz}$ | | 15 | 25 | | 15 | 25 | | pF |

ELECTRICAL CHARACTERISTICS
 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST FIGURE | TEST CONDITIONS | ULN2003AI | | | UNIT | |
|---|-------------|---|-----------------------|------|------|------|---------------|
| | | | MIN | TYP | MAX | | |
| $V_{I(\text{on})}$ On-state input voltage | Figure 6 | $V_{CE} = 2\text{ V}$ | $I_C = 200\text{ mA}$ | | | 2.4 | V |
| | | | $I_C = 250\text{ mA}$ | | | 2.7 | |
| | | | $I_C = 300\text{ mA}$ | | | 3 | |
| $V_{CE(\text{sat})}$ Collector-emitter saturation voltage | Figure 5 | $I_I = 250\ \mu\text{A}$, $I_C = 100\text{ mA}$ | | 0.9 | 1.1 | V | |
| | | $I_I = 350\ \mu\text{A}$, $I_C = 200\text{ mA}$ | | 1 | 1.3 | | |
| | | $I_I = 500\ \mu\text{A}$, $I_C = 350\text{ mA}$ | | 1.2 | 1.6 | | |
| I_{CEX} Collector cutoff current | Figure 1 | $V_{CE} = 50\text{ V}$, $I_I = 0$ | | | | 50 | μA |
| V_F Clamp forward voltage | Figure 8 | $I_F = 350\text{ mA}$ | | | 1.7 | 2 | V |
| $I_{I(\text{off})}$ Off-state input current | Figure 3 | $V_{CE} = 50\text{ V}$, $I_C = 500\ \mu\text{A}$ | 50 | 65 | | | μA |
| I_I Input current | Figure 4 | $V_I = 3.85\text{ V}$ | | 0.93 | 1.35 | | mA |
| I_R Clamp reverse current | Figure 7 | $V_R = 50\text{ V}$ | | | | 50 | μA |
| C_i Input capacitance | | $V_I = 0$, $f = 1\text{ MHz}$ | | 15 | 25 | | pF |

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 105°C

| PARAMETER | TEST FIGURE | TEST CONDITIONS | ULN2003AI | | | UNIT |
|---|-------------|--|-------------------------|------|-----|------|
| | | | MIN | TYP | MAX | |
| V _{I(on)} On-state input voltage | Figure 6 | V _{CE} = 2 V | I _C = 200 mA | 2.7 | | V |
| | | | I _C = 250 mA | 2.9 | | |
| | | | I _C = 300 mA | 3 | | |
| V _{CE(sat)} Collector-emitter saturation voltage | Figure 5 | I _I = 250 μA, I _C = 100 mA | 0.9 | 1.2 | V | |
| | | I _I = 350 μA, I _C = 200 mA | 1 | 1.4 | | |
| | | I _I = 500 μA, I _C = 350 mA | 1.2 | 1.7 | | |
| I _{CEX} Collector cutoff current | Figure 1 | V _{CE} = 50 V, I _I = 0 | 100 | | μA | |
| V _F Clamp forward voltage | Figure 8 | I _F = 350 mA | 1.7 | 2.2 | V | |
| I _{I(off)} Off-state input current | Figure 3 | V _{CE} = 50 V, I _C = 500 μA | 30 | 65 | μA | |
| I _I Input current | Figure 4 | V _I = 3.85 V | 0.93 | 1.35 | mA | |
| I _R Clamp reverse current | Figure 7 | V _R = 50 V | 100 | | μA | |
| C _i Input capacitance | | V _I = 0, f = 1 MHz | 15 | 25 | pF | |

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST FIGURE | TEST CONDITIONS | ULQ2003A | | | ULQ2004A | | | UNIT |
|---|-------------|--|-------------------------|------|------|----------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{I(on)} On-state input voltage | Figure 6 | V _{CE} = 2 V | I _C = 125 mA | | | | | 5 | V |
| | | | I _C = 200 mA | 2.7 | | | | 6 | |
| | | | I _C = 250 mA | 2.9 | | | | | |
| | | | I _C = 275 mA | | | | | 7 | |
| | | | I _C = 300 mA | 3 | | | | | |
| | | | I _C = 350 mA | | | | | 8 | |
| V _{CE(sat)} Collector-emitter saturation voltage | Figure 5 | I _I = 250 μA, I _C = 100 mA | 0.9 | 1.2 | 0.9 | 1.1 | V | | |
| | | I _I = 350 μA, I _C = 200 mA | 1 | 1.4 | 1 | 1.3 | | | |
| | | I _I = 500 μA, I _C = 350 mA | 1.2 | 1.7 | 1.2 | 1.6 | | | |
| I _{CEX} Collector cutoff current | Figure 1 | V _{CE} = 50 V, I _I = 0 | 100 | | | | 50 | μA | |
| | Figure 2 | V _{CE} = 50 V, T _A = 70°C, V _I = 6 V | | | | | 100 | | |
| | | | | | | | 500 | | |
| V _F Clamp forward voltage | Figure 8 | I _F = 350 mA | 1.7 | 2.3 | 1.7 | 2 | V | | |
| I _{I(off)} Off-state input current | Figure 3 | V _{CE} = 50 V, T _A = 70°C, I _C = 500 μA | 65 | | 50 | 65 | μA | | |
| I _I Input current | Figure 4 | V _I = 3.85 V | 0.93 | 1.35 | | | | | |
| | | V _I = 5 V | | | 0.35 | 0.5 | mA | | |
| | | V _I = 12 V | | | 1 | 1.45 | | | |
| I _R Clamp reverse current | Figure 7 | V _R = 50 V | T _A = 25°C | | | | 100 | μA | |
| | | | | | | | 50 | | |
| | | | | | | | 100 | | |
| C _i Input capacitance | | V _I = 0, f = 1 MHz | 15 | 25 | 15 | 25 | pF | | |

SWITCHING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | ULN2002A, ULN2003A, ULN2004A | | | UNIT |
|---|---|---------------------------------|------|-----|---------------|
| | | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low- to high-level output | See Figure 9 | | 0.25 | 1 | μs |
| t_{PHL} Propagation delay time, high- to low-level output | See Figure 9 | | 0.25 | 1 | μs |
| V_{OH} High-level output voltage after switching | $V_S = 50\text{ V}$, $I_O = 300\text{ mA}$, See Figure 10 | $V_S - 20$ | | | mV |

SWITCHING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | ULN2003AI | | | UNIT |
|---|---|------------|------|-----|---------------|
| | | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low- to high-level output | See Figure 9 | | 0.25 | 1 | μs |
| t_{PHL} Propagation delay time, high- to low-level output | See Figure 9 | | 0.25 | 1 | μs |
| V_{OH} High-level output voltage after switching | $V_S = 50\text{ V}$, $I_O \approx 300\text{ mA}$, See Figure 10 | $V_S - 20$ | | | mV |

SWITCHING CHARACTERISTICS

 $T_A = -40^\circ\text{C}$ to 105°C

| PARAMETER | TEST CONDITIONS | ULN2003AI | | | UNIT |
|---|---|------------|-----|-----|---------------|
| | | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low- to high-level output | See Figure 9 | | 1 | 10 | μs |
| t_{PHL} Propagation delay time, high- to low-level output | See Figure 9 | | 1 | 10 | μs |
| V_{OH} High-level output voltage after switching | $V_S = 50\text{ V}$, $I_O \approx 300\text{ mA}$, See Figure 10 | $V_S - 50$ | | | mV |

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | ULQ2003A, ULQ2004A | | | UNIT |
|---|---|--------------------|-----|-----|---------------|
| | | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low- to high-level output | See Figure 9 | | 1 | 10 | μs |
| t_{PHL} Propagation delay time, high- to low-level output | See Figure 9 | | 1 | 10 | μs |
| V_{OH} High-level output voltage after switching | $V_S = 50\text{ V}$, $I_O = 300\text{ mA}$, See Figure 10 | $V_S - 20$ | | | mV |

PARAMETER MEASUREMENT INFORMATION

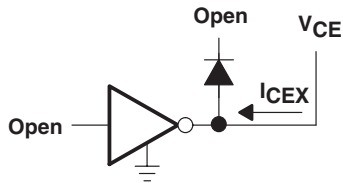


Figure 1. I_{CEX} Test Circuit

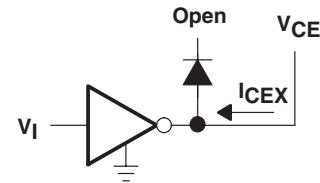


Figure 2. I_{CEX} Test Circuit

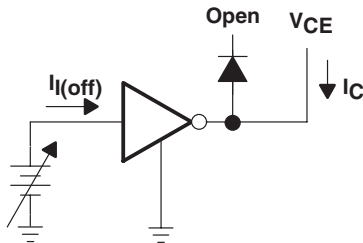


Figure 3. $I_{I(off)}$ Test Circuit

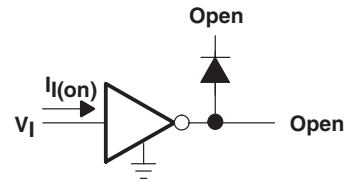


Figure 4. I_I Test Circuit

A. I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

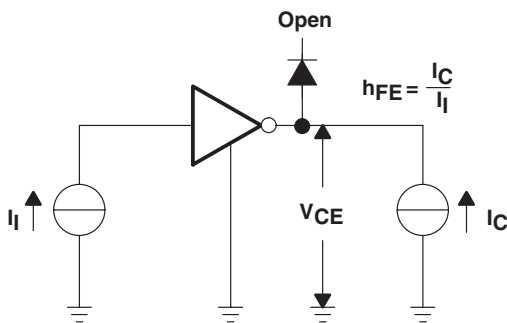


Figure 5. h_{FE} , $V_{CE(sat)}$ Test Circuit

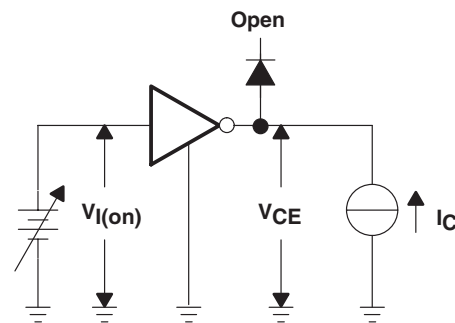


Figure 6. $V_{I(on)}$ Test Circuit

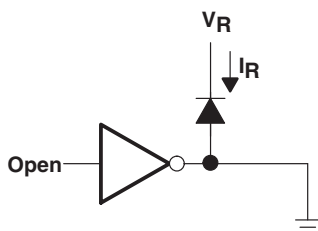


Figure 7. I_R Test Circuit

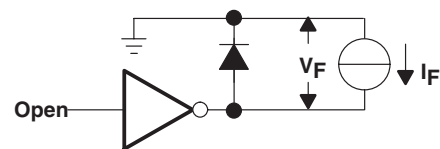


Figure 8. V_F Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

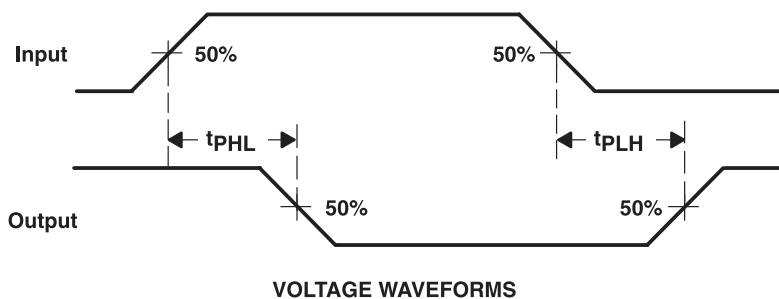
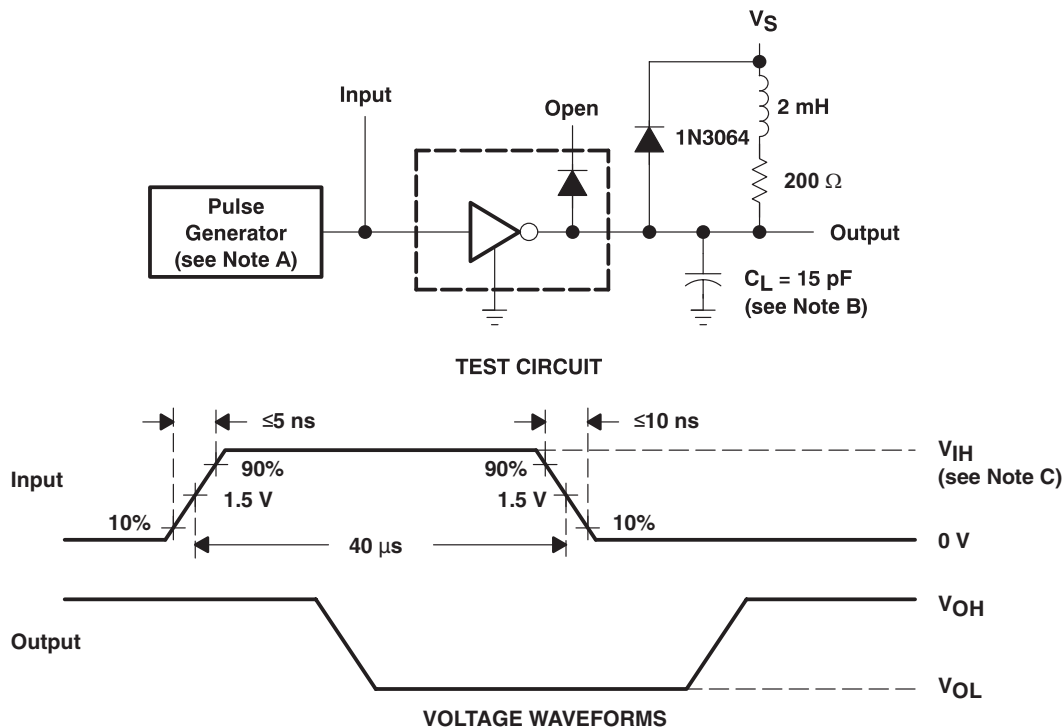


Figure 9. Propagation Delay-Time Waveforms



- A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. For testing the ULN2003A, ULN2003AI, and ULQ2003A, $V_{IH} = 3 \text{ V}$; for the ULN2002A, $V_{IH} = 13 \text{ V}$; for the ULN2004A and the ULQ2004A, $V_{IH} = 8 \text{ V}$.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

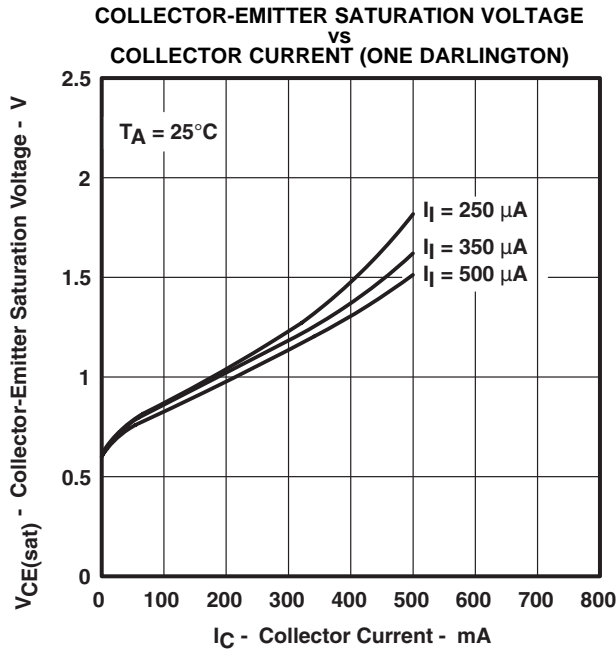


Figure 11.

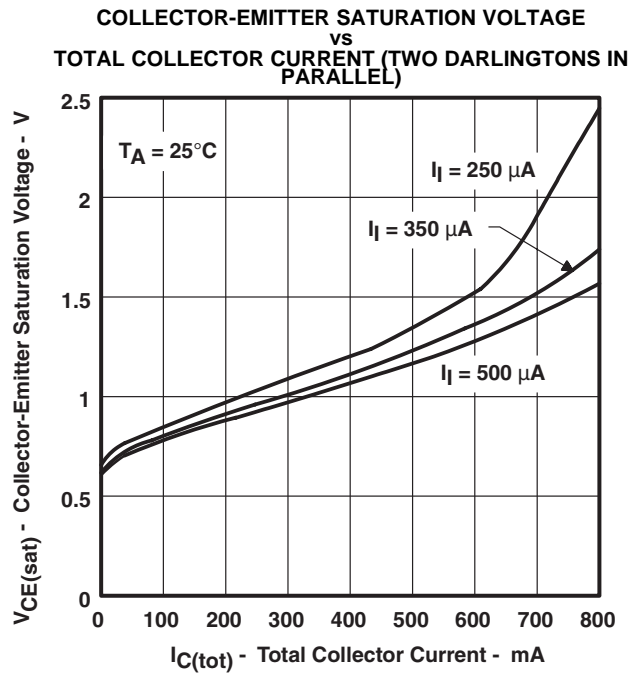


Figure 12.

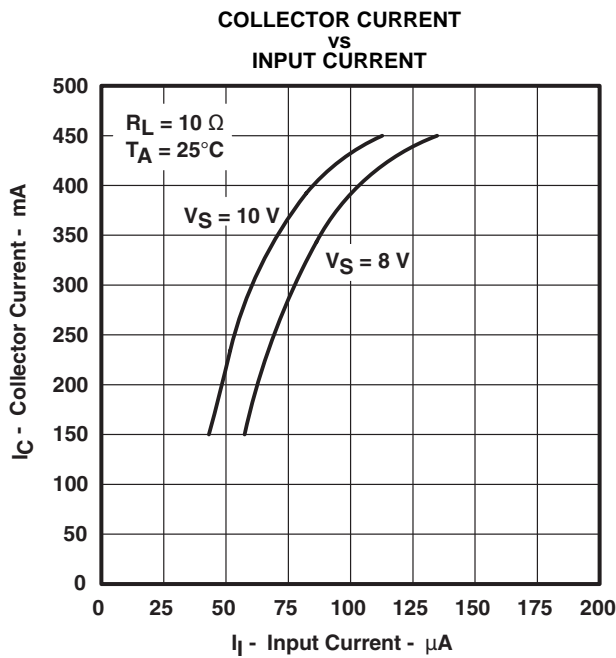


Figure 13.

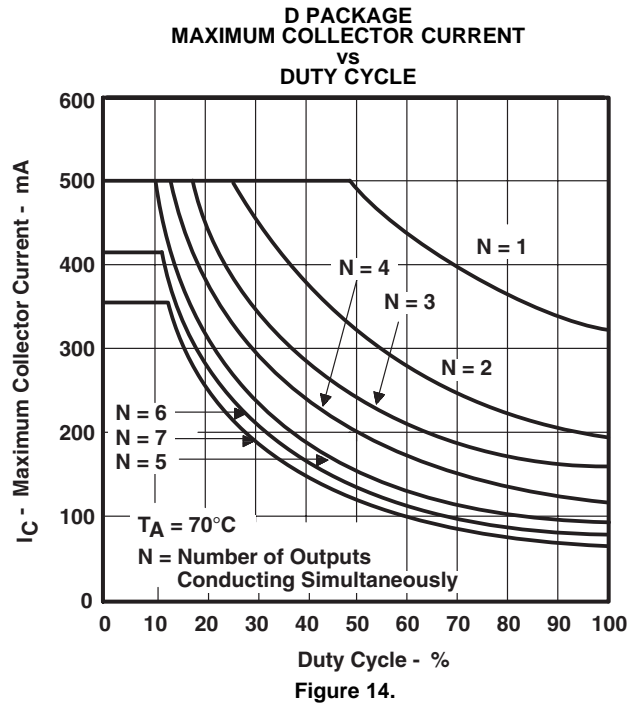
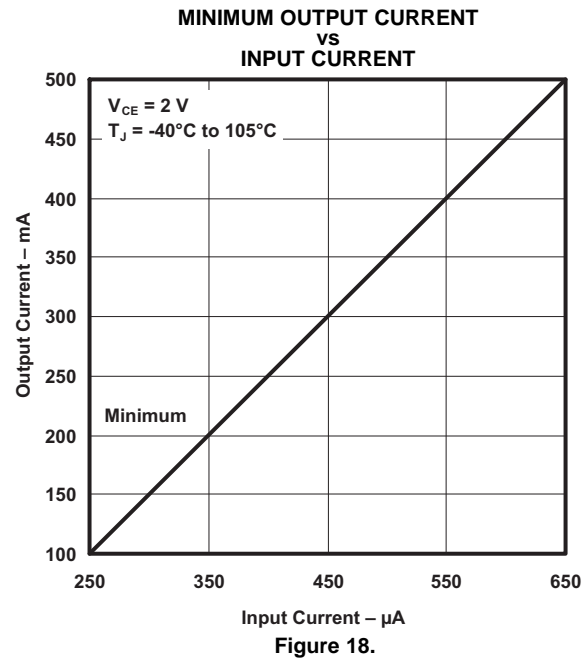
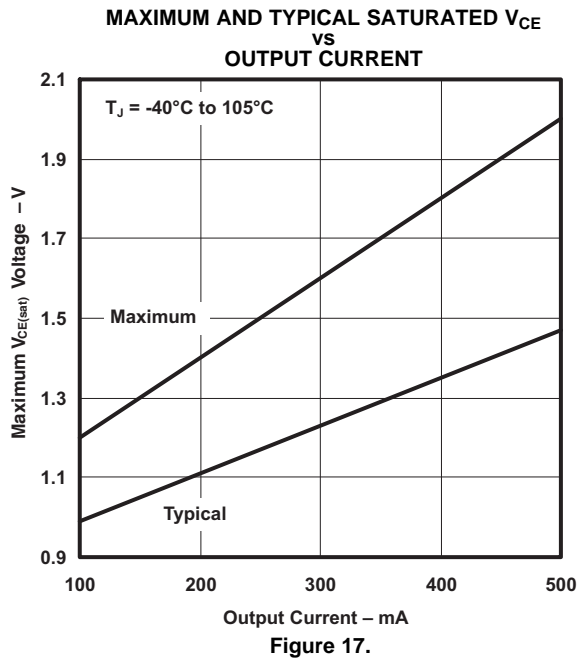
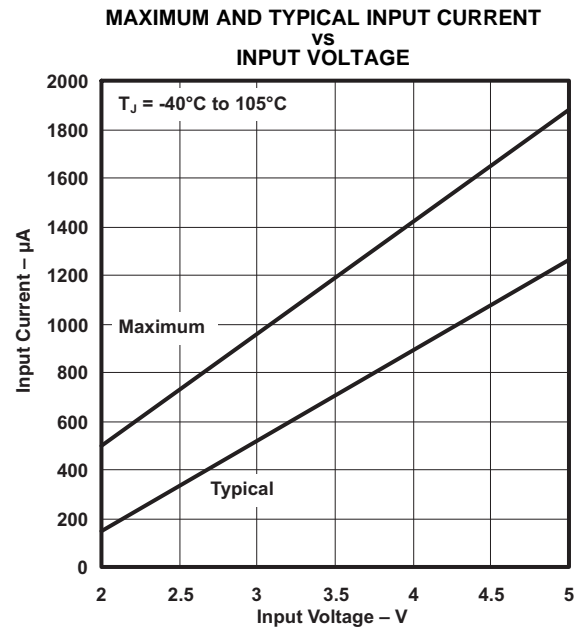
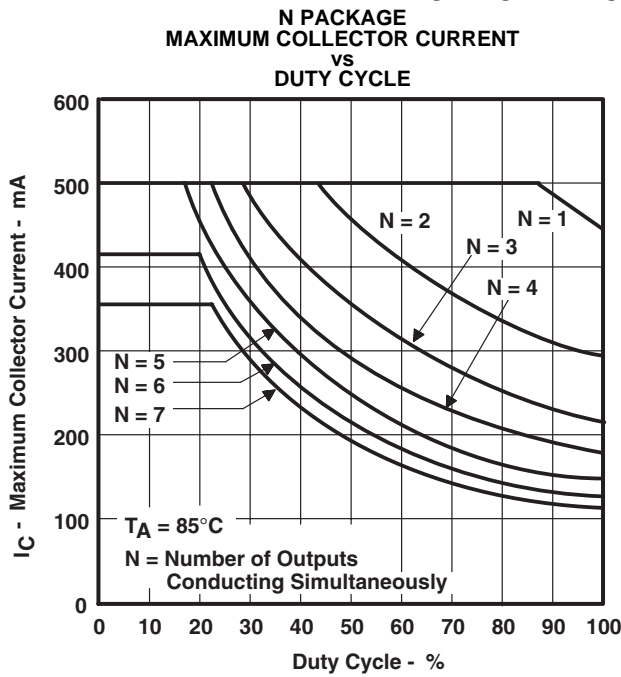


Figure 14.

TYPICAL CHARACTERISTICS (continued)



APPLICATION INFORMATION

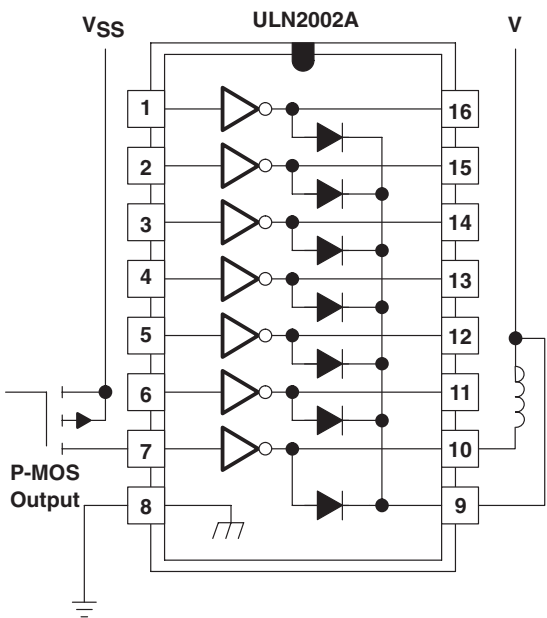


Figure 19. P-MOS to Load

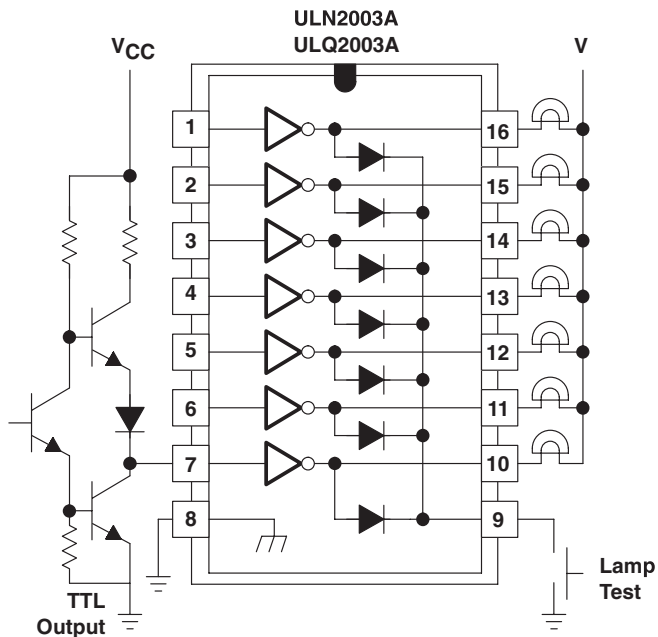


Figure 20. TTL to Load

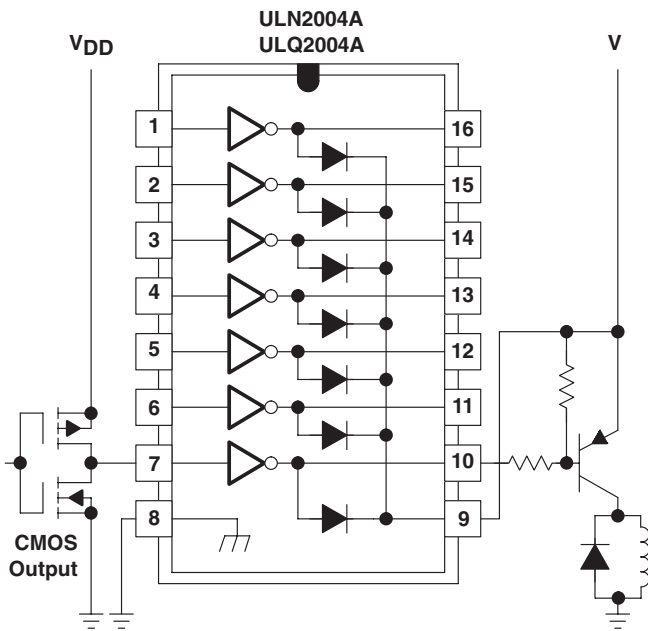


Figure 21. Buffer for Higher Current Loads

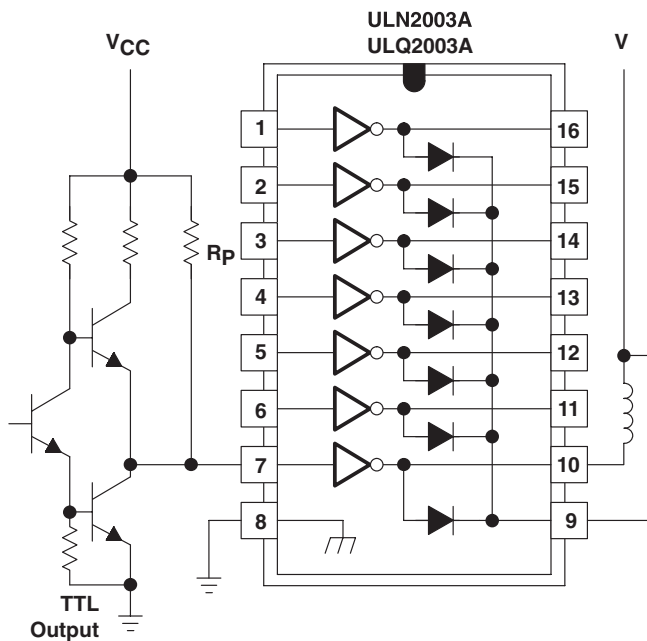


Figure 22. Use of Pullup Resistors to Increase Drive Current

REVISION HISTORY

| Changes from Revision K (August 2011) to Revision L | Page |
|--|-------------|
|--|-------------|

- Removed reference to obsolete ULN2001 part [1](#)
-

| Changes from Revision L (March 2012) to Revision M | Page |
|---|-------------|
|---|-------------|

- Updated temperature rating for ULN2003AI in the ORDERING INFORMATION table. [2](#)
-

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ULN2001AD | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | | | |
| ULN2001ADR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | | | |
| ULN2001AN | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | | | |
| ULN2002AD | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | | | |
| ULN2002AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2002AN | Samples |
| ULN2002ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2002AN | Samples |
| ULN2003AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADRG3 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003AID | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ULN2003AIN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 105 | ULN2003AIN | Samples |
| ULN2003AINE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 105 | ULN2003AIN | Samples |
| ULN2003AINSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| ULN2003AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU CU SN | N / A for Pkg Type | -20 to 70 | ULN2003AN | Samples |
| ULN2003ANE3 | PREVIEW | PDIP | N | 16 | 25 | TBD | Call TI | Call TI | -20 to 70 | | |
| ULN2003ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2003AN | Samples |
| ULN2003ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003APW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2003APWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2003APWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ULN2003APWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2003APWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2003APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2004AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2004AN | Samples |
| ULN2004ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2004AN | Samples |
| ULN2004ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULQ2003AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ULQ2003A | Samples |
| ULQ2003ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | ULQ2003A | Samples |
| ULQ2003ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ULQ2003A | Samples |
| ULQ2003ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | ULQ2003A | Samples |
| ULQ2003AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | ULQ2003A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ULQ2004AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ULQ2004A | Samples |
| ULQ2004ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | ULQ2004A | Samples |
| ULQ2004ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ULQ2004A | Samples |
| ULQ2004ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | ULQ2004A | Samples |
| ULQ2004AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | ULQ2004AN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ULQ2003A, ULQ2004A :

- Automotive: [ULQ2003A-Q1](#), [ULQ2004A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

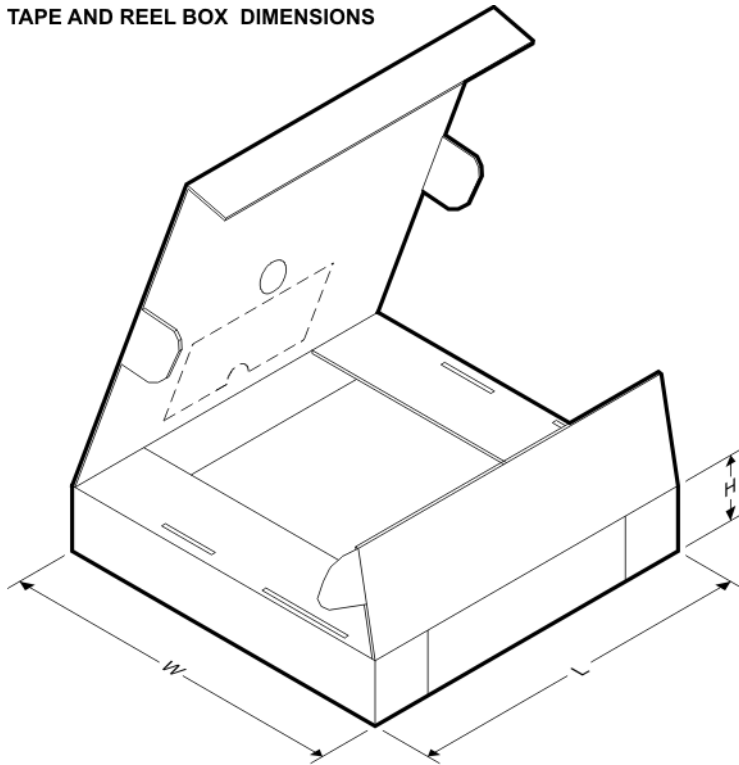
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ULN2003ADR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003ADRG3 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003AIDR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003AIDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003AIDRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003AIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003AIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003AIPWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ULQ2003ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ULN2003ADR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| ULN2003ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2003ADRG3 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| ULN2003ADRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2003AIDR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| ULN2003AIDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2003AIDRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2003AIPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| ULN2003AIPWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| ULN2003AIPWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| ULN2003APWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| ULN2003APWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| ULN2003APWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ULN2004ADRG4 | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| ULN2004ADRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULQ2003ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

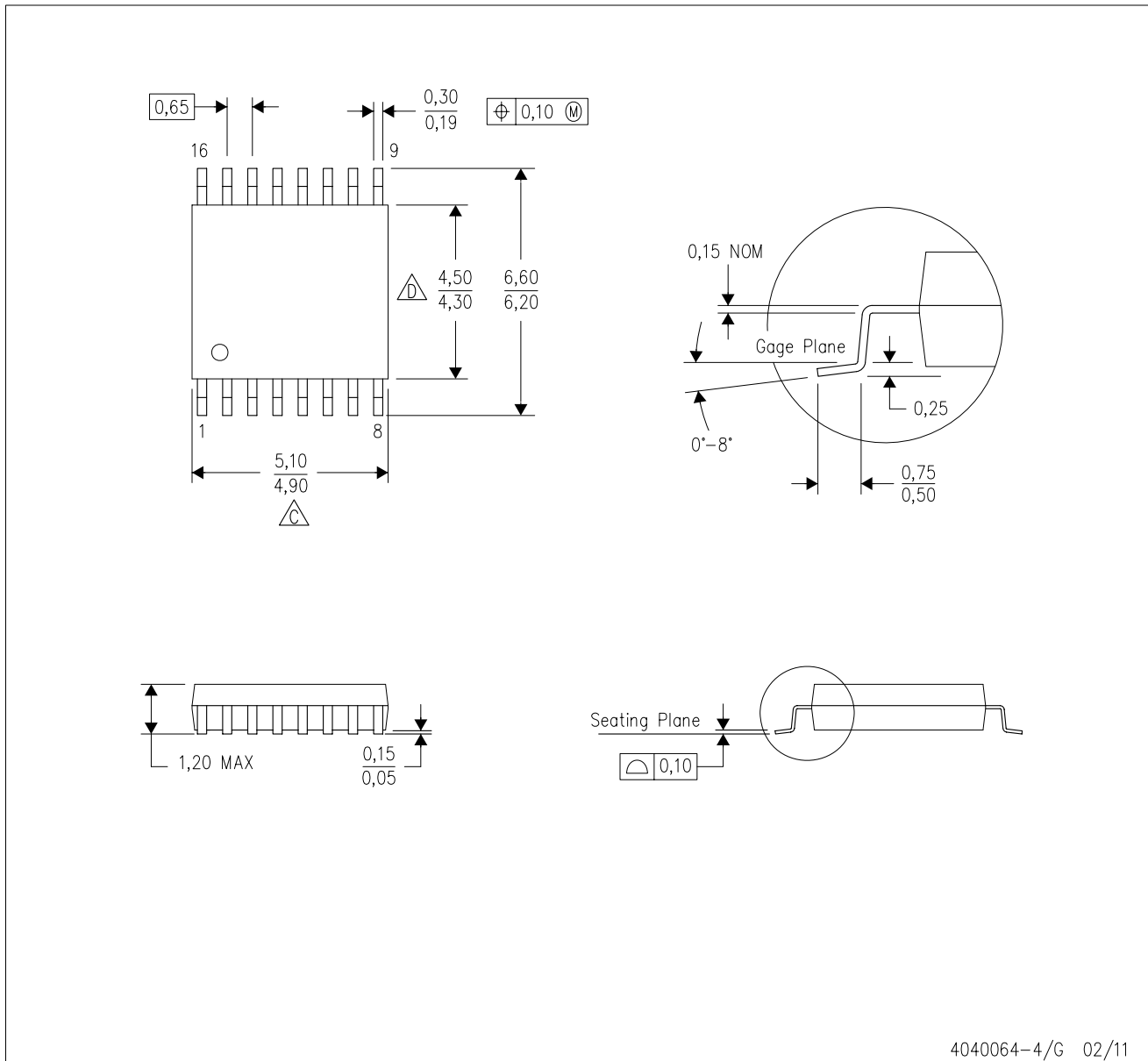


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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