UCC12050EVM-022 User's Guide

This user's guide provides a description as well as directions for the use of UCC12050EVM-022 to evaluate the UCC12050 Isolated DC-DC Converter from Texas Instruments. This EVM allows designers to quickly and efficiently evaluate the UCC12050DVE for use in electrically isolated system designs.

CAUTION

This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the 0 V to 5.5 V recommended operating range.

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Trademarks

1 Introduction

The UCC12050DVE is a high efficiency, low-emissions, 5 kVrms Isolated DC-DC Converter capable of delivering up to 500 mW of power to isolated applications. Since the UCC12050DVE provides isolated power in an integrated package, this allows systems to reduce cost and size by removing the need for separate isolated power supplies. The UCC12050DVE delivers class-leading efficiency in power conversion from the primary to the secondary side while removing the need for bulky external transformer or power modules common in current designs. This integration allows for a much smaller area as well as a much shorter profile when compared to industry standards for power isolation techniques used in the field today.

2 Description

The UCC12050EVM-022 is intended to allow designers to evaluate the performance characteristics and abilities of the UCC12050DVE quickly and easily for use in isolated systems. The EVM allows users to test functions of the UCC12050DVE such as: Enable/Disable the device easily, Sync the device with an external clock source, detect potential external clock faults, select 5 V or 5.4 V output modes, and easily apply variable resistive loads to the output.

This EVM allows the user to easily measure efficiency across the input voltage range and varying output loads that the system might require. Section 5 documents how to make connections and measurements for testing efficiency across varying loads. Another feature of this EVM is the test points, which are labeled as TP1, TP2 and TP3, specially intended for use with oscilloscope probe ground springs, also known as *pig tails*, for measuring small signals such as input/output ripple voltages.

3 Pin Configuration and Pin Functions

DVE Package
16-Pin SOIC
Top View

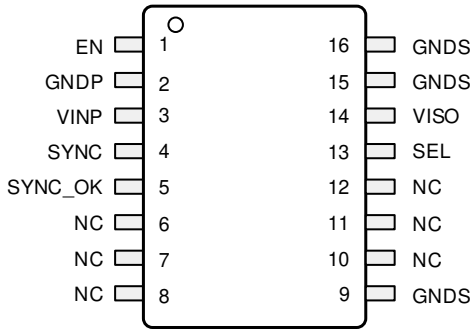


Figure 1. UCC12050DVE Pinout

Table 1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
EN	1	I	Active-high enable input. Connect EN to GNDP to disable the device. Connect EN to VINP to enable the device.docato-extra-info-title EN must be in the desired state (enabled/disabled) prior to power up. Switching the state of EN while the EVM is powered on may result in undesirable performance.
GNDP	2	P	Ground return for primary side supply (VINP).
VINP	3	P	Primary side input supply voltage input. Connect a 10-µF ceramic capacitor between VINP and GNDP, close to the device pins, for proper operation. Connect a 0.1µF ceramic capacitor in parallel with the 10µF for additional high frequency filtering.
SYNC	4	I	Synchronous clock input pin. Provide a clock signal to synchronize multiple UCC12050 devices or connect to GNDP for standalone operation using the internal oscillator. If the SYNC pin is left open it should be separated from any switching noise to avoid false clock coupling.
SYNC_OK	5	O	Active-low, open-drain diagnostic output. Pin is asserted LOW if no external SYNC clock or one that is outside of the operating range of the UCC12050 is detected. In this state, the external clock is ignored and the DC-DC converter is clocked by the device's internal oscillator. The pin is in high-impedance if a good clock is applied on SYNC.
NC	6, 7, 8	—	No internal connection. Connect NC to GNDP on printed circuit board.
GNDS	9, 15, 16	P	Ground return for secondary side (VISO).
NC	10, 11, 12	—	No internal connection. Connect NC to GNDS on printed circuit board.
SEL	13	I	VISO regulation voltage selection input. VISO regulation is selectable between 3.3V, 3.7V, 5.0V, and 5.4V using the SEL input. See for more details using SEL to select the VISO regulation threshold.
VISO	14	P	Isolated supply voltage output. Connect a 10-µF ceramic capacitor between VISO and GNDS, close to the device pins, for proper operation. Connect a 0.1µF ceramic capacitor in parallel with the 10µF for additional high frequency filtering.

(1) P = Power, G = Ground, I = Input, O = Output

4 Typical Application Circuit and Top Component View

Figure 2 shows the typical application circuit for UCC12050DVE.

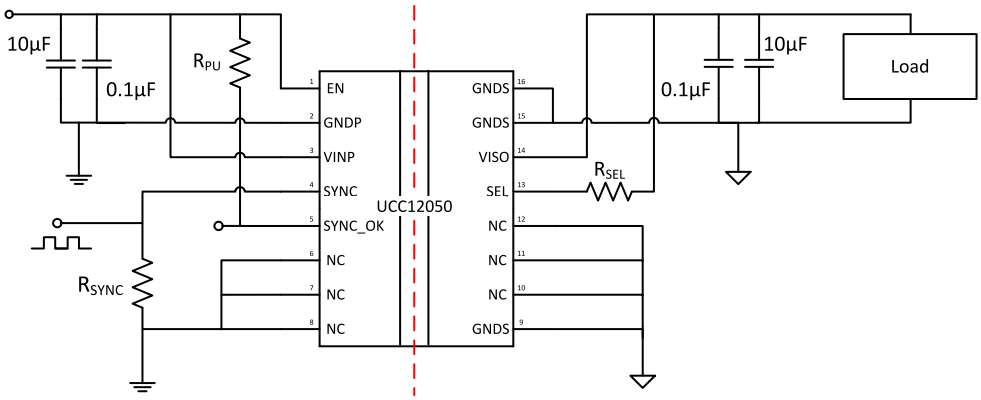


Figure 2. Typical application circuit

Figure 3 shows a top view picture of the EVM.

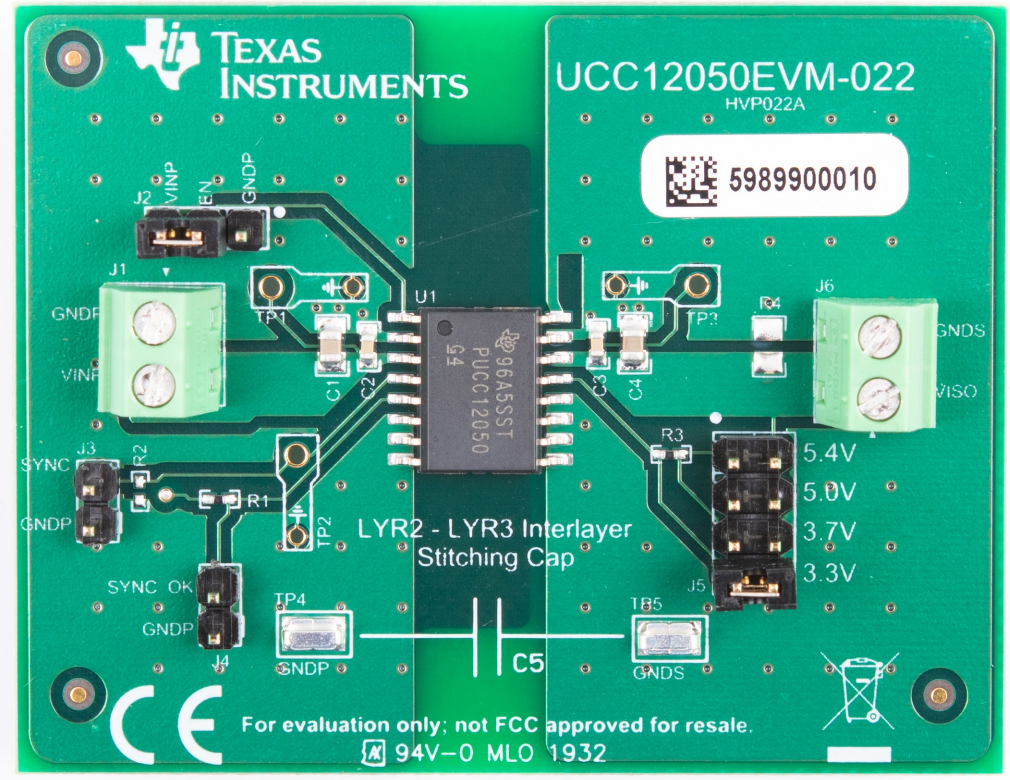


Figure 3. Top view of UCC12050EVM-022 Rev. A

5 EVM Setup and Operation

5.1 External Connections for Easy Evaluation

The UCC12050EVM-022 EVM utilizes screw terminals for quickly connecting to VINP and VISO. Connect a +5 V supply (+4.5 V to +5.5 V) between VINP and GNDP of J1 to supply power to the board. Connect a variable load between VISO and GNDS of J6. Alternatively, R4 is available to solder down a load resistor directly to the board. It is recommended to use an 0805 resistor that is rated for 0.5 W or greater. The value depends on the application needs, but the load should not exceed 0.5 W.

5.2 High Voltage Isolation

The UCC12050DVE is capable of supporting reinforced isolation. To this end, the PCB in the UCC12050DVE is designed to demonstrate proper layout techniques to enable reinforced isolation. The channel distance between the primary and secondary side (including the GNDP to GNDS planes and VINP to VISO distance) satisfies requirements for minimum required creepage and clearance distances to maintain reinforced isolation barrier across from the input side to the output side.

NOTE: This EVM is not intended for high voltage isolation testing, but merely to demonstrate proper isolation board design.

5.3 Enabling and Disabling the UCC12050

The enable/disable function is easily evaluated using the jumper, J2. Connect the shunt between EN and VINP to enable the UCC12050. Connect the shunt between EN and GNDP to disable the UCC12050 and place it in a low-power state.

5.4 SYNC and SYNC_OK Functionality

J3 is provided to connect an external clock to the UCC12050. In order to synchronize multiple UCC12050 devices to a single clock source, connect an external oscillator (a function generator) between SYNC and GNDP. The oscillator must be a 0 V to 5 V square wave at a frequency of double the desired switching frequency with a 50% duty cycle. The frequency must be within the specified operating range of the device, 14.4 MHz - 17.6 MHz.

The SYNC_OK output, J4, indicates when a valid clock source is connected to SYNC_OK. SYNC_OK is high impedance when a valid clock is connected, and pulled to GNDP when no clock, or an invalid clock, is connected to SYNC. SNYC_OK is pulled up to VINP on the EVM. R2 pads are available to place a termination resistor on SYNC, if needed.

5.5 Output Voltage Selection

The SEL input determines the output voltage regulation threshold of VISO. The UCC12050EVM-022 provides J5 to easily select between the different output voltage selections. J5 is clearly labeled to easily identify the jumper position required for the desired output voltage. For reference, the SEL connection required to achieve a particular ISO regulation is provided in Table 2. The device interprets the SEL pin as part of the startup routine, so the SEL state at startup is used to set the regulation point. Any change to J5 has no effect during operation. To change the output voltage regulation, it is required to disable the device (or power down), change the shunt to the desired position, then enable (or power on) the UCC12050.

Table 2. Output Voltage Regulation Selections

SEL Position	Output Voltage
SEL connected directly to VISO	5.0V
SEL connected to VISO through 100k	5.4V
SEL connected to GNDS through 100k	3.7V
SEL connected directly to GNDS	3.3V

5.6 Test Points :TP1, TP2 & TP3

Test points for VINP, VISO, and SYNC are provided on the EVM. To get the cleanest measurement of output ripple using an oscilloscope, use probe tip with a ground spring. This reduces the added noise that is introduced when using the longer alligator clip style ground lead. Figure 4 shows a picture illustrating how these test points are best used. Comparison scope shots between the two grounding methods are shown in Figure 5.

Figure 4. Using the pig tail test points: TP1, TP2, TP3

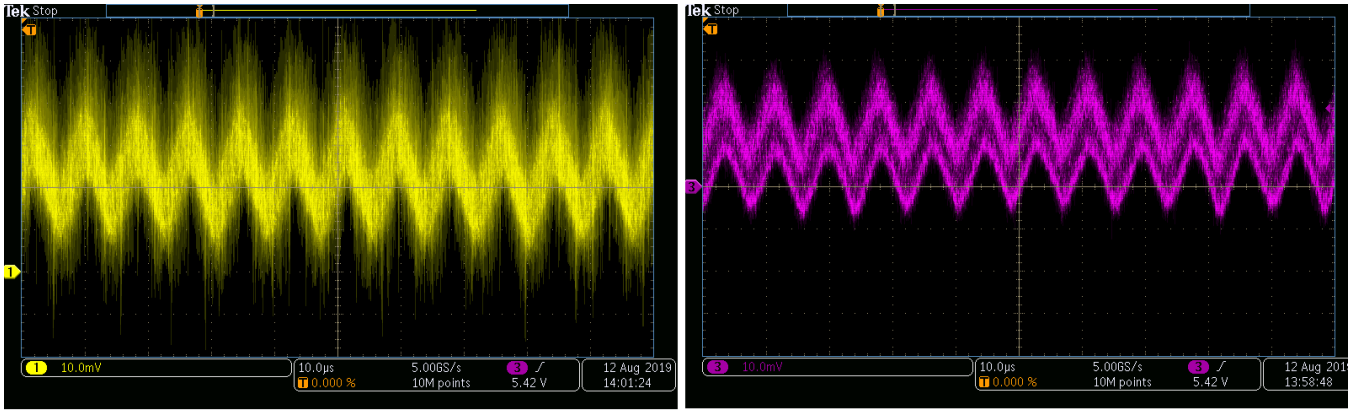


Figure 5. Comparison between voltage measured by a alligator clip (left) versus ground spring (right).

5.7 Board Level EMI Mitigation Techniques

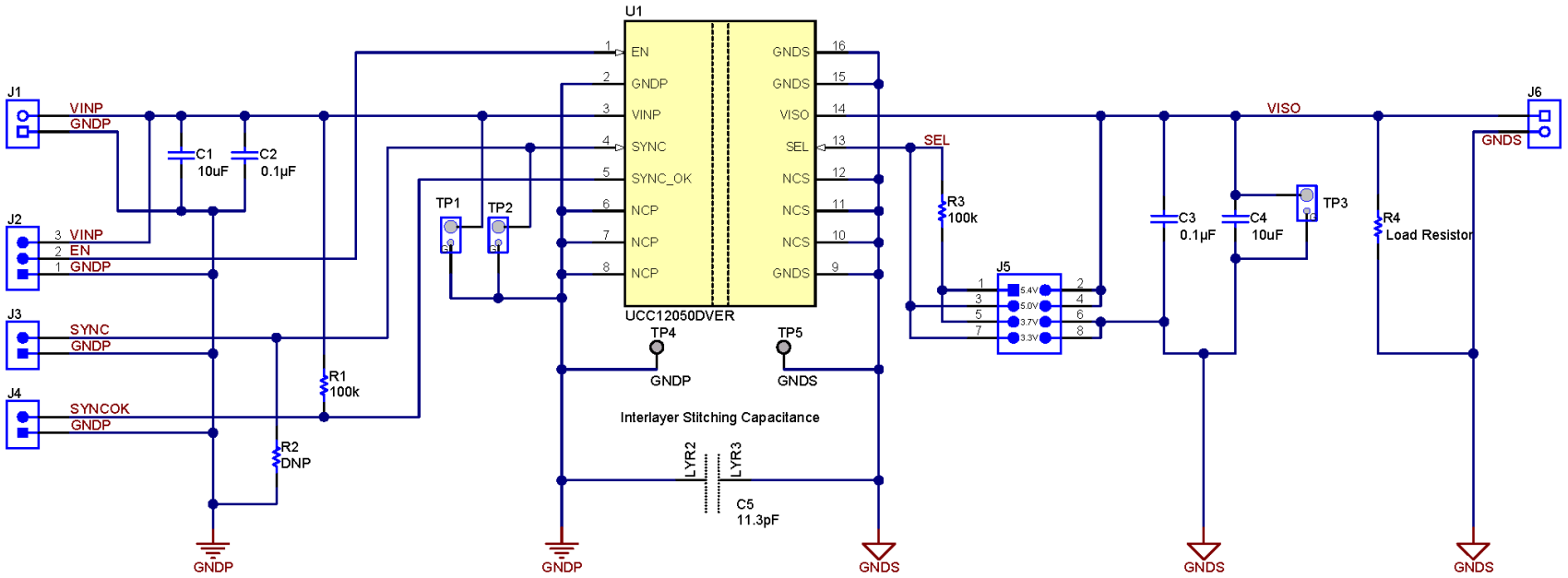
The UCC12050EVM-022 board layout is optimized for EMI performance. One EMI mitigation techniques demonstrated is a interlayer stitching capacitor (shown as C5 in the schematic). The GNDP and GNDS planes on the inner layers (layer 2 and layer 3) are overlapped in order to form a capacitive filter coupling between the two ground planes. GNDP on layer 2 and GNDS on layer 3 overlap. Note that the GND planes do not go all the way to the edge of the board where they overlap. This is to illustrate how to satisfy isolation requirements. There is sufficient distance between the edge of the overlapping layers using this methodology. This only must be used when the planes overlap close to the edge of the board. The second EMI mitigation technique used is to use stitch vias in the GND planes (GNDP and GNDS) to further suppress EM transmissions.

6 List of Materials

Table 3. List of Materials

Designator	Qty	Description	Part Number	Manufacturer
C1, C4	2	Capacitor, ceramic, 10 uF, 16 V, +/- 10%, X7R, 0805	CL21B106KOQNNNE	Samsung Electro-Mechanics
C2, C3	2	Capacitor, ceramic, 0.1 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	06035C104KAZ2A	AVX
J1, J6	2	Conn term block, 2POS, 3.81mm, TH	1727010	Phoenix Contact
J2	1	Header, 100 mil, 3x1, Tin, TH	PEC03SAAN	Sullins Connector Solutions
J3, J4, J5	3	Header, 100 mil, 2x1, Tin, TH	PEC02SAAN	Sullins Connector Solutions
R1, R3	2	Resistor, 100 kΩ, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402100KJNED	Vishay-Dale
R2	0	Termination resistor for SYNC, 0402, DNP		
R4	0	Load resistor, 0805, DNP		
TP4, TP5	2	Test point, Miniature, SMT	5019	Keystone
U1	1	500 mW, High-Efficiency, Low-Emissions, 5 kVRMS Isolated DC-DC Converter, DVE0016A (SO-MOD-16)	UCC12050DVER	Texas Instruments
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A

7 Schematic



8 Layout Diagrams

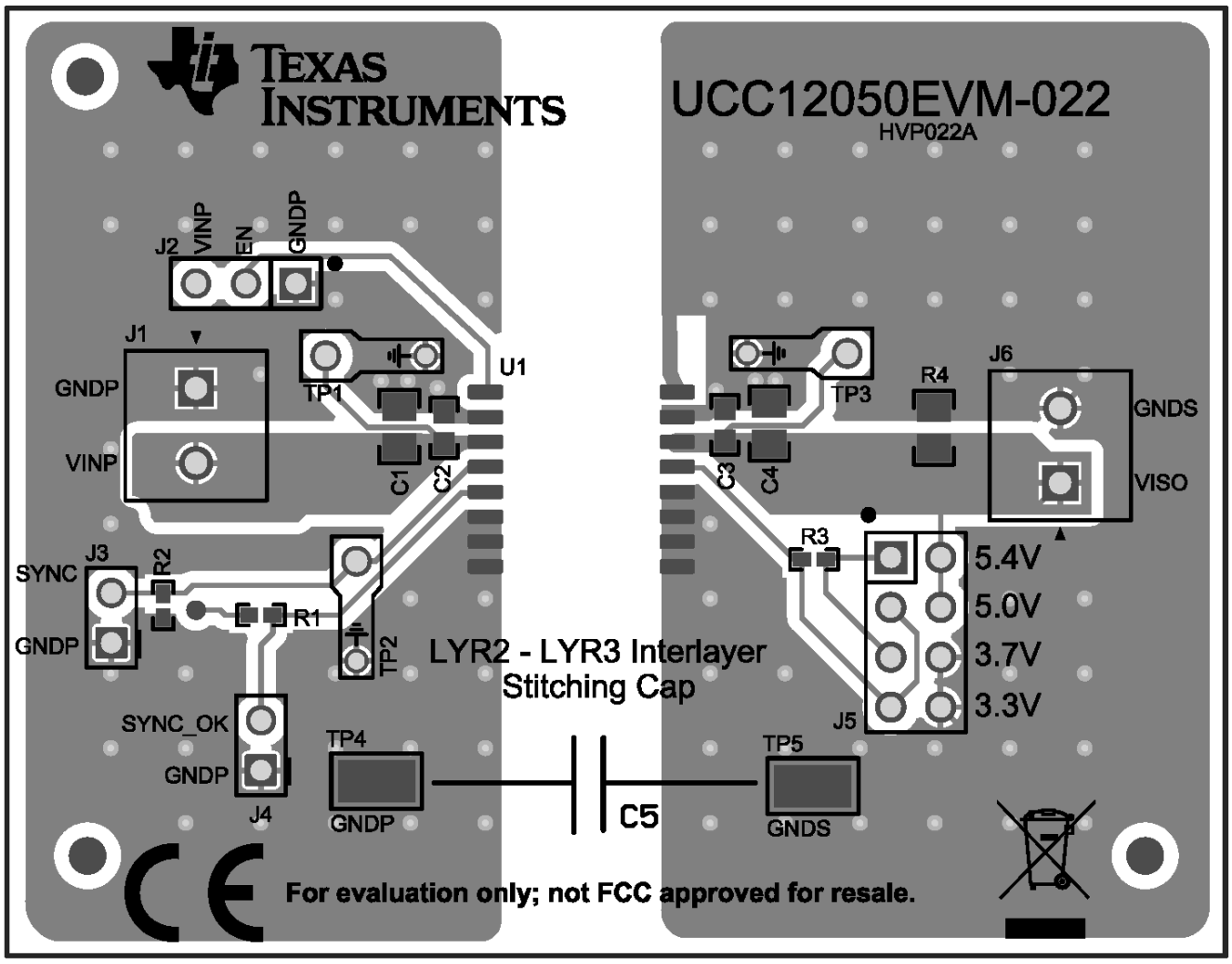


Figure 6. Top Layer Composite

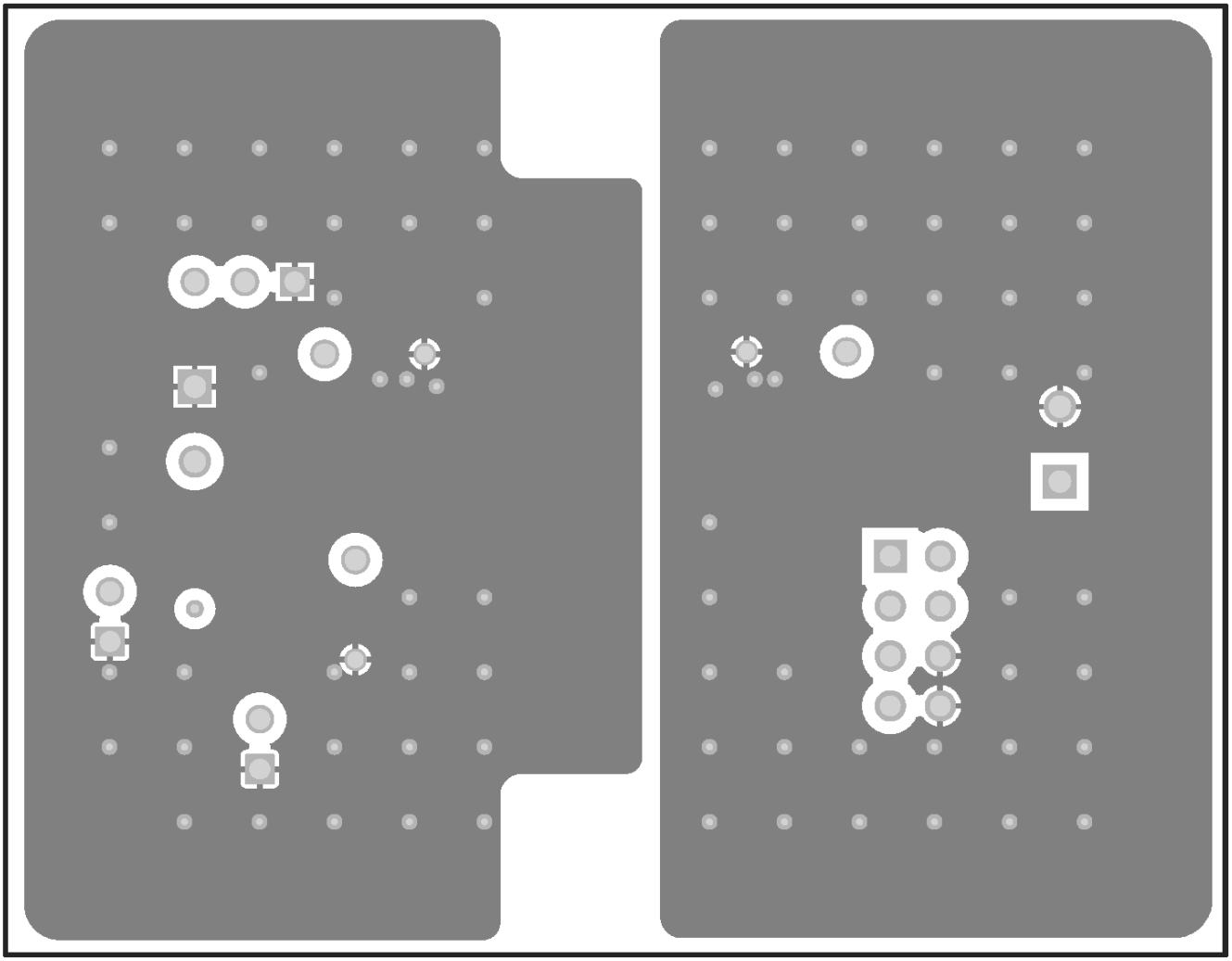


Figure 7. Signal Layer 1

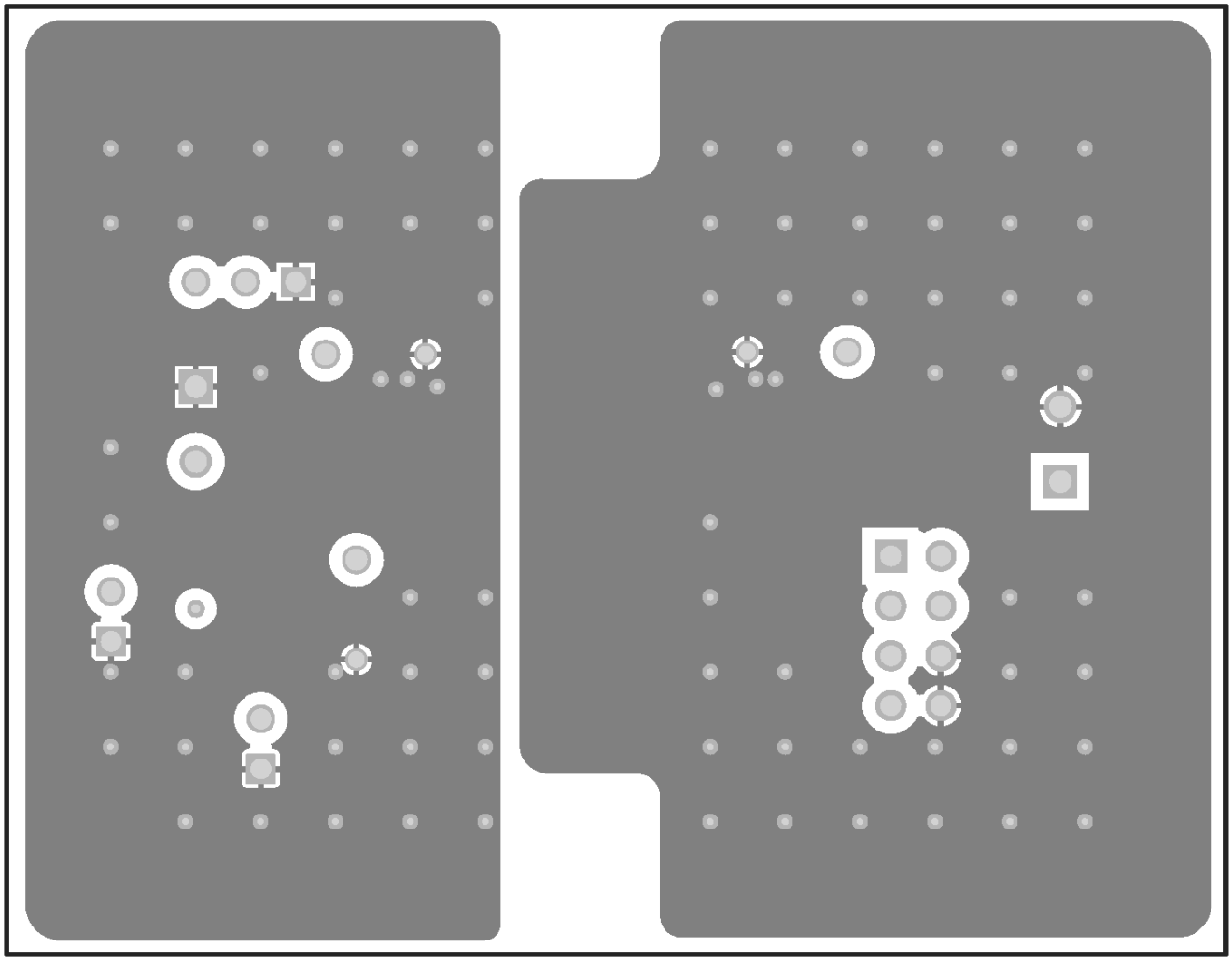


Figure 8. Signal Layer 2

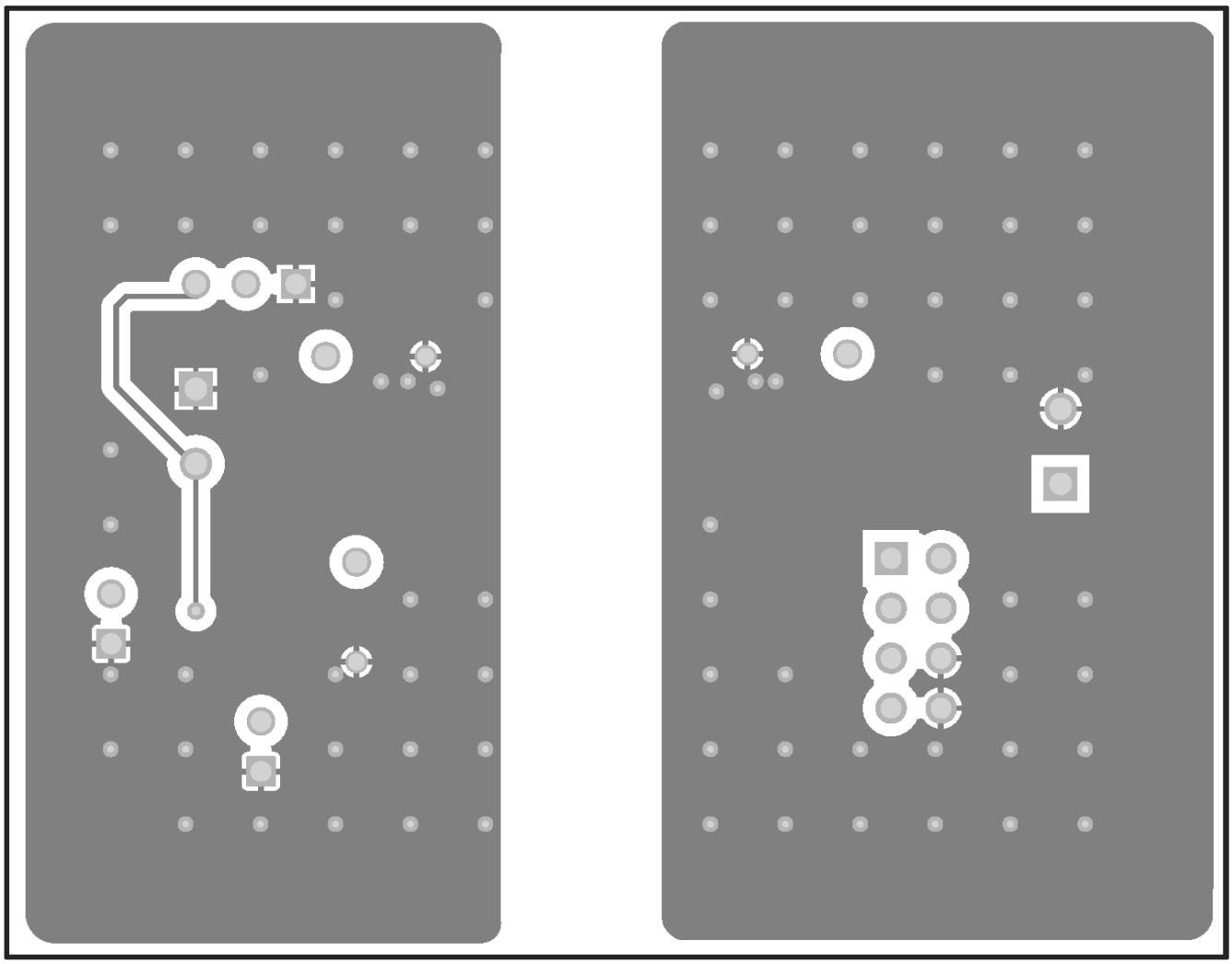


Figure 9. Bottom Layer

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