UNITRODE

High Power Factor Preregulator

UC1854
UC2854
UC3854

FEATURES

- Control Boost PWM to 0.99 Power Factor
- Limit Line Current Distortion To <5%
- World-Wide Operation Without Switches
- Feed-Forward Line Regulation
- Average Current-Mode Control
- Low Noise Sensitivity
- Low Start-Up Supply Current
- Fixed-Frequency PWM Drive
- Low-Offset Analog Multiplier/Divider
- 1A Totem-Pole Gate Driver
- Precision Voltage Reference

DESCRIPTION

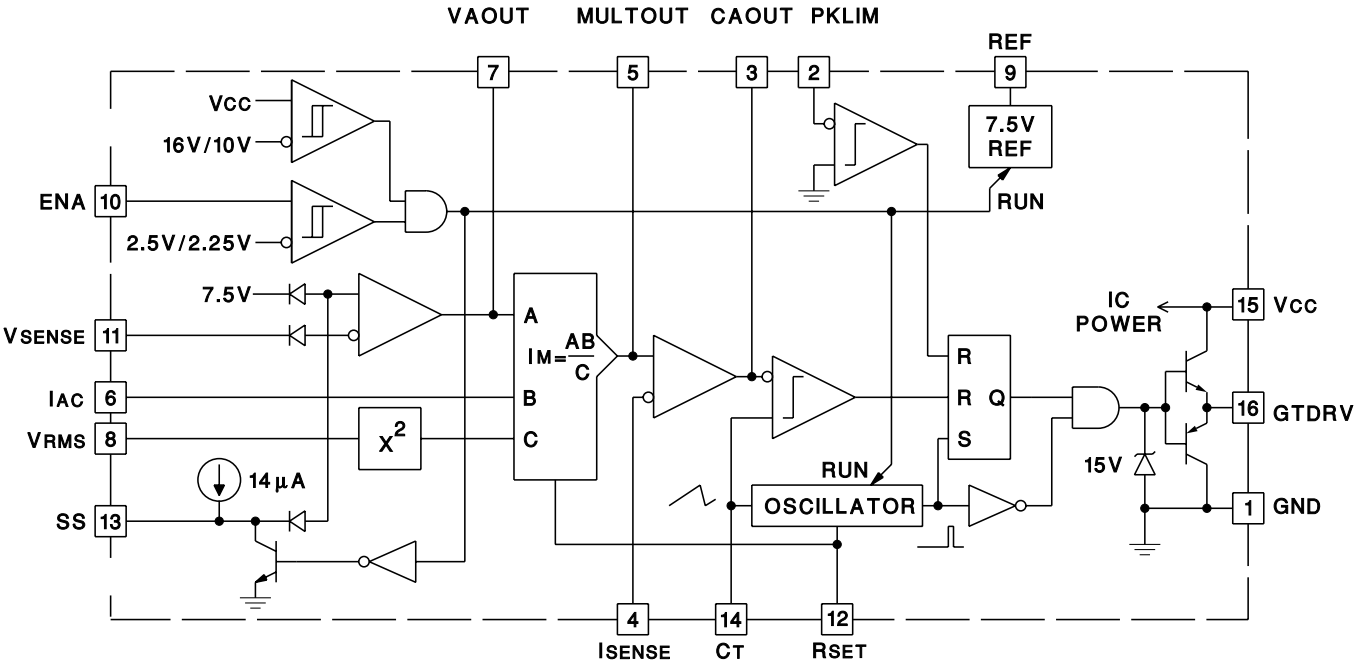
The UC1854 provides active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC1854 contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC1854 contains a power MOSFET compatible gate driver, 7.5V reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator.

The UC1854 uses average current-mode control to accomplish fixed-frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

The UC1854's high reference voltage and high oscillator amplitude minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200kHz. The UC1854 can be used in single and three phase systems with line voltages that vary from 75 to 275 volts and line frequencies across the 50Hz to 400Hz range. To reduce the burden on the circuitry that supplies power to this device, the UC1854 features low starting supply current.

These devices are available packaged in 16-pin plastic and ceramic dual in-line packages, and a variety of surface-mount packages.

BLOCK DIAGRAM



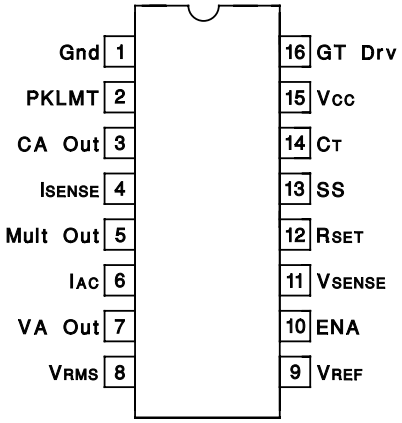
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 35V
GT Drv Current, Continuous 0.5A
GT Drv Current, 50% Duty Cycle 1.5A
Input Voltage, V_{SENSE}, V_{RMS} 11V
Input Voltage, I_{SENSE}, Mult Out 11V
Input Voltage, PKLMT 5V
Input Current, R_{SET}, I_{AC}, PKLMT, ENA 10mA
Power Dissipation 1W
Storage Temperature . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering, 10 Seconds) . . . . . $+300^oC$

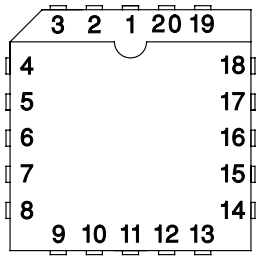
Note 1: All voltages with respect to Gnd (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: ENA input is internally clamped to approximately 14V.
Note 4: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limita-

CONNECTION DIAGRAMS

DIL–16 & SOIC-16
(Top View)
J, N & DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Gnd	2
PKLMT	3
CA Out	4
I_{SENSE}	5
N/C	6
Mult Out	7
I_{AC}	8
VA Out	9
V_{RMS}	10
N/C	11
V_{REF}	12
ENA	13
V_{SENSE}	14
R_{SET}	15
N/C	16
SS	17
C_T	18
V_{CC}	19
GT Drv	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_{SET}=15k to ground, C_T=1.5nF to ground, PKLMT=1V, ENA=7.5V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=7.5V, no load on SS, CA Out, VA Out, REF, GT Drv, $-55^oC<T_A<125^oC$ for the UC1854, $-40^oC<T_A<85^oC$ for the UC2854, and $0^oC<T_A<70^oC$ for the UC3854, and $T_A=T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	ENA=0V		1.5	2.0	mA
Supply Current, On			10	16	mA
V_{CC} Turn-On Threshold		14.5	16	17.5	V
V_{CC} Turn-Off Threshold		9	10	11	V
ENA Threshold, Rising		2.4	2.55	2.7	V
ENA Threshold Hysteresis		0.2	0.25	0.3	V
ENA Input Current	ENA=0V	–5.0	–0.2	5.0	µA
V_{RMS} Input Current	V_{RMS}=5V	–1.0	–.01	1.0	µA
VOLTAGE AMPLIFIER					
Voltage Amp Offset Voltage	VA Out=5V	–8		8	mV
V_{SENSE} Bias Current		–500	–25	500	nA
Voltage Amp Gain		70	100		dB
Voltage Amp Output Swing			0.5 to 5.8		V
Voltage Amp Short Circuit Current	VA Out=0V	–36	–20	–5	mA
SS Current	SS=2.5V	–20	–14	–6	µA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_{SET}=15k to ground, C_T=1.5nF to ground, PKLMT=1V, ENA=7.5V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=7.5V, no load on SS, CA Out, VA Out, REF, GT Drv, –55°C<T_A<125°C for the UC1854, –40°C<T_A<85°C for the UC2854, and 0°C<T_A<70°C for the UC3854, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT AMPLIFIER					
Current Amp Offset Voltage		–4		4	mV
I_{SENSE} Bias Current		–500	–120	500	nA
Input Range, I_{SENSE}, Mult Out		–0.3 to 2.5			V
Current Amp Gain		80	110		dB
Current Amp Output Swing			0.5 to 16		V
Current Amp Short Circuit Current	CA Out=0V	–36	–20	–5	mA
Current Amp Gain-BW Product	T_A=25°C (Note 6)	400	800		kHz
REFERENCE					
Reference Output Voltage	I_{REF}=0mA, T_A=25°C	7.4	7.5	7.6	V
	I_{REF}=0mA, Over Temp.	7.35	7.5	7.65	V
V_{REF} Load Regulation	–10mA<I_{REF}<0mA	–15	5	15	mV
V_{REF} Line Regulation	15V<V_{CC}<35V	–10	2	10	mV
V_{REF} Short Circuit Current	REF=0V	–50	–28	–12	mA
MULTIPLIER					
Mult Out Current I_{AC} Limited	I_{AC}=100µA, R_{SET}=10k, V_{RMS}=1.25V	–220	–200	–180	µA
Mult Out Current Zero	I_{AC}=0µA, R_{SET}=15k	–2.0	–0.2	2.0	µA
Mult Out Current R_{SET} Limited	I_{AC}=450µA, R_{SET}=15k, V_{RMS}=1V, VA Out = 6V	–280	–255	–220	µA
Mult Out Current	I_{AC}=50µA, V_{RMS}=2V, VA=4V	–50	–42	–33	µA
	I_{AC}=100µA, V_{RMS}=2V, VA=2V	–38	–27	–12	µA
	I_{AC}=200µA, V_{RMS}=2V, VA=4V	–165	–150	–105	µA
	I_{AC}=300µA, V_{RMS}=1V, VA=2V	–250	–225	–150	µA
	I_{AC}=100µA, V_{RMS}=1V, VA=2V	–95	–80	–60	µA
Multiplier Gain Constant	(Note 5)		–1.0		V
OSCILLATOR					
Oscillator Frequency	R_{SET}=15k	46	55	62	kHz
	R_{SET}=8.2k	86	102	118	kHz
C_T Ramp Peak-to-Valley Amplitude		4.9	5.4	5.9	V
C_T Ramp Valley Voltage		0.8	1.1	1.3	V
GATE DRIVER					
Maximum GT Drv Output Voltage	0mA load on GT Drv, 18V<V_{CC}<35V	13	14.5	18	V
GT Drv Output Voltage High	–200mA load on GT Drv, V_{CC}=15V	12	12.8		V
GT Drv Output Voltage Low, Off	V_{CC}=0V, 50mA load on GT Drv		0.9	1.5	V
GT Drv Output Voltage Low	200mA load on GT Drv		1.0	2.2	V
	10mA load on GT Drv		0.1	0.4	V
Peak GT Drv Current	10nF from GT Drv to Gnd		1.0		A
GT Drv Rise/Fall Time	1nF from GT Drv to Gnd		35		ns
GT Drv Maximum Duty Cycle	$V_{CA\ Out}$=7V		95		%
CURRENT LIMIT					
PKLMT Offset Voltage		–10		10	mV
PKLMT Input Current	PKLMT=–0.1V	–200	–100		µA
PKLMT to GT Drv Delay	PKLMT falling from 50mV to –50mV		175		ns

Note 5: Multiplier Gain Constant (k) is defined by: $I_{Mult\ Out} = \frac{k \times I_{AC} \times (VA\ Out - 1)}{V_{RMS}^2}$

Note 6: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS (Pin Numbers Refer to DIL Packages)

Gnd (Pin 1) (ground): All voltages are measured with respect to Gnd. V_{CC} and REF should be bypassed directly to Gnd with an 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to Gnd should also be as short and as direct as possible.

PKLMT (Pin 2) (peak limit): The threshold for PKLMT is 0.0V. Connect this input to the negative voltage on the current sense resistor as shown in Figure 1. Use a resistor to REF to offset the negative current sense signal up to Gnd.

CA Out (Pin 3) (current amplifier output): This is the output of a wide-bandwidth op amp that senses line current and commands the pulse width modulator (PWM) to force the correct current. This output can swing close to Gnd, allowing the PWM to force zero duty cycle when necessary. The current amplifier will remain active even if the IC is disabled. The current amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

I_{SENSE} (Pin 4) (current sense minus): This is the inverting input to the current amplifier. This input and the non-inverting input Mult Out remain functional down to and below Gnd. Care should be taken to avoid taking these inputs below –0.5V, because they are protected with diodes to Gnd.

Mult Out (Pin 5) (multiplier output and current sense plus): The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at Mult Out. The cautions about taking I_{SENSE} below –0.5V also apply to Mult Out. As the multiplier output is a current, this is a high impedance input similar to I_{SENSE}, so the current amplifier can be configured as a differential amplifier to reject Gnd noise. Figure 1 shows an example of using the current amplifier differentially.

I_{AC} (Pin 6) (input AC current): This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{AC}) to Mult Out, so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on I_{AC} is 6V, so in addition to a resistor from I_{AC} to rectified 60Hz, connect a resistor from I_{AC} to REF. If the resistor to REF is one fourth of the value of the resistor to the rectifier, then the 6V offset will be cancelled, and the line current will have minimal cross-over distortion.

VA Out (Pin 7) (voltage amplifier output): This is the output of the op amp that regulates output voltage. Like the current amplifier, the voltage amplifier will stay active even if the IC is disabled with either ENA or V_{CC}. This means that large feedback capacitors across the amplifier will stay charged through momentary disable cycles. Voltage amplifier output levels below 1V will inhibit multiplier output. The voltage amplifier output is internally limited to approximately 5.8V to prevent overshoot. The voltage amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

V_{RMS} (Pin 8) (RMS line voltage): The output of a boost PWM is proportional to the input voltage, so when the line voltage into a low-bandwidth boost PWM voltage regulator changes, the output will change immediately and slowly recover to the regulated level. For these devices, the V_{RMS} input compensates for line voltage changes if it is connected to a voltage proportional to the RMS input line voltage. For best control, the V_{RMS} voltage should stay between 1.5V and 3.5V.

REF (Pin 9) (voltage reference output): REF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and will remain at 0V when V_{CC} is low or when ENA is low. Bypass REF to Gnd with an 0.1µF or larger ceramic capacitor for best stability.

ENA (Pin 10) (enable): ENA is a logic input that will enable the PWM output, voltage reference, and oscillator. ENA also will release the soft start clamp, allowing SS to rise. When unused, connect ENA to a +5V supply or pull ENA high with a 22k resistor. The ENA pin is not intended to be used as a high speed shutdown to the PWM output.

V_{SENSE} (Pin 11) (voltage amplifier inverting input): This is normally connected to a feedback network and to the boost converter output through a divider network.

R_{SET} (Pin 12) (oscillator charging current and multiplier limit set): A resistor from R_{SET} to ground will program oscillator charging current and maximum multiplier output. Multiplier output current will not exceed 3.75V divided by the resistor from R_{SET} to ground.

SS (Pin 13) (soft start): SS will remain at Gnd as long as the IC is disabled or V_{CC} is too low. SS will pull up to over 8V by an internal 14µA current source when both V_{CC} becomes valid and the IC is enabled. SS will act as the reference input to the voltage amplifier if SS is below REF. With a large capacitor from SS to Gnd, the reference to the voltage regulating amplifier will rise slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.

C_T (Pin 14) (oscillator timing capacitor): A capacitor from C_T to Gnd will set the PWM oscillator frequency according to this relationship:

$$F = \frac{1.25}{R_{SET} \times C_T}$$

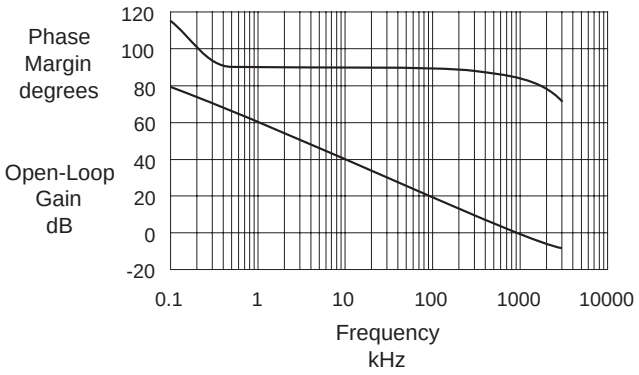
V_{CC} (Pin 15) (positive supply voltage): Connect V_{CC} to a stable source of at least 20mA above 17V for normal operation. Also bypass V_{CC} directly to Gnd to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate GT Drv signals, these devices will be inhibited unless V_{CC} exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

PIN DESCRIPTIONS (cont.)

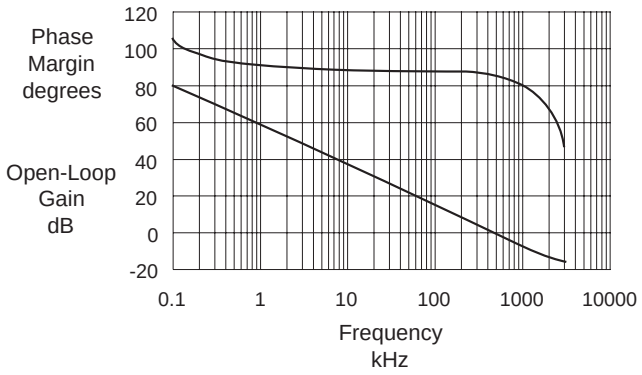
GT Drv (Pin 16) (gate drive): The output of the PWM is a totem pole MOSFET gate driver on GT Drv. This output is internally clamped to 15V so that the IC can be operated with V_{CC} as high as 35V. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GT Drv output driver that might cause the GT Drv output to overshoot excessively. Some overshoot of the GT Drv output is always expected when driving a capacitive load.

TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$

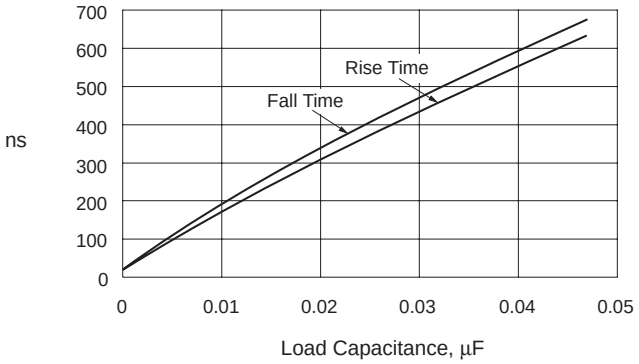
Current Amplifier Gain and Phase vs Frequency



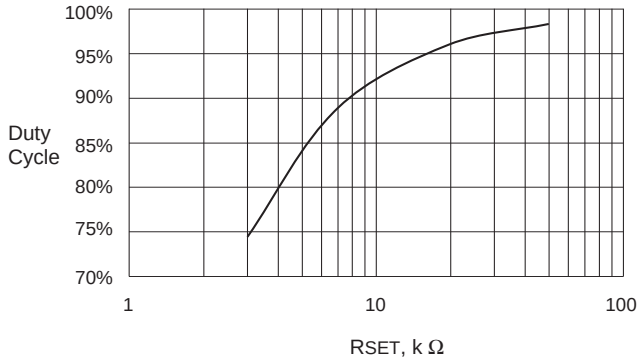
Voltage Amplifier Gain and Phase vs Frequency



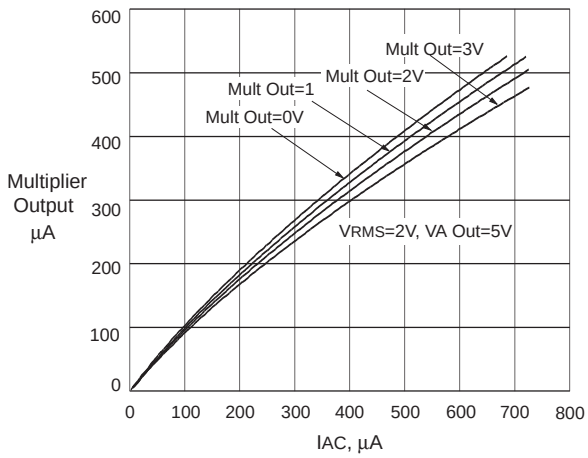
Gate Drive Rise and Fall Time



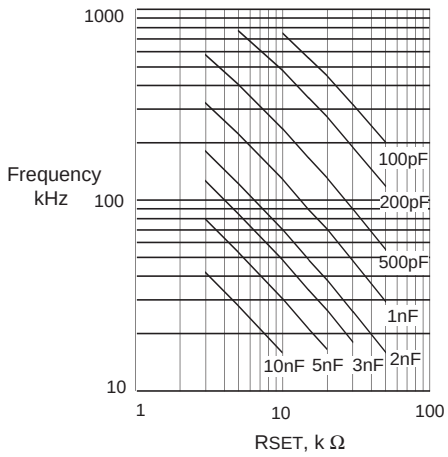
Gate Drive Maximum Duty Cycle



Multiplier Output vs Voltage on Mult

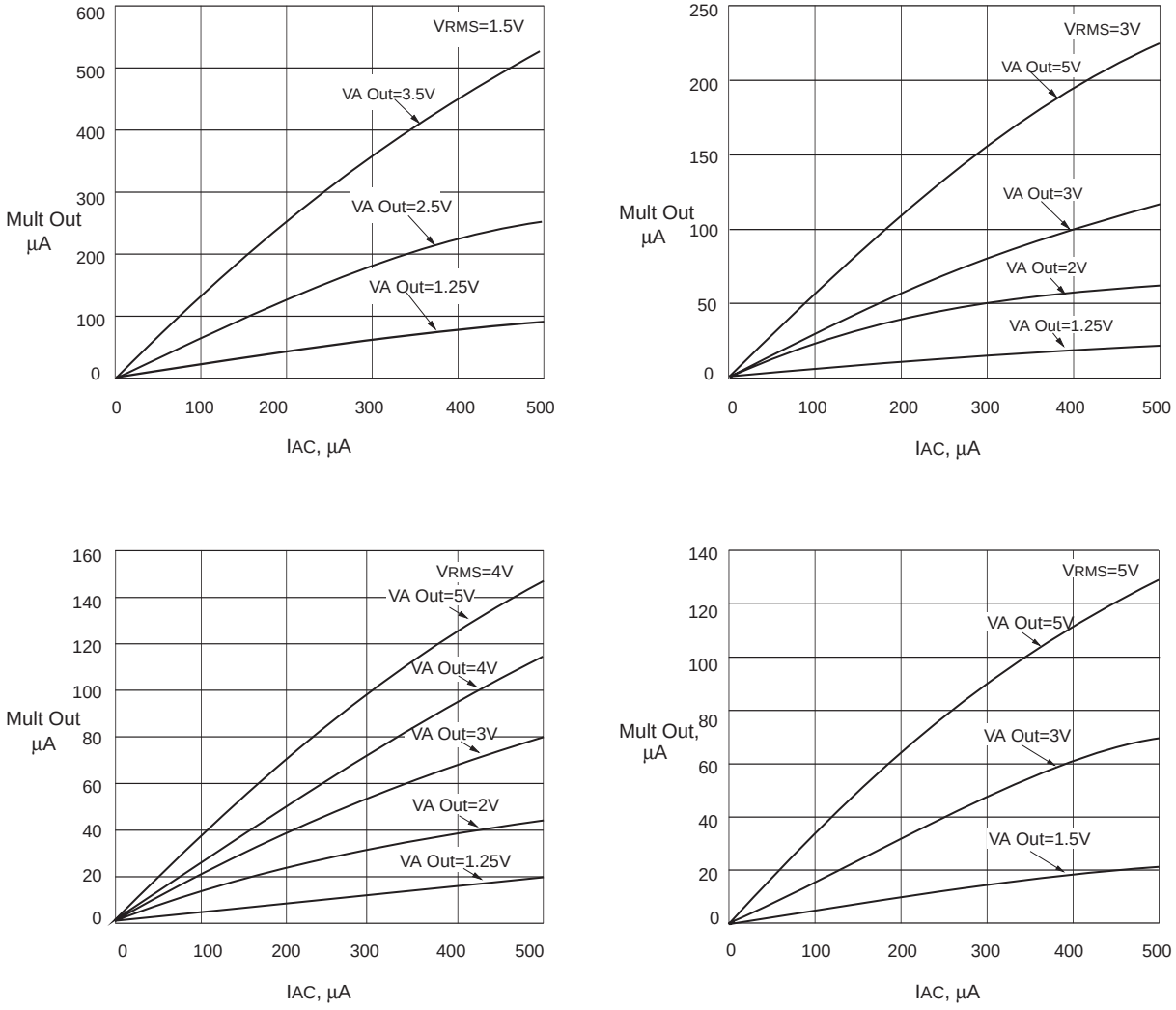


Oscillator Frequency vs R_{SET} and C_T



TYPICAL CHARACTERISTICS at $T_A = T_J = 25^oC$ (cont.)

Multiplier Output vs Multiplier Inputs with Mult Out=0V



APPLICATIONS INFORMATION

A 250W PREREGULATOR

The circuit of Figure 1 shows a typical application of the UC3854 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts, the control circuit centering on the UC3854 and the power section.

The power section is a "boost" converter, with the inductor operating in the continuous mode. In this mode, the duty cycle is dependent on the ratio between input and output voltages; also, the input current has low switching frequency ripple, which means that the line noise is low. Furthermore, the output voltage must be higher than the peak value of the highest expected AC line voltage, and all components must be rated accordingly.

In the control section, the UC3854 provides PWM pulses (GT Drv, Pin 16) to the power MOSFET gate. The duty cycle of this output is simultaneously controlled by four separate inputs to the chip:

INPUT	PIN #	FUNCTION
V_{SENSE}	11	Output DC Voltage
I_{AC}	6	LineVoltage Waveform
I_{SENSE}/Mult Out	4/5	Line Current
V_{RMS}	8	RMS Line Voltage

Additional controls of an auxiliary nature are provided. They are intended to protect the switching power MOSFETS from certain transient conditions, as follows:

INPUT	PIN #	FUNCTION
ENA	10	Start-Up Delay
SS	13	Soft Start
PKLIM	2	Maximum Current Limit

APPLICATIONS INFORMATION (cont.)

PROTECTION INPUTS

ENA (Enable): The ENA input must reach 2.5 volts before the REF and GT Drv outputs are enabled. This provides a means to shut down the gate in case of trouble, or to add a time delay at power up. A hysteresis gap of 200mV is provided at this terminal to prevent erratic operation. Undervoltage protection is provided directly at pin 15, where the on/off thresholds are 16V and 10V. If the ENA input is unused, it should be pulled up to V_{CC} through a current limiting resistor of 100k.

SS (Soft start): The voltage at pin 13 (SS) can reduce the reference voltage used by the error amplifier to regulate the output DC voltage. With pin 13 open, the reference voltage is typically 7.5V. An internal current source delivers approximately -14µA from pin 13. Thus a capacitor connected between that pin and ground will charge linearly from zero to 7.5V in 0.54C seconds, with C expressed in microfarads.

PKLIM (Peak current limit): Use pin 2 to establish the highest value of current to be controlled by the power MOSFET. With the resistor divider values shown in Figure 1, the 0.0V threshold at pin 2 is reached when the voltage drop across the 0.25 ohm current sense resistor is 7.5V*2k/10k=1.5V, corresponding to 6A. A bypass capacitor from pin 2 to ground is recommended to filter out very high frequency noise.

CONTROL INPUTS

V_{SENSE} (Output DC voltage sense): The threshold voltage for the V_{SENSE} input is 7.5V and the input bias current is typically 50nA. The values shown in Figure 1 are for an output voltage of 400V DC. In this circuit, the voltage amplifier operates with a constant low frequency gain for minimum output excursions. The 47nF feedback capacitor places a 15Hz pole in the voltage loop that prevents 120Hz ripple from propagating to the input current.

I_{AC} (Line waveform): In order to force the line current waveshape to follow the line voltage, a sample of the power line voltage in waveform is introduced at pin 6. This signal is multiplied by the output of the voltage amplifier in the internal multiplier to generate a reference signal for the current control loop.
This input is not a voltage, but a current (hence I_{AC}). It is set up by the 220k and 910k resistive divider (see Figure 1). The voltage at pin 6 is internally held at 6V, and the two resistors are chosen so that the current flowing into pin 6 varies from zero (at each zero crossing) to about 400µA at the peak of the waveshape. The following formulas were used to calculate these resistors:

$$R_{AC} = \frac{V_{pk}}{I_{ACpk}} = \frac{260VAC \times \sqrt{2}}{400\mu A} = 910k$$

$$R_{REF} = \frac{R_{AC}}{4} = 220k$$

(where Vpk is the peak line voltage)

I_{SENSE}/Mult Out (Line current): The voltage drop across the 0.25 ohm current-sense resistor is applied to pins 4 and 5 as shown. The current-sense amplifier also operates with high low-frequency gain, but unlike the voltage amplifier, it is set up to give the current-control loop a very wide bandwidth. This enables the line current to follow the line voltage as closely as possible. In the present example, this amplifier has a zero at about 500Hz, and a gain of about 18dB thereafter.

V_{RMS} (RMS line voltage): An important feature of the UC3854 preregulator is that it can operate with a three-to-one range of input line voltages, covering everything from low line in the US (85VAC) to high line in Europe (255VAC). This is done using line feedforward, which keeps the input power constant with varying input voltage (assuming constant load power). To do this, the multiplier divides the line current by the square of the RMS value of the line voltage. The voltage applied to pin 8, proportional to the average of the rectified line voltage (and proportional to the RMS value), is squared in the UC3854, and then used as a divisor by the multiplier block. The multiplier output, at pin 5, is a current that increases with the current at pin 6 and the voltage at pins 7, and decreases with the square of the voltage at pin 8.

PWM FREQUENCY: The PWM oscillator frequency in Figure 1 is 100kHz. This value is determined by C_T at pin 14 and R_{SET} at pin 12. R_{SET} should be chosen first because it affects the maximum value of I_{MULT} according to the equation:

$$I_{MULT_{MAX}} = \frac{-3.75V}{R_{SET}}$$

This effectively sets a maximum PWM-controlled current. With R_{SET}=15k,

$$I_{MULT_{MAX}} = \frac{-3.75V}{15k} = -250\mu A$$

Also note that the multiplier output current will never exceed twice I_{AC}.

With the 4k resistor from Mult Out to the 0.25 ohm current sense resistor, the maximum current in the current sense resistor will be

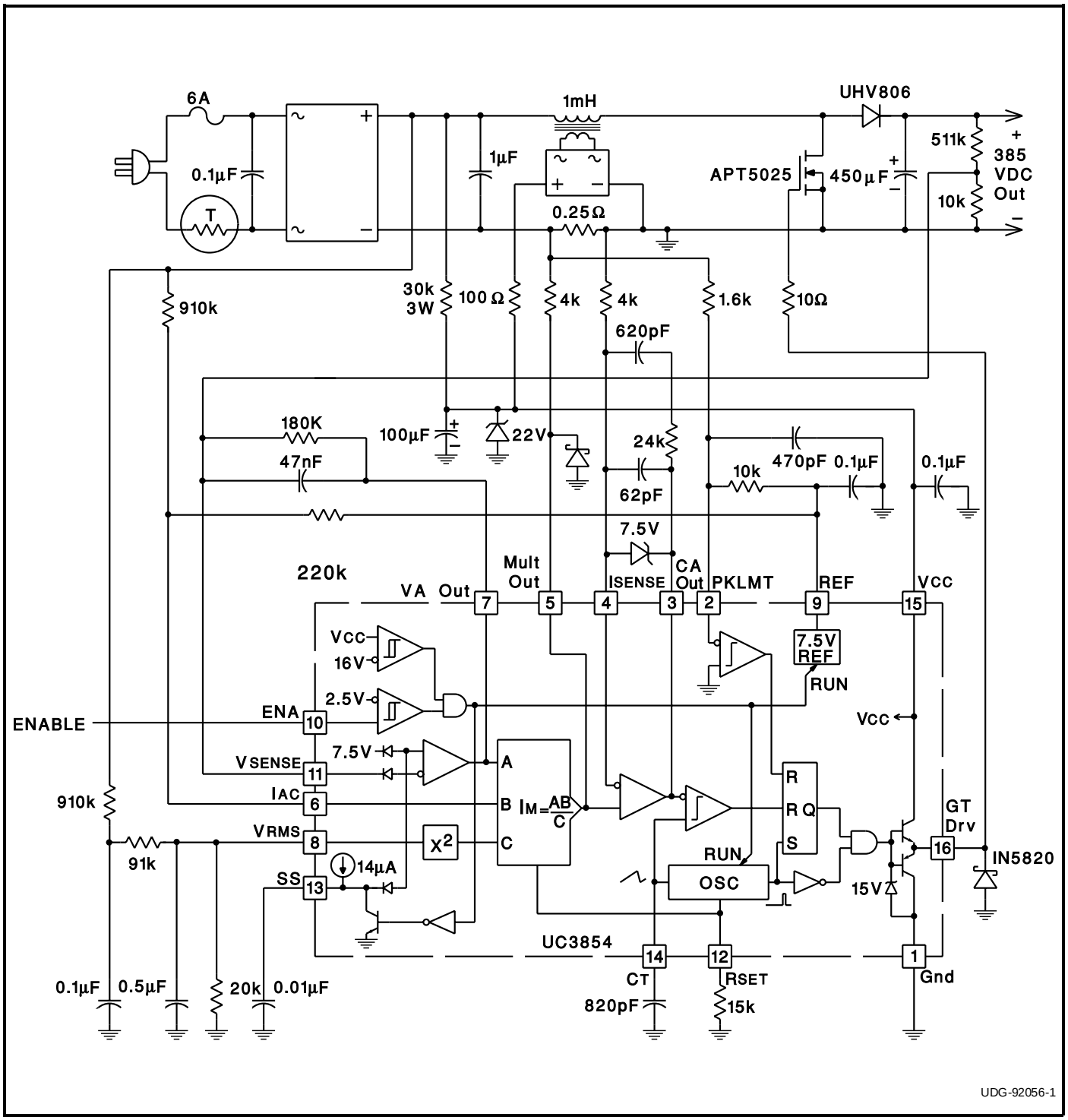
$$I_{MAX} = \frac{-I_{MULT_{MAX}} \times 4k}{0.25\Omega} = -4A$$

Having thus selected R_{SET}, the current sense resistor, and the resistor from Mult Out to the current sense resistor, calculate C_T for the desired PWM oscillator frequency from the equation

$$C_T = \frac{1.25}{F \times R_{SET}}$$

FIGURE 1 - Typical Application

This diagram depicts a complete 250 Watt Preregulator. At full load, this preregulator will exhibit a power factor of 0.99 at any power line voltage between 80 and 260 VRMS. This same circuit can be used at higher power levels with minor modifications to the power stage. See Design Note 39B and Application Note U-134 for further details.



NOTE: Boost inductor can be fabricated with ARNOLD MPP toroidal core part number A-438381-2, using a 55 turn primary and a 13 turn secondary.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9326101M2A	OBSOLETE	TO/SOT	L	20		TBD	Call TI	Call TI
5962-9326101MEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1854J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1854J883B	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1854L	OBSOLETE	TO/SOT	L	20		TBD	Call TI	Call TI
UC1854L883B	OBSOLETE	TO/SOT	L	20		TBD	Call TI	Call TI
UC2854BJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC2854DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2854DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2854DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2854DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2854N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2854NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3854DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3854DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3854DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3854DWTR-FG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3854DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3854N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3854NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3854Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3854QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3854QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3854QTRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

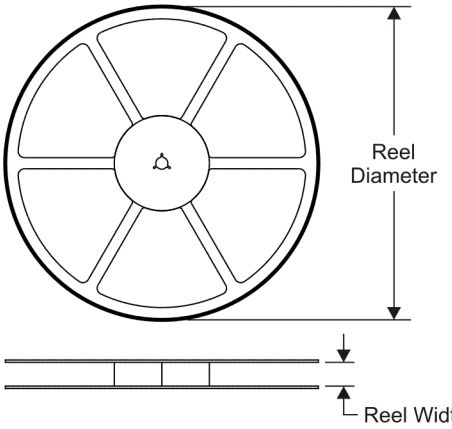
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

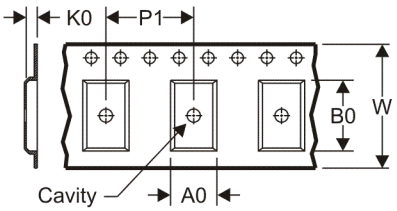
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

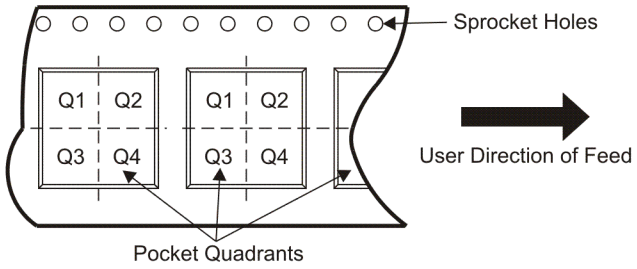


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

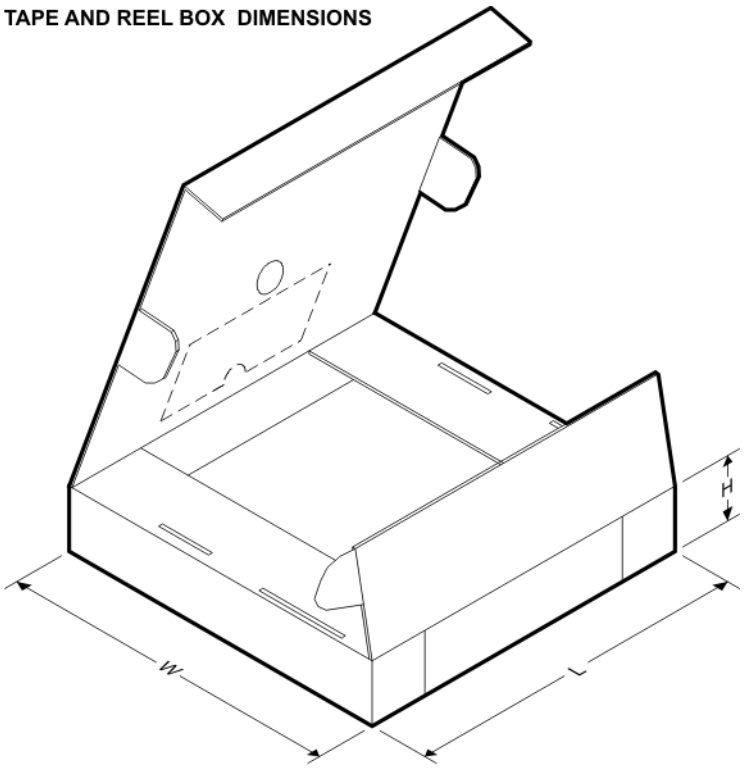
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2854DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3854DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2854DWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3854DWTR	SOIC	DW	16	2000	346.0	346.0	33.0

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