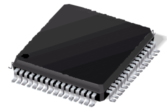
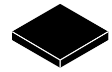




PROGRAMMABLE TOUCH SCREEN CONTROLLER WITH STEREO AUDIO CODEC

FEATURES

- **SPI™ Serial Interface**
- **Touch Screen Controller**
  - **– 4-Wire Touch Screen Interface**
  - **– Internal Detection of Screen Touch and Keypad Press**
  - **– Touch Pressure Measurement**
  - **– Ratiometric Conversion**
  - **– Programmable 8-, 10- or 12-Bit Resolution**
  - **– Programmable Sampling Rates Up to 125 kHz**
  - **– Direct Battery Measurement (0 to 6 V)**
  - **– On-Chip Temperature Measurement**
  - **– 4-by-4 Keypad Interface With Programmable De-Bounce and Key Masking**
  - **– Integrated Touch Screen Processor Reduces Host CPU Interrupts and Overhead**
  - **– Internal Timing Control With Programmable Delays and Averaging**
- **Stereo Audio Codec**
  - **– 20-Bit Delta-Sigma ADC/DAC**
  - **– Dynamic Range: 98 dB**
  - **– Sampling Rate Up to 48 kHz**
  - **– I^2S Serial Interface**
  - **– Stereo 16-Ω Headphone Driver**
- **Full Power-Down Control**
- **8-Bit Current Output DAC**
- **On-Chip Crystal Oscillator**
- **Programmable Bass/ Midrange/ Treble EQ Effects Processing**
- **6 GPIO Pins**
- **Single 2.7-V to 3.6-V Supply**
- **64-Pin TQFP Package**
- **120-Ball MicroStar Junior™ BGA Package**

APPLICATIONS

- **Personal Digital Assistants**
- **Cellular Phones**
- **MP3 Players**
- **Internet Appliances**
- **Smartphones**

DESCRIPTION

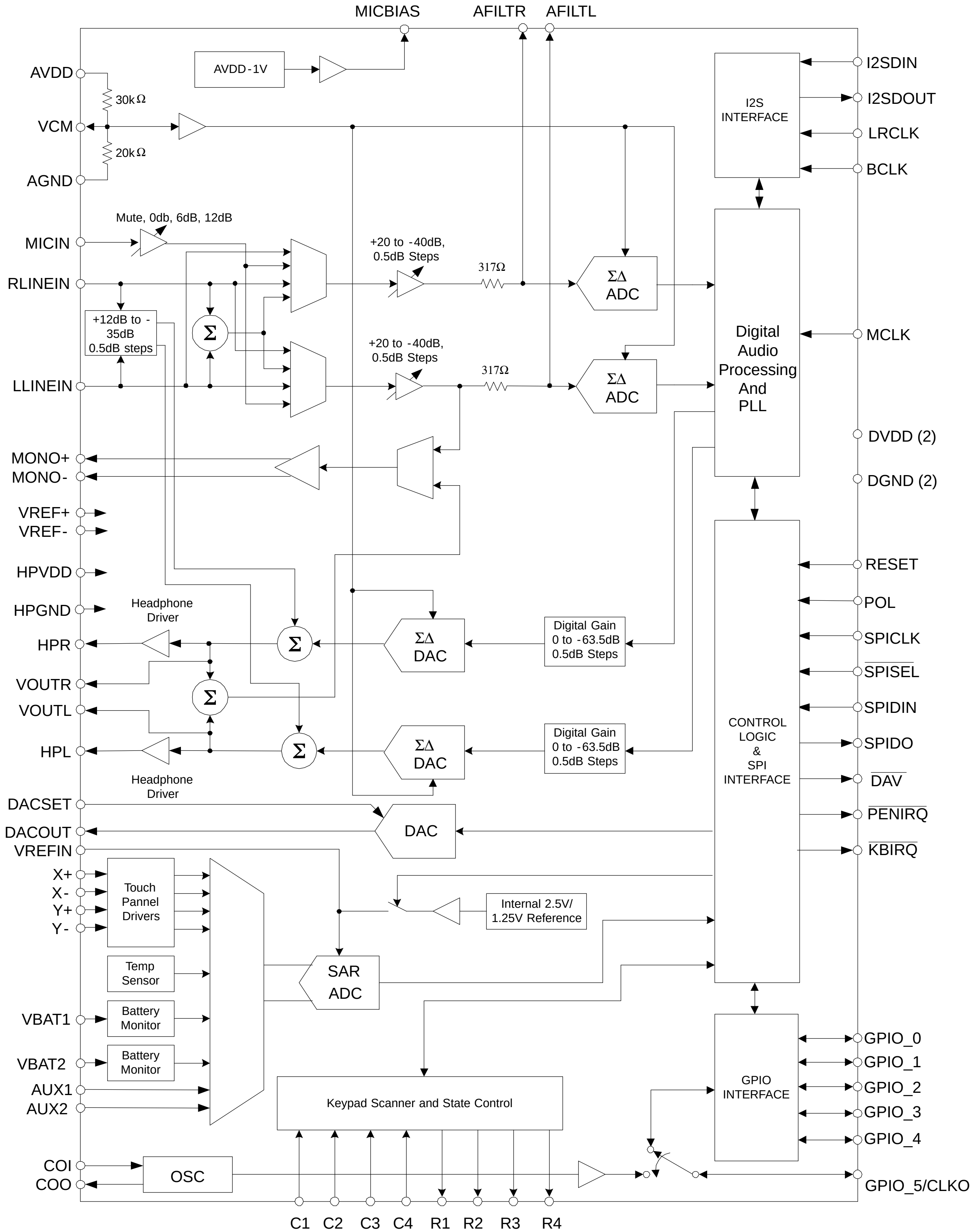
The TSC2301 is a highly integrated PDA analog interface circuit. It contains a complete 12-bit A/D resistive touch screen converter (ADC) including drivers, touch pressure measurement capability, keypad controller, and 8-bit D/A converter (DAC) output for LCD contrast control. The TSC2301 offers programmable resolution of 8, 10, and 12 bits and sampling rates up to 125 kHz to accommodate different screen sizes. The TSC2301 interfaces to the host controller through a standard SPI serial interface.

The TSC2301 features a high-performance 20-bit, 48-ksps stereo audio codec with highly integrated analog functionality. The audio portion of the TSC2301 contains microphone input with built-in pre-amp and microphone bias circuit, an auxiliary stereo analog input, a stereo line-level output, a differential mono line-level output, and a stereo headphone amplifier output. The digital audio data is transferred through a standard I^2S interface. A fully programmable PLL for generating audio clocks from a wide variety of system clocks is also included.

The TSC2301 also offers two battery measurement inputs capable of battery voltages up to 6 V, while operating at a supply voltage of only 2.7 V. It also has an on-chip temperature sensor capable of reading 0.3°C resolution. The TSC2301 is available in 64-lead TQFP, and 120-ball VFBGA packages.

US Patent No. 6246394

FUNCTIONAL BLOCK DIAGRAM


MICBIAS
AFILTR
AFILTL
AVDD
VCM
AGND
AVDD-1V
30kΩ
20kΩ
I2SDIN
I2SDOUT
LRCLK
BCLK
I2S INTERFACE
MICIN
RLINEIN
LLINEIN
Mute, 0db, 6dB, 12dB
+20 to -40dB, 0.5dB Steps
+12dB to -35dB 0.5dB steps
317Ω
ΣΔ ADC
Digital Audio Processing And PLL
MCLK
DVDD (2)
DGND (2)
MONO+
MONO-
VREF+
VREF-
HPVDD
HPGND
Headphone Driver
HPR
VOUTR
VOUTL
HPL
ΣΔ DAC
Digital Gain 0 to -63.5dB 0.5dB Steps
RESET
POL
SPICLK
SPISEL
SPIDIN
SPIDO
DAV
PENIRQ
KBIRQ
CONTROL LOGIC & SPI INTERFACE
DACSET
DACOUT
VREFIN
DAC
X+
X-
Y+
Y-
Touch Pannel Drivers
Internal 2.5V/ 1.25V Reference
Temp Sensor
SAR ADC
VBAT1
VBAT2
Battery Monitor
AUX1
AUX2
Keypad Scanner and State Control
GPIO INTERFACE
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5/CLKO
COI
COO
OSC
C1
C2
C3
C4
R1
R2
R3
R4

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA QUANTITY
TSC2301I	TQFP-64	PAG	–40°C to 85°C	TSC2301IPAG	Trays, 160
				TSC2301IPAGR	Tape and reel, 1500
	VFBGA-120	GQZ		TSC2301IGQZ	Trays, 250
				TSC2301IGQZR	Tape and reel, 2500
		ZQZ		TSC2301IZQZ	Trays, 250
				TSC2301IZQZR	Tape and reel, 2500

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TSC2301
Supply voltage	AVDD, HPVDD, DVDD	4 V
Ground voltage differences	AGND, DGND	±0.1 V
Digital input voltage		-0.3 V to (DV_{DD} + 0.3 V)
Analog input voltage		-0.3 V to (AV_{DD} + 0.3 V)
Ambient temperature under bias, T_A		-40°C to 125°C
Storage temperature, T_{stg}		-55°C to 150°C
Junction temperature, T_J		150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At 25°C, $HPV_{DD} = AV_{DD} = DV_{DD}$ = +3.3 V, V_{REF} = External 2.5 V, unless otherwise noted.

Parameter		Conditions	TSC2301			Units
			Min	Typ	Max	
Auxilary Analog Inputs						
Input voltage range			0		+VREFIN	V
Input capacitance				25		ρF
Input leakage current				1		μA
Battery Monitor Input						
Input voltage range			0		6.0	V
Input capacitance				25		ρF
Input leakage current				±1		μA
Temperature Measurement						
Temperature range			-40		+85	°C
Temperature resolution				0.3		°C
Accuracy				±2		°C
Touch Screen A/D Converter						
Resolution		Programmable: 8-, 10-,12-Bits			12	Bits
No missing codes		12-bit resolution		10		Bits
Integral linearity					±6	LSB
Offset error					±6	LSB
Gain error	TSC2301IPAG				±6	LSB
	TSC2301IGQZ				±10	
Noise				<300		μV RMS
Audio Codec						
Sampling frequency					48	kHz
Audio I/O						
Audio in		Line, Mic inputs	0.15* AVDD		0.65* AVDD	V
Audio out		Line outputs	0.15* AVDD		0.65* AVDD	V
Audio ADC		ADC performance measured using Fs = 48 kHz				
Signal-to-noise ratio, A-weighted		No input	80	88		dB
Total harmonic distortion		1 kHz, -0.5 dB input		-70	-60	dB
Full-scale input voltage				0.18* AVDD		Vrms
Transition band			0.45 Fs		0.55 Fs	Hz
Stop band			0.55 Fs		127 Fs	Hz
Stop band rejection				70dB		
Audio DAC		DAC performance measured at Line Outputs using Fs = 48 kHz				
Full-scale output voltage				0.18* AVDD		Vrms
Signal-to-noise ratio, A-weighted		No input		98		dB
Total harmonic distortion		1-kHz, 0-dB input		-100		dB
Frequency response			20		0.45 Fs	Hz
Transition band			0.45 Fs		0.55 Fs	Hz
Stop band			0.55 Fs		3.5 Fs	Hz
Stop band rejection				65		dB
Headphone Driver		DAC playback through headphone driver				

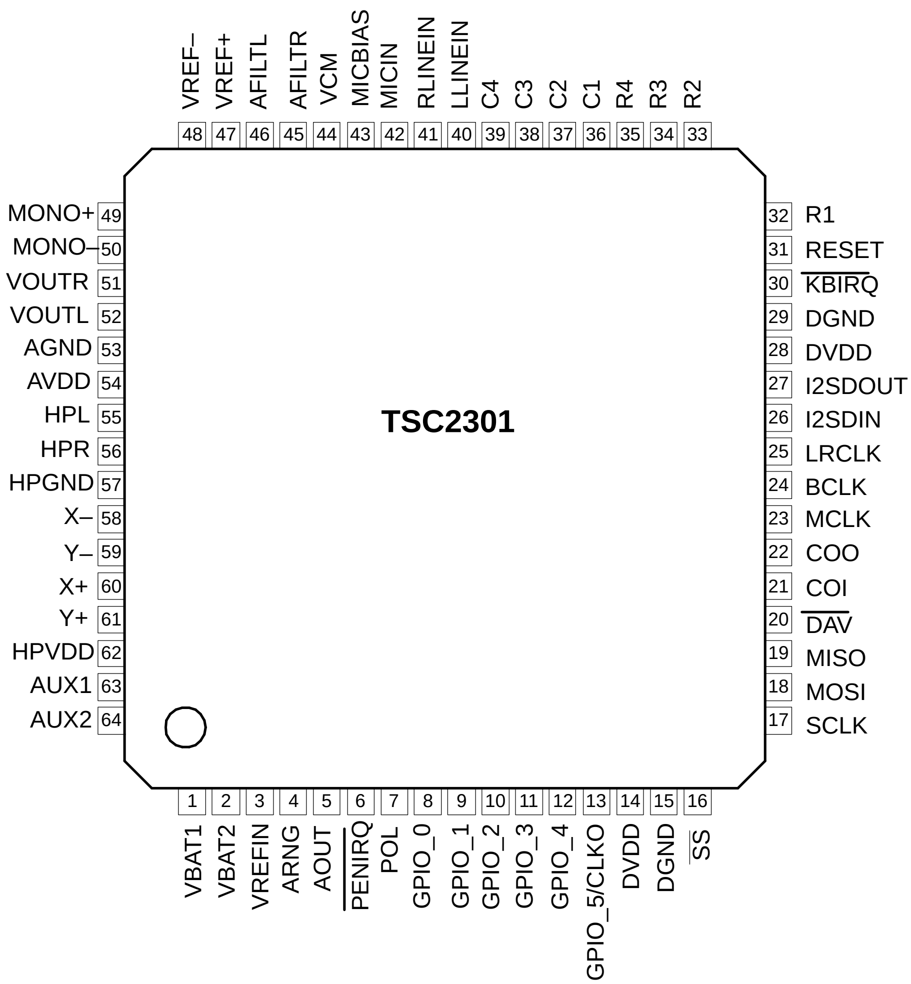
ELECTRICAL CHARACTERISTICS (continued)

At 25°C, HPV_{DD} = AV_{DD} = DV_{DD} = +3.3 V, V_{REF} = External 2.5 V, unless otherwise noted.

Parameter		Conditions	TSC2301 Min	TSC2301 Typ	TSC2301 Max	Units
Output power per channel		R = 32 Ω		14		mW
		R = 16 Ω		27		mW
		R = 16 Ω V_{DD} = 3.6V		32		mW
Signal-to-noise ratio, A-weighted			85	96		dB
Total harmonic distortion		R = 32 Ω 1-kHz, 0-dB input		-83	-70	dB
		R = 16 Ω 1-kHz, -3-dB input		-77		dB
D/A Converter						
Output current range		Measured with ARNG floating	0.75	1.10		mA
Resolution					8	Bits
Voltage Reference						
Voltage range	TSC2301IPAG	Internal 2.5 V	2.34	2.49	2.54	V
	TSC2301IGQZ		2.34	2.49	2.64	
Reference drift				50		ppm/°C
Current drain				20		µA
Digital Input / Output						
Internal clock frequency				8.8		MHz
Logic family				CMOS		
Logic level: V_{IH}		I_{IH} = 5 µA	0.7 V_{DD}			V
V_{IL}		I_{IL} = 5 µA	-0.3		0.3 V_{DD}	V
V_{OH}		I_{OH} = 2 TTL loads	0.8* DVDD			V
V_{OL}		I_{OL} = 2 TTL loads			0.2* DVDD	V
Power Supply Requirements						
Power supply voltage						
DV_{DD}, AV_{DD}, HPV_{DD}			2.7		3.6	V
Quiescent current (1)						
Touch screen only		1-kHz SAR sample rate, external V_{ref}		14		µA
Touch screen only		20-kHz SAR sample rate, internal V_{ref}		1.7		mA
Stereo playback only		44.1-kHz Playback, V_{DD} = 2.7V		10		mA
Voice record only		Mono 8-kHz record, V_{DD} = 2.7V		5.8		mA
Power down		Audio fully powered down		.05		µA

(1) For more details on power consumption, see the Audio Codec section of the description overview.

PIN ASSIGNMENT
(TOP VIEW)



PIN DESCRIPTION

VFBGA BALL	TQFP PIN	I/O	NAME	DESCRIPTION
A10	1	I	VBAT1	Battery monitor input 1
B9	2	I	VBAT2	Battery monitor input 2
A9	3	I/O	VREFIN	SAR reference voltage
B8	4		ARNG	DAC analog output range set
A8	5	O	AOUT	Analog output current from DAC
A7	6	O	PENIRQ	Pen interrupt
B6	7	I	POL	SPI clock polarity
A6	8	I/O	GPIO_0	General-purpose input/output pin
A5	9	I/O	GPIO_1	General-purpose input/output pin
B4	10	I/O	GPIO_2	General-purpose input/output pin
A4	11	I/O	GPIO_3	General-purpose input/output pin
B3	12	I/O	GPIO_4	General-purpose input/output pin
A3	13	I/O	GPIO_5/CLKO	General-purpose input/output pin/buffered oscillator clock out
NC	14	I	DVDD	Digital voltage supply
A2	15	I	DGND	Digital ground

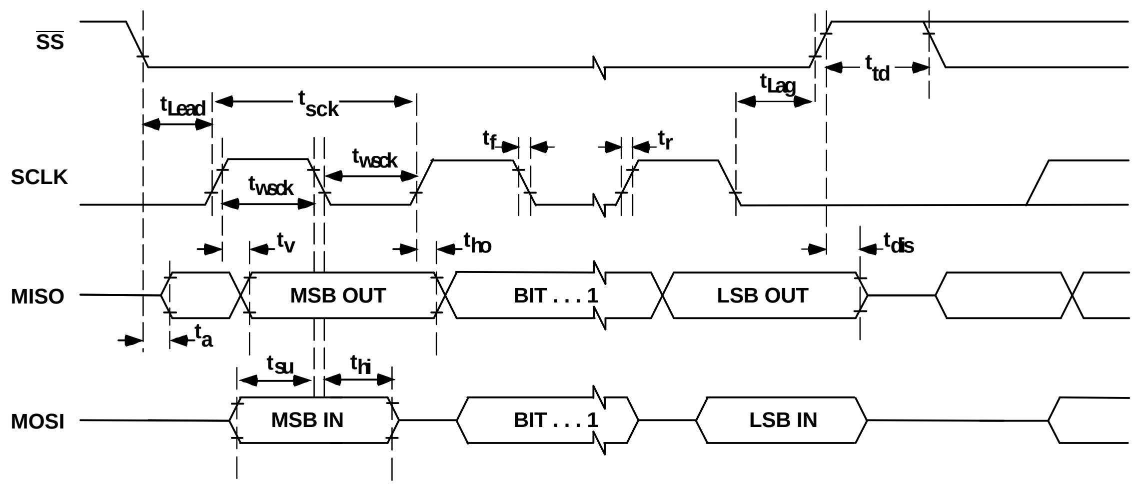
PIN DESCRIPTION (continued)

VFBGA BALL	TQFP PIN	I/O	NAME	DESCRIPTION
B2	16	I	$\overline{SS}$	Slave select input (active low). Data is not clocked into MOSI unless $\overline{SS}$ is low. When $\overline{SS}$ is high, MISO is high impedance.
B1	17	I	SCLK	SPI clock input
C2	18	I	MOSI	SPI data input. Data is clocked in at SCLK rising edge
C1	19	O	MISO	SPI data output. Data is clocked out at SCLK falling edge. High impedance when $\overline{SS}$ is high.
D2	20	O	$\overline{DAV}$	Data available (active low).
D1	21	I	COI	Crystal input
E2	22	O	COO	Crystal output
E1	23	I	MCLK	Master clock input for audio codec
F2	24	I	BCLK	I^2S bit clock
F1	25	I	LRCLK	I^2S left/right clock
G1	26	I	I2SDIN	I^2S serial data in
G2	27	O	I2SDOUT	I^2S serial data out
H1	28	I	DVDD	Digital voltage supply
J1	29	I	DGND	Digital ground
J2	30	O	$\overline{KBIRQ}$	Keypad interrupt (active low). Indicates a key has been depressed
K1	31	I	RESET	Device reset (active high)
K2	32	O	R1	Keypad row 1
L2	33	O	R2	Keypad row 2
K3	34	O	R3	Keypad row 3
L3	35	O	R4	Keypad row 4
K4	36	I	C1	Keypad column 1
L4	37	I	C2	Keypad column 2
K5	38	I	C3	Keypad column 3
L5	39	I	C4	Keypad column 4
L6	40	I	LLINEIN	Left-channel analog input to audio codec
L7	41	I	RLINEIN	Right-channel analog input to audio codec
K7	42	I	MICIN	Analog input from microphone
L8	43	O	MICBIAS	Bias voltage output
K8	44	O	VCM	Common-mode voltage bypass capacitor
L9	45	O	AFILTR	Right-channel audio ADC antialiasing filter capacitor
K9	46	O	AFILTL	Left-channel audio ADC antialiasing filter capacitor
L10	47	I	VREF+	Audio codec positive reference voltage
K10	48	I	VREF-	Audio codec negative reference voltage
K11	49	O	MONO+	Mono differential output
J10	50	O	MONO-	Mono differential output
J11	51	O	VOUTR	Audio right line output
H10	52	O	VOUTL	Audio left line output
H11	53	I	AGND	Analog ground
G10	54	I	AVDD	Analog supply
G11	55	O	HPL	Headphone amplifier left output
F10	56	O	HPR	Headphone amplifier right output
F11	57	I	HPGND	Analog ground for headphone amplifier and touch screen circuitry
E11	58	I	X-	X- position input
E10	59	I	Y-	Y- position input
D11	60	I	X+	X+ position input

PIN DESCRIPTION (continued)

VFBGA BALL	TQFP PIN	I/O	NAME	DESCRIPTION
D10	61	I	Y+	Y+ position input
C11	62	I	HPVDD	Analog supply for headphone amplifier and touch screen circuitry
B11	63	I	AUX1	SAR auxiliary analog input 1
B10	64	I	AUX2	SAR auxiliary analog input 2

TIMING DIAGRAM



TIMING CHARACTERISTICS (1)(2)

All specifications typical at -40°C to +85°C, $+V_{DD}$ = +2.7 V, POL = 1

Parameter	Symbol	Min	Max	Units
SCLK period	t_{sck}	30		ns
Enable lead time	t_{Lead}	15		ns
Enable lag time	t_{Lag}	15		ns
Sequential transfer delay	t_{td}	30		ns
Data setup time	t_{su}	10		ns
Data hold time (inputs)	t_{hi}	10		ns
Data hold time (outputs)	t_{ho}	0		ns
Slave access time	t_a		15	ns
Slave DOUT disable time	t_{dis}		15	ns
Data valid	t_v		10	ns
Rise time	t_r		30	ns
Fall time	t_f		30	ns

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagram, above.

TYPICAL CHARACTERISTICS

At T_A = +25°C, $+V_{DD}$ = +3.3 V, V_{REF} = +2.5 V, f_{SAMPLE} = 125 kHz, unless otherwise noted.

CHANGE IN GAIN ERROR
vs
TEMPERATURE

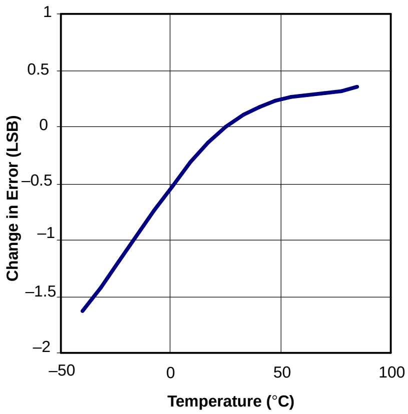


Figure 1.

CHANGE IN OFFSET ERROR
vs
TEMPERATURE

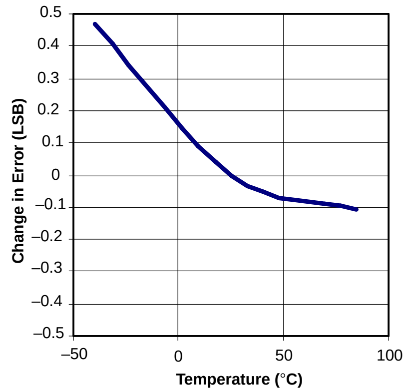


Figure 2.

CONVERSION SUPPLY CURRENT
vs
TEMPERATURE

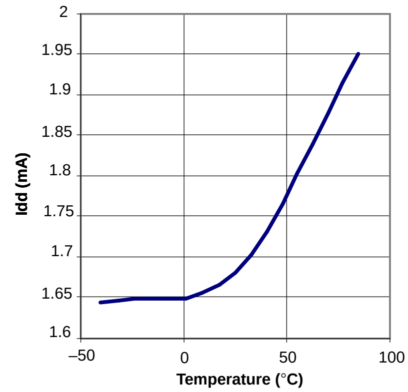


Figure 3.

TOUCH SCREEN DRIVER
ON-RESISTANCE
vs
TEMPERATURE

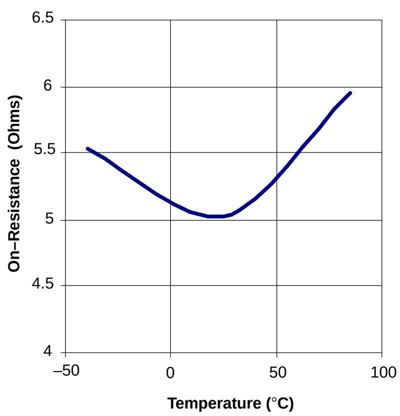


Figure 4.

INTERNAL 1.25-V REFERENCE
vs
TEMPERATURE

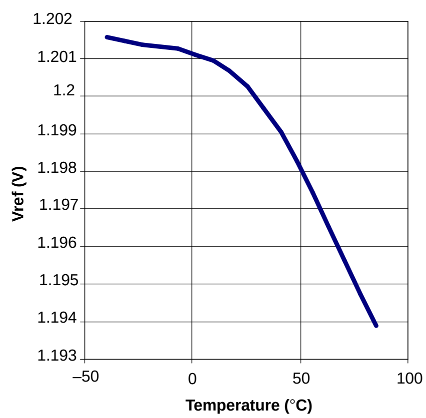


Figure 5.

INTERNAL OSCILLATOR
FREQUENCY
vs
TEMPERATURE

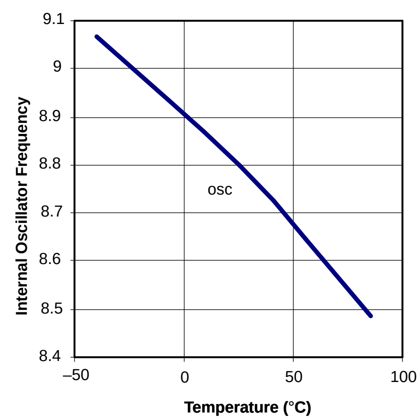


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, +V_{DD} = +3.3 V, V_{REF} = +2.5 V, f_{SAMPLE} = 125 kHz, unless otherwise noted.

INTERNAL 2.5-V REFERENCE vs TEMPERATURE

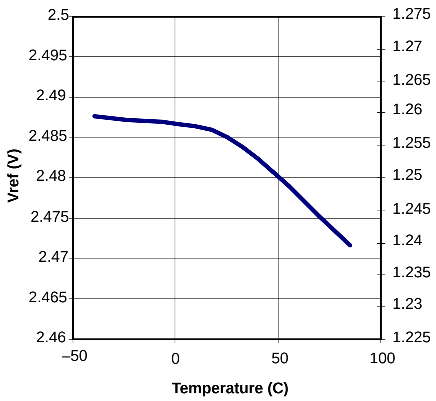


Figure 7.

DAC OUTPUT CURRENT vs TEMPERATURE

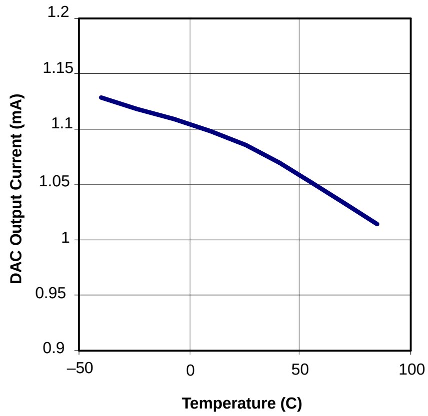


Figure 8.

TEMP2 DIODE VOLTAGE vs TEMPERATURE

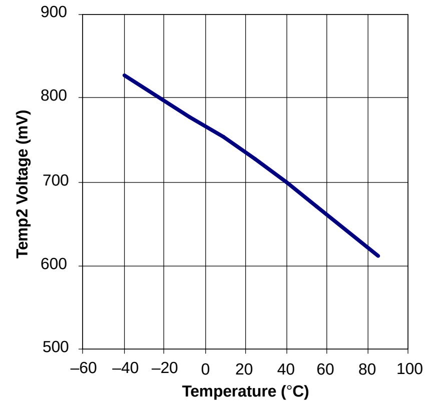


Figure 9.

TEMP1 DIODE VOLTAGE vs TEMPERATURE

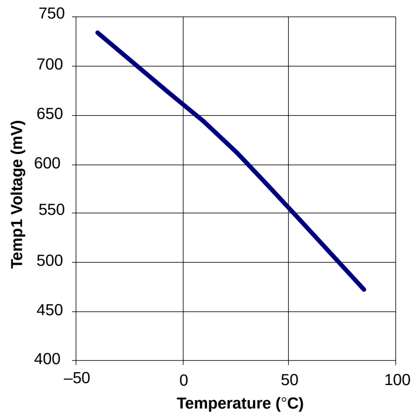


Figure 10.

MICBIAS vs TEMPERATURE

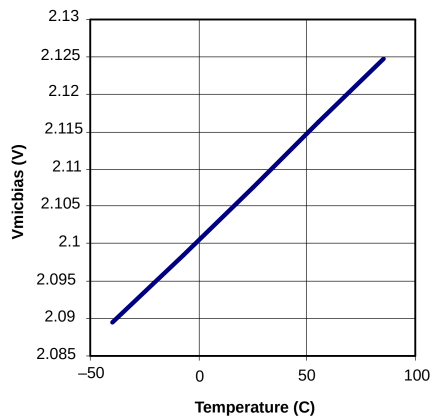


Figure 11.

THD OF DAC (LINEOUT) vs TEMPERATURE

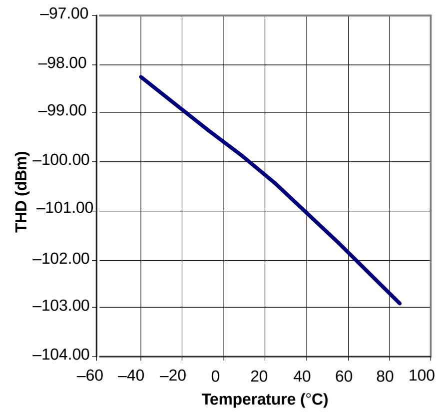


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, +V_{DD} = +3.3 V, V_{REF} = +2.5 V, f_{SAMPLE} = 125 kHz, unless otherwise noted.

SNR OF DAC (LINEOUT)
vs
TEMPERATURE

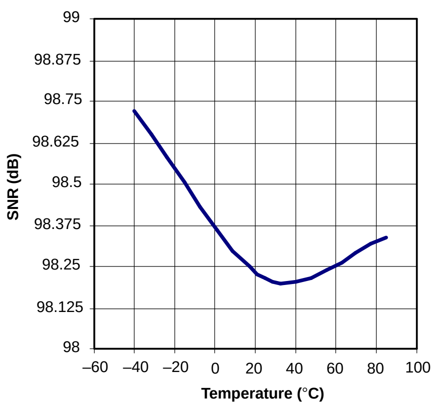


Figure 13.

THD OF ADC (LINEIN)
vs
TEMPERATURE

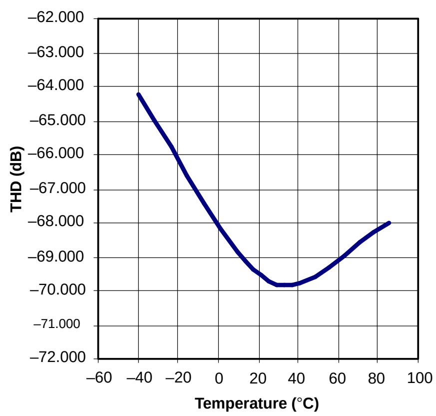


Figure 14.

SNR OF ADC (LINEIN)
vs
TEMPERATURE

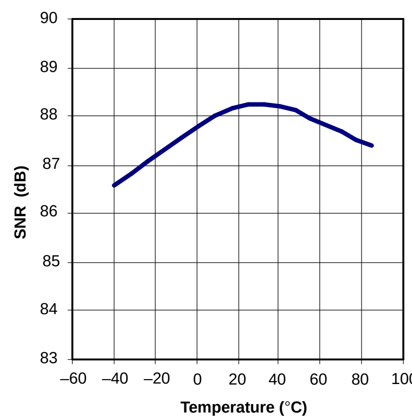


Figure 15.

THD OF DAC (HP DRIVER), 32-Ω LOAD
vs
TEMPERATURE

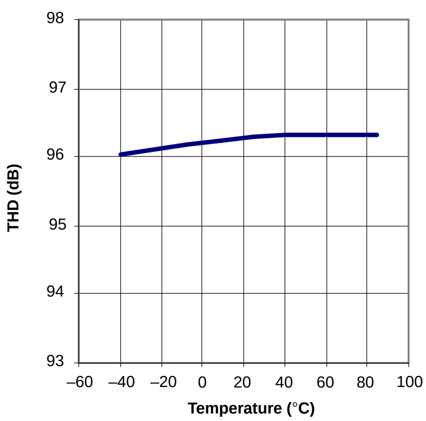


Figure 16.

SNR OF DAC (HP DRIVER)
vs
TEMPERATURE

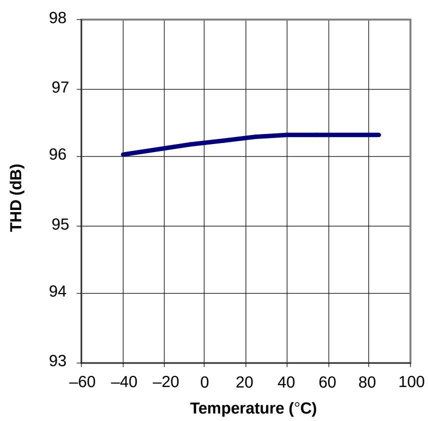


Figure 17.

THD OF BYPASS PATH
vs
TEMPERATURE

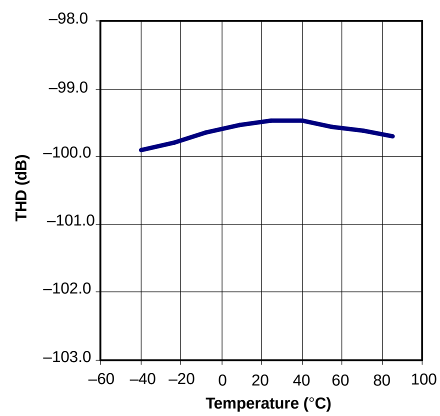


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, $+V_{DD}$ = +3.3 V, V_{REF} = +2.5 V, f_{SAMPLE} = 125 kHz, unless otherwise noted.

SNR OF BYPASS PATH vs TEMPERATURE

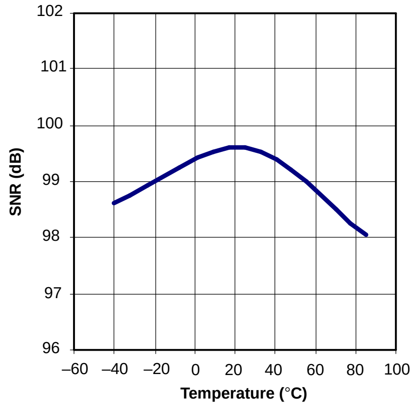


Figure 19.

THD OF MONO PATH vs TEMPERATURE

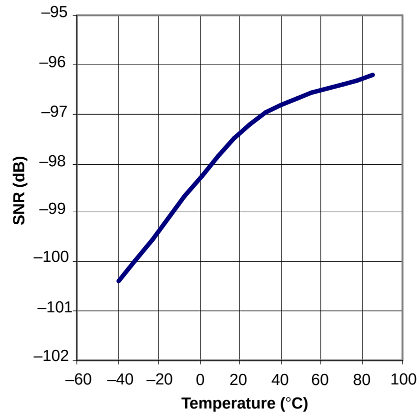


Figure 20.

SNR OF MONO PATH vs TEMPERATURE

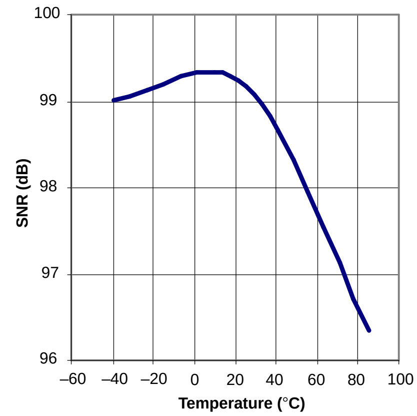


Figure 21.

1.25-V REFERENCE vs SUPPLY VOLTAGE

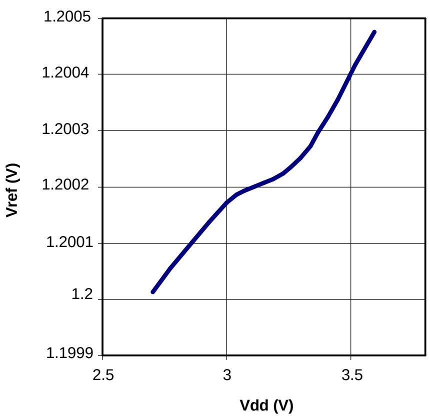


Figure 22.

2.5-V INTERNAL REFERENCE vs SUPPLY VOLTAGE

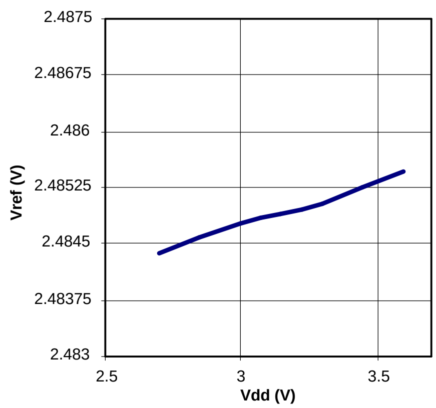


Figure 23.

SWITCH ON-RESISTANCE vs SUPPLY VOLTAGE

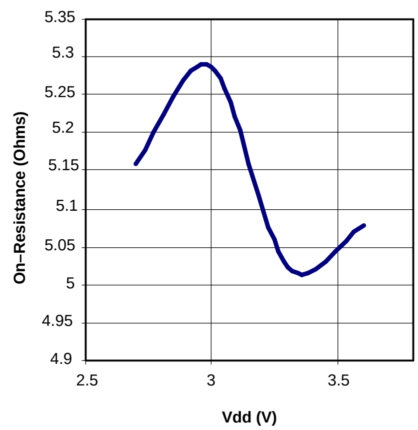


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, $+V_{DD}$ = +3.3 V, V_{REF} = +2.5 V, f_{SAMPLE} = 125 kHz, unless otherwise noted.

TEMP2 DIODE VOLTAGE vs SUPPLY VOLTAGE

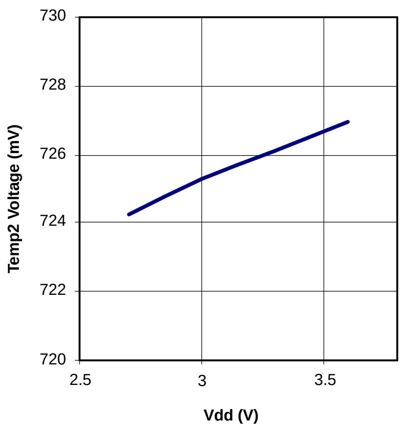


Figure 25.

TEMP1 DIODE VOLTAGE vs SUPPLY VOLTAGE

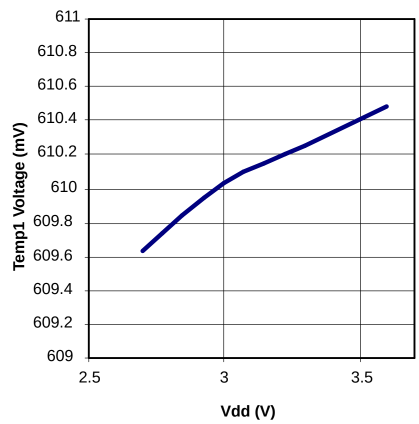


Figure 26.

INTERNAL OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

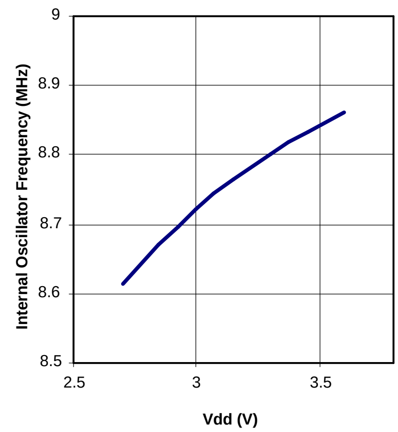


Figure 27.

DAC MAXIMUM CURRENT vs SUPPLY VOLTAGE

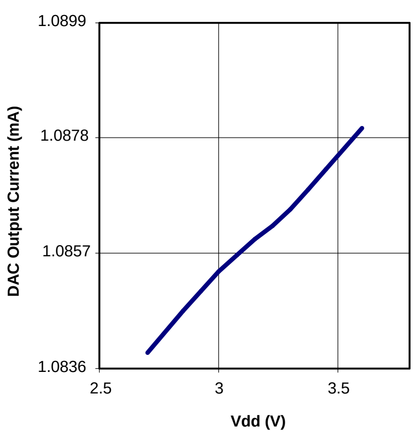


Figure 28.

PD SUPPLY CURRENT vs SUPPLY VOLTAGE

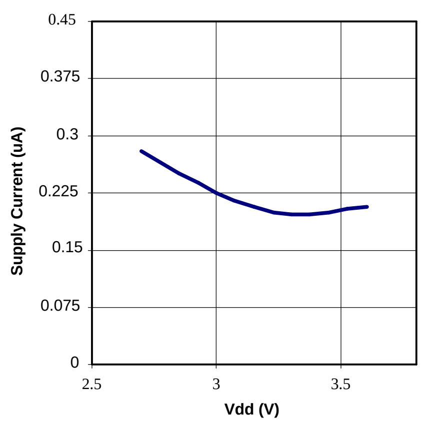


Figure 29.

INL MAXIMUM vs SUPPLY VOLTAGE

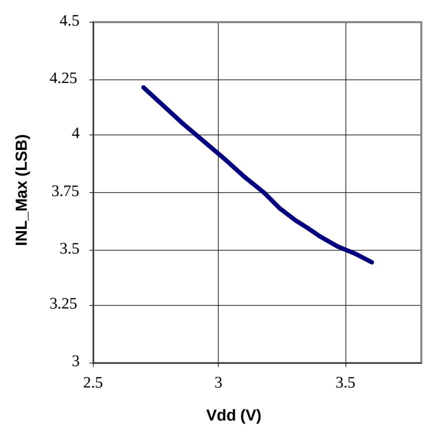


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, +V_{DD} = +3.3 V, V_{REF} = +2.5 V, f_{SAMPLE} = 125 kHz, unless otherwise noted.

INL MINIMUM vs SUPPLY VOLTAGE

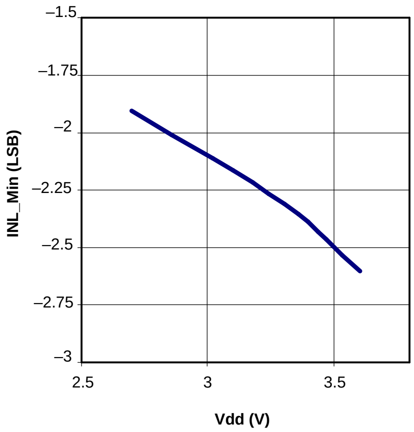


Figure 31.

CONVERSION SUPPLY CURRENT vs SUPPLY VOLTAGE

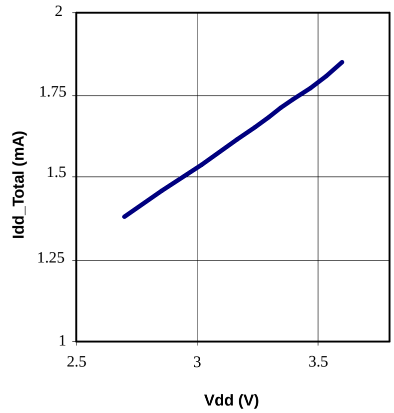


Figure 32.

MICBIAS vs SUPPLY VOLTAGE

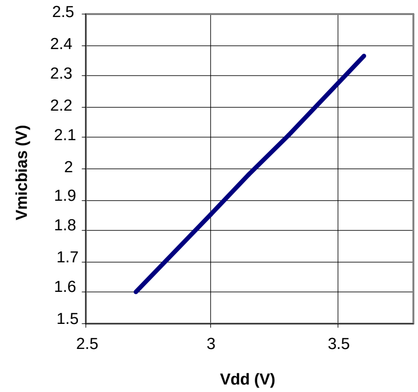


Figure 33.

THD OF DAC (LINEOUT) vs SUPPLY VOLTAGE

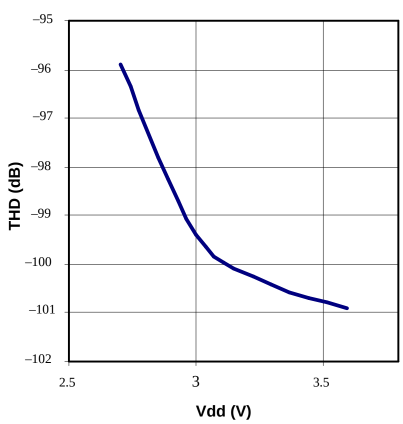


Figure 34.

SNR OF DAC (LINEOUT) vs SUPPLY VOLTAGE

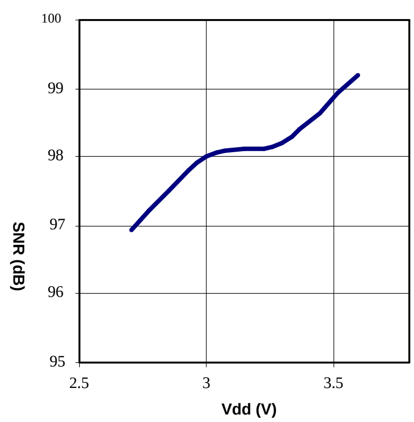


Figure 35.

THD OF ADC (LINEIN) vs SUPPLY VOLTAGE

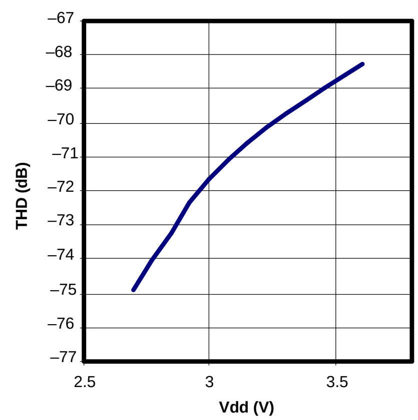


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, +V_{DD} = +3.3 V, V_{REF} = +2.5 V, f_{SAMPLE} = 125 kHz, unless otherwise noted.

SNR OF ADC (LINEIN)
vs
SUPPLY VOLTAGE

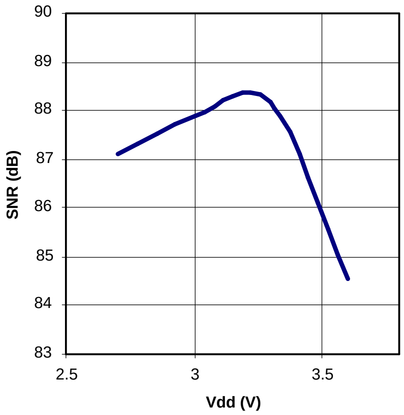


Figure 37.

THD OF DAC (HP DRIVER)
vs
SUPPLY VOLTAGE

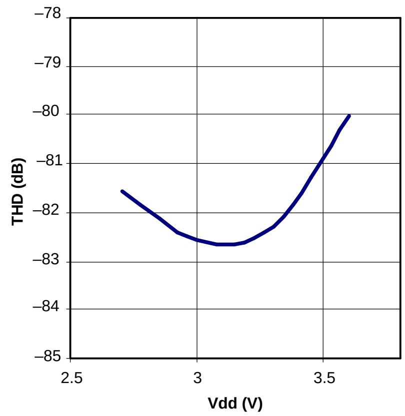


Figure 38.

SNR OF DAC (HP DRIVER)
vs
SUPPLY VOLTAGE

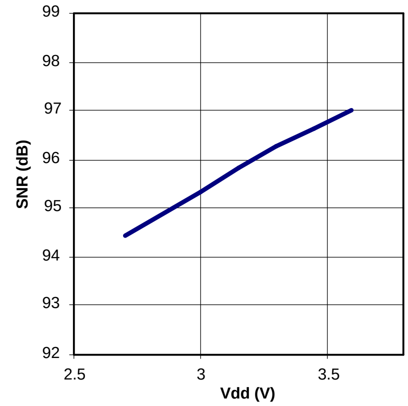


Figure 39.

THD OF BYPASS PATH
vs
SUPPLY VOLTAGE

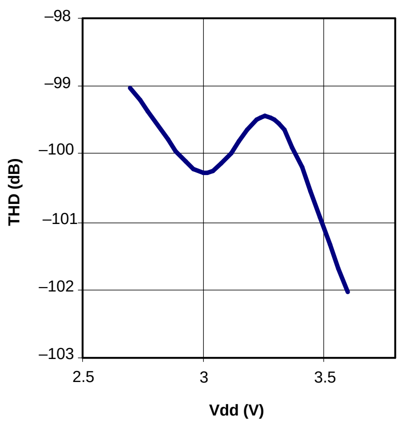


Figure 40.

SNR OF BYPASS PATH
vs
SUPPLY VOLTAGE

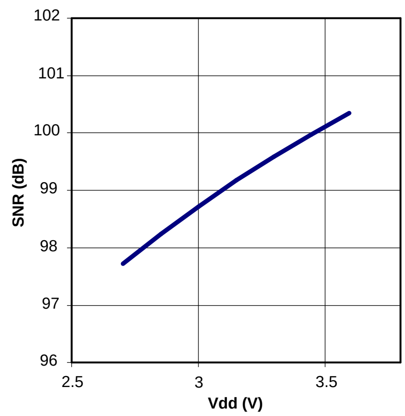


Figure 41.

THD OF MONO PATH
vs
SUPPLY VOLTAGE

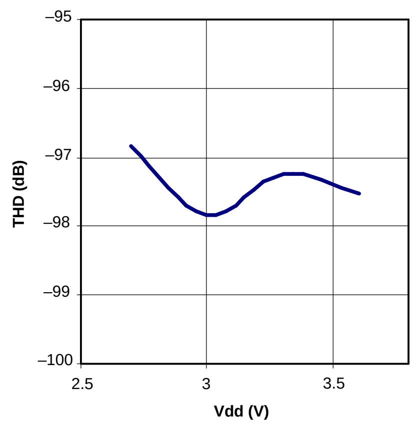


Figure 42.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, $+V_{DD}$ = +3.3 V, V_{REF} = +2.5 V, f_{SAMPLE} = 125 kHz, unless otherwise noted.

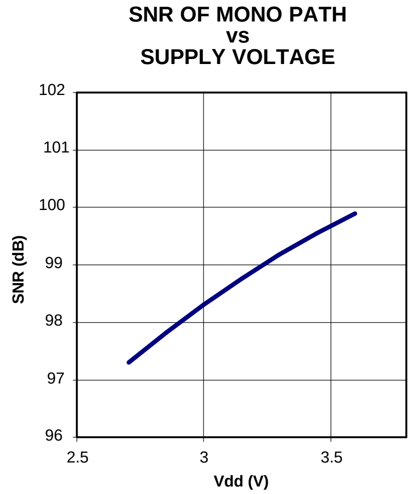


Figure 43.

OVERVIEW

The TSC2301 is an analog interface circuit for human interface devices. A register-based architecture eases integration with microprocessor-based systems through a standard SPI bus. All peripheral functions are controlled through the registers and onboard state machines.

The TSC2301 consists of the following blocks (refer to the block diagram on p. 2):

1. Touch screen interface
2. Keypad interface
3. Battery monitors
4. Auxiliary inputs
5. Temperature monitor
6. Current output digital-to-analog converter
7. Audio codec and signal processing

Communication to the TSC2301 is via a standard SPI serial interface. This interface requires that the slave select signal be driven low to communicate with the TSC2301. Data is then shifted into or out of the TSC2301 under control of the host microprocessor, which also provides the serial data clock.

Control of the TSC2301 and its functions is accomplished by writing to different registers in the TSC2301. A simple command protocol is used to address the 16-bit registers. Registers control the operation of the touch screen A/D converter, keypad scanner, and audio codec.

The result of measurements made are placed in the TSC2301 memory map and can be read by the host at any time. Three signals are available from the TSC2301 to indicate that data is available for the host to read. The $\overline{DAV}$ output indicates that an analog-to-digital conversion has completed and that data is available. The $\overline{KBIRQ}$ output indicates that an unmasked key on the keypad has been pressed and de-bounced. The $\overline{PENIRQ}$ output indicates that a touch has been detected on the touch screen.

A typical application of the TSC2301 is shown in Figure 44.

OVERVIEW (continued)

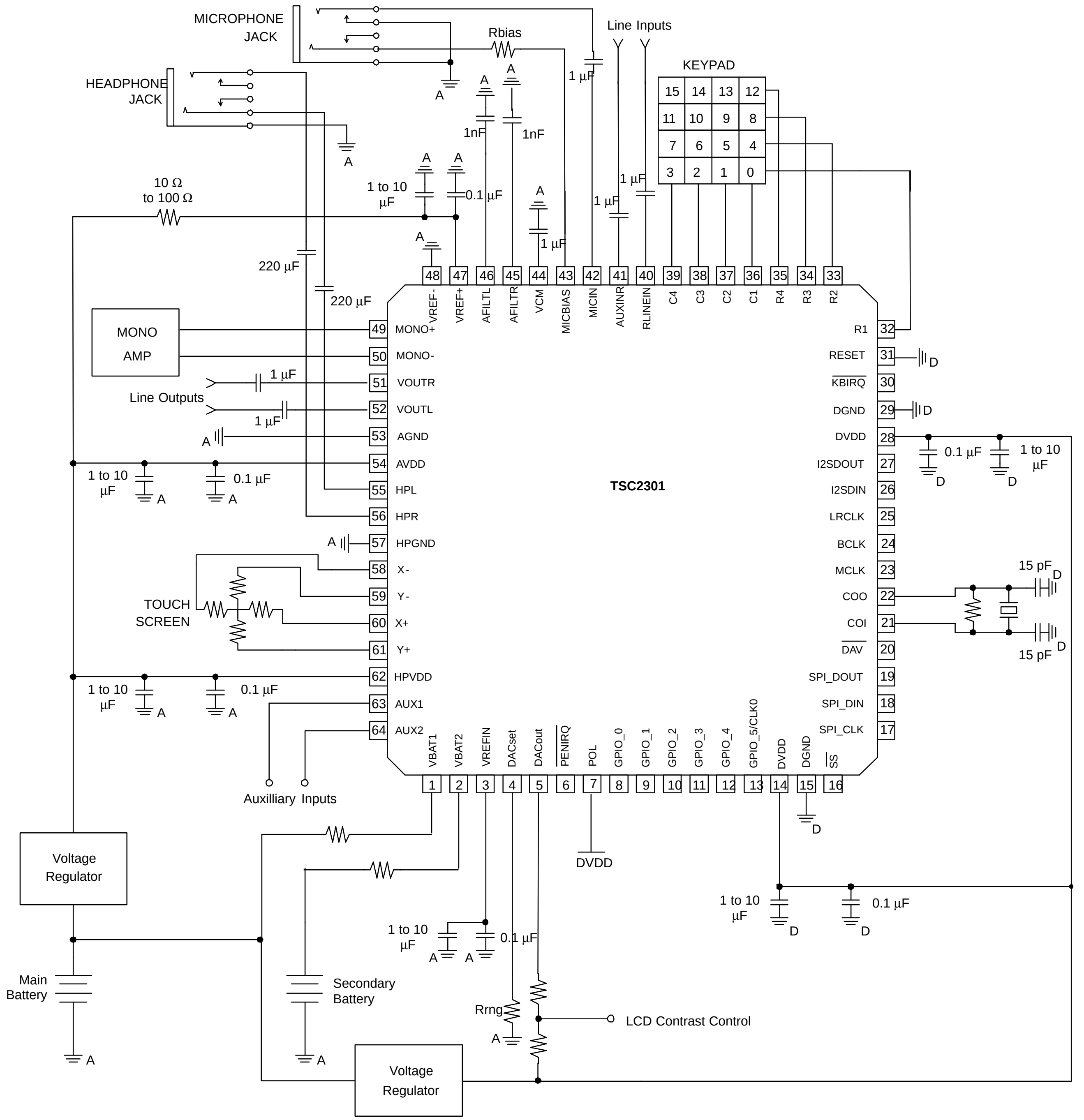


Figure 44. Typical Circuit Configuration

DETAILED DESCRIPTION

OPERATION - TOUCH SCREEN

A resistive touch screen works by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where a screen is touched by an input stylus, pen, or finger. The change in the resistance ratio marks the location on the touch screen.

DETAILED DESCRIPTION (continued)

The TSC2301 supports the resistive 4-wire configuration (see Figure 44). The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

The 4-Wire Touch Screen Coordinate Pair Measurement

A 4-wire touch screen is constructed as shown in Figure 45. It consists of two transparent resistive layers separated by insulating spacers.

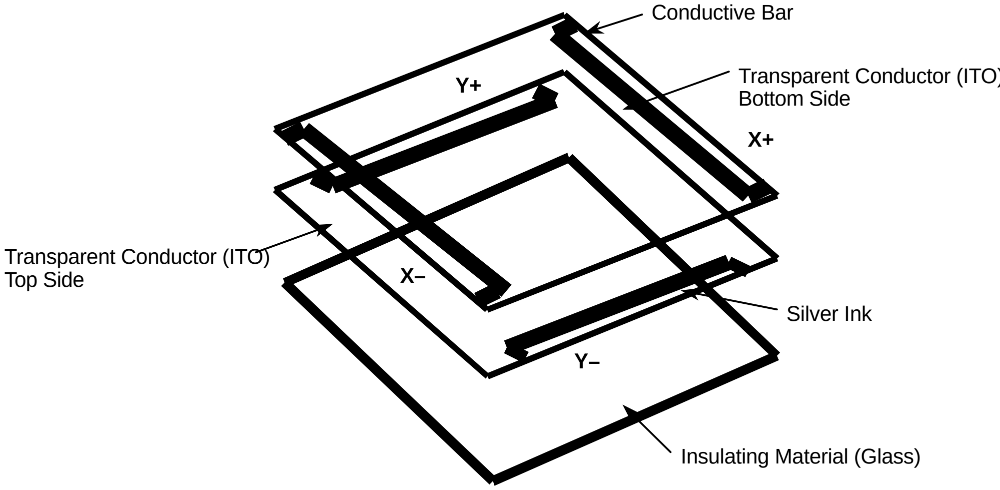


Figure 45. 4-Wire Touch Screen Construction

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The ADC converts the voltage measured at the point where the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to the ADC input, driving Y+ to +VDD and Y- to GND using switches internal to the TSC2301, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion, due to the high input impedance of the ADC.

Voltage is then applied to the other axis, and the ADC converts the voltage representing the X position on the screen. This provides the X and Y coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2301. To determine pen or finger touch, the pressure of the *touch* needs to be determined. Generally, it is not necessary to have very high performance for this test, therefore, the 8-bit resolution mode is recommended (however, calculations are shown with the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2301 supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-position, and two additional cross panel measurements (Z2 and Z1) of the touch screen (see Figure 46). Using Equation 1 calculates the touch resistance:

$$R_{TOUCH} = R_{X\text{–}plate}\,\frac{X\text{–}position}{4096}\left(\frac{Z_2}{Z_1} - 1\right) \tag{1}$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-position and Y-position, and Z_1. Using Equation 2 also calculates the touch resistance:

$$R_{TOUCH} = \left(\frac{R_{X\text{–plate}} \; X\text{–position}}{4096} \right) \left(\frac{4096}{Z_1} - 1 \right) - R_{Y\text{–plate}} \left(1 - \frac{Y\text{–position}}{4096} \right) \quad (2)$$

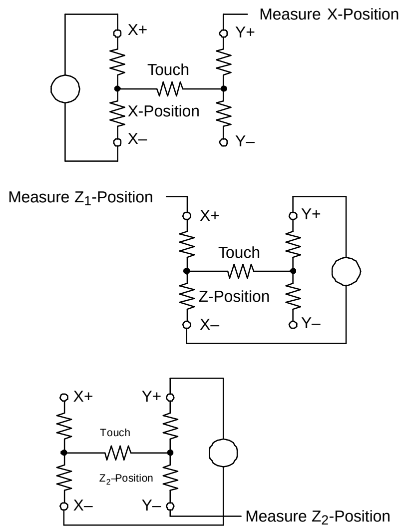


Figure 46. Pressure Measurement

When the touch panel is pressed or touched, and the drivers to the panel are turned on, the voltage across the touch panel often overshoots and then slowly settles (decay) down to a stable dc value. This is due to mechanical bouncing, which is caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value is in error. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen, i.e. noise generated by the LCD panel or back-light circuitry. The value of these capacitors provides a low-pass filter to reduce the noise, but causes an additional settling time requirement when the panel is touched.

Several solutions to this problem are available in the TSC2301. A programmable delay time is available which sets the delay between turning the drivers on and making a conversion. This is referred to as the panel voltage stabilization time, and is used in some of the modes available in the TSC2301. In other modes, the TSC2301 can be commanded to turn on the drivers only without performing a conversion. Time can then be allowed before the command is issued to perform a conversion.

The TSC2301 touch screen interface can measure position (X,Y) and pressure (Z). Determination of these coordinates is possible under three different modes of the A/D converter: conversion controlled by the TSC2301, initiated by detection of a touch; conversion controlled by the TSC2301, initiated by the host responding to the $\overline{\text{PENIRQ}}$ signal; or conversion completely controlled by the host processor.

A/D CONVERTER

The analog inputs of the TSC2301 are shown in Figure 47. The analog inputs (X, Y, and Z touch panel coordinates, battery voltage monitors, chip temperature, and auxiliary inputs) are provided via a multiplexer to the successive approximation register (SAR) analog-to-digital converter (ADC). The A/D architecture is based on capacitive redistribution architecture, which inherently includes a sample/hold function.

A unique configuration of low on-resistance switches allows an unselected ADC input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistances.

The ADC is controlled by an ADC control register. Several modes of operation are possible, depending upon the bits set in the control register. Channel selection, scan operation, averaging, resolution, and conversion rate may all be programmed through this register. These modes are outlined in the sections below for each type of analog input. The results of conversions made are stored in the appropriate result register.

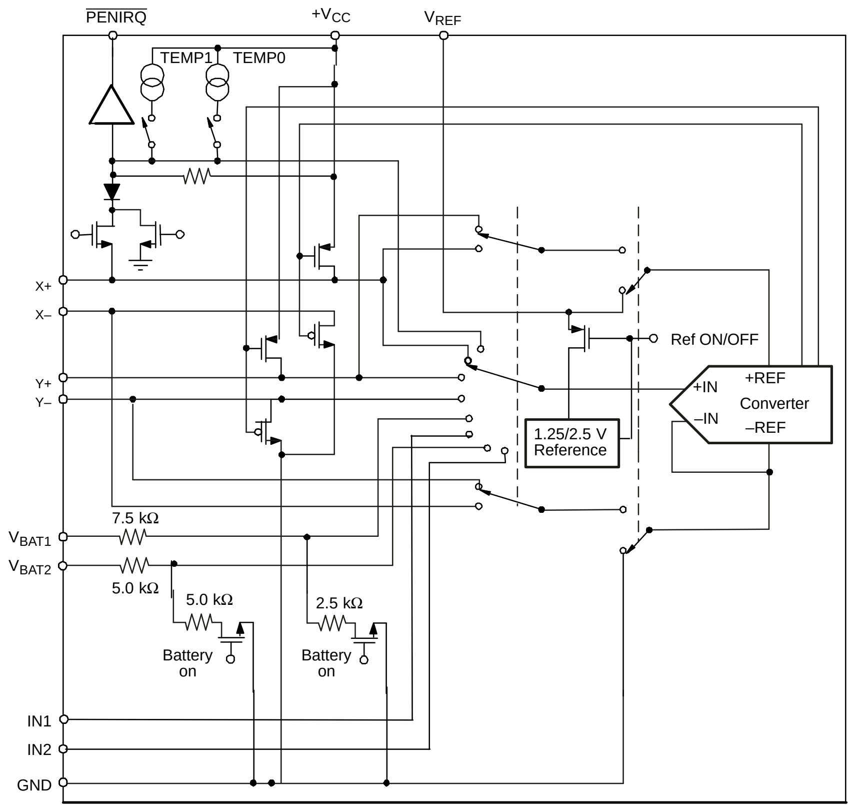


Figure 47. Simplified Diagram of the Touch Screen Analog Input Section

Data Format

The TSC2301 output data is in straight binary format as shown in Figure 48. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

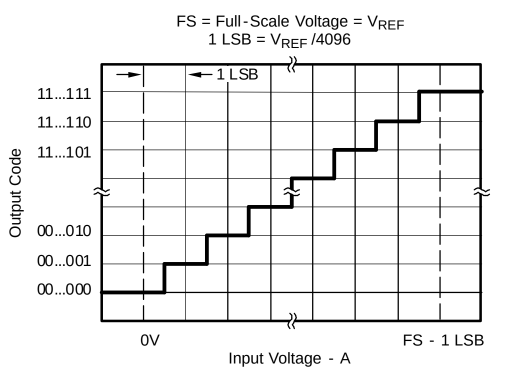


Figure 48. Ideal Input Voltages and Output Codes

Reference

The TSC2301 has an internal voltage reference that can be set to 1.2 V or 2.5 V, through the reference control register. This reference can also be set to automatically power down between conversions to save power, or remain on to reduce settling time.

The internal reference voltage is only used in the single-ended mode for battery monitoring, temperature measurement, and for utilizing the auxiliary inputs. Optimal touch screen performance is achieved when using a ratiometric conversion, thus all touch screen measurements are done automatically in the differential mode.

An external reference can also be applied to the VREFIN pin, and the internal reference can be turned off.

Variable Resolution

The TSC2301 provides three different resolutions for the ADC: 8, 10, or 12 bits. Lower resolutions are often practical for measurements such as touch pressure. Performing the conversions at lower resolution reduces the amount of time it takes for the ADC to complete its conversion process, which lowers power consumption.

Conversion Clock and Conversion Time

The TSC2301 contains an internal 8-MHz clock, which is used to drive the state machines inside the device that perform the many functions of the part. This clock is divided down to generate the actual ADC conversion clock. The division ratio for this clock is set in the ADC control register. The ability to change the conversion clock rate allows the user to choose the optimal value for resolution, speed, and power. If the 8-MHz clock is used directly, the ADC is limited to 8-bit resolution; using higher resolutions at this speed does not result in accurate conversions. Using a 4-MHz conversion clock is suitable for 10-bit resolution; 12-bit resolution requires that the conversion clock run at 1 or 2 MHz.

Regardless of the conversion clock speed, the internal clock runs nominally at 8 MHz. The conversion time of the TSC2301 is dependent upon several functions. While the conversion clock speed plays an important role in the time it takes for a conversion to complete, a certain number of internal clock cycles is needed for proper sampling of the signal. Moreover, additional times, such as the panel voltage stabilization time, can add significantly to the time it takes to perform a conversion. Conversion time can vary depending upon the mode in which the TSC2301 is used. Throughout this data sheet, internal and conversion clock cycles are used to describe the times that many functions take. In considering the total system design, these times must be taken into account by the user.

Touch Detect

The pen interrupt ($\overline{\text{PENIRQ}}$) output function is detailed in Figure 49. While in the touch screen monitoring mode, the Y- driver is ON and connected to GND, the X+ input is connected through a pullup resistor to V_{DD}, and the $\overline{\text{PENIRQ}}$ output reflects the state of the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen and $\overline{\text{PENIRQ}}$ output goes LOW due to the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycles for X- and Y-position, the X+ input is disconnected from $\overline{\text{PENIRQ}}$ to eliminate any leakage current from the pullup resistor that might flow through the touch screen, thus causing no errors.

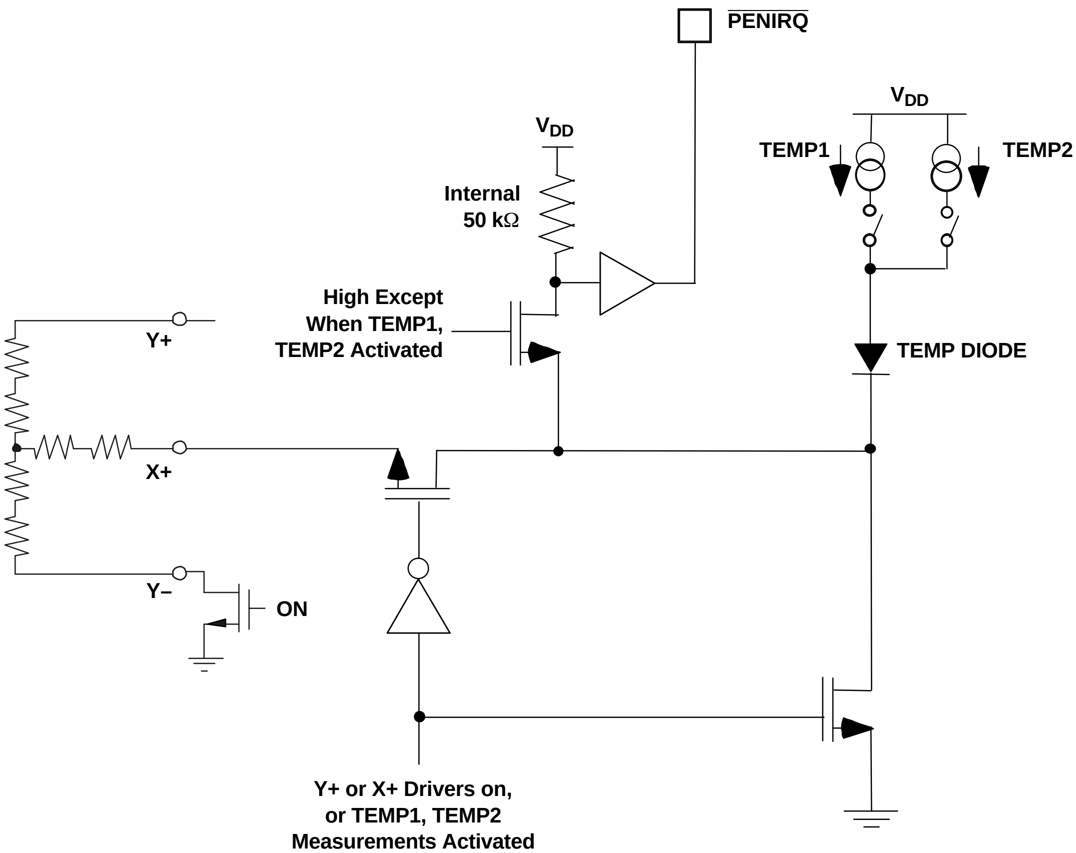


Figure 49. PENIRQ Functional Block Diagram

In modes where the TSC2301 needs to detect if the screen is still touched (for example, when doing a PENIRQ-initiated X, Y, and Z conversion), the TSC2301 must reconnect the drivers so that the 50-kΩ resistor is connected again. Because of the high value of this pullup resistor, any capacitance on the touch screen inputs cause a long delay time, and may prevent the detection from occurring correctly. To prevent this, the TSC2301 has a circuit which allows any screen capacitance to be *precharged* through a low-resistance connection to VDD, so that the pullup resistor doesn't have to be the only source for the charging current. The time allowed for this precharge, as well as the time needed to sense if the screen is still touched, can be set in the configuration control register. All other drivers (X-,Y+, Y-) are off during precharging.

This does point out, however, the need to use the minimum capacitor values possible on the touch screen inputs. These capacitors may be needed to reduce noise, but too large a value increases the needed precharge and sense times, as well as panel voltage stabilization time.

In self-controlled modes where the TSC2301 automatically performs conversions when it detects a pen touch, it is generally not necessary for the host processor to monitor PENIRQ. Instead, the host must monitor DAV, which goes low when data is available in the appropriate data register, and returns high when all new data has been read back by the host.

DIGITAL INTERFACE

The TSC2301 communicates through a standard SPI bus. The SPI allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master generates the synchronizing clock and initiates transmissions. The SPI slave devices depend on a master to start and synchronize transmissions.

A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock. As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

When the POL pin of the TSC2301 is tied high (POL=1), the idle state of the serial clock for the TSC2301 is low, which corresponds to a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). When the POL pin of the TSC2301 is tied low (POL=0), the idle state of the serial clock is high, which corresponds to a clock polarity setting of 1 (typical microprocessor SPI control bit CPOL = 1). The TSC2301 interface is designed so that with a clock phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI pin and the slave begins driving its MISO pin on the first serial clock edge. The $\overline{SS}$ pin can remain low between transmissions; however, the TSC2301 only interprets the first 16 bits transmitted after the falling edge of $\overline{SS}$ as a command word, and the next 16 bits as a data word only if writing to a register. Reserved register bits should be written to their default values (see Table 4).

TSC2301 Communication Protocol

The TSC2301 is entirely controlled by registers. Reading and writing these registers is accomplished by the use of a 16-bit command, which is sent prior to the data for that register. The command is constructed as shown in Table 2.

The command word begins with an R/W bit, which specifies the direction of data flow on the serial bus. The following 4 bits specify the page of memory this command is directed to, as shown in Table 1. The next six bits specify the register address on that page of memory to which the data is directed. The last five bits are reserved for future use.

Table 1. Page Addressing

PG3	PG2	PG1	PG0	Page Addressed
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	reserved
0	1	0	0	reserved
0	1	0	1	reserved
0	1	1	0	reserved
0	1	1	1	reserved
1	0	0	0	reserved
1	0	0	1	reserved
1	0	1	0	reserved
1	0	1	1	reserved
1	1	0	0	reserved
1	1	0	1	reserved
1	1	1	0	reserved
1	1	1	1	reserved

To read all the first page of memory, for example, the host processor must send the TSC2301 the command 0x8000 - this specifies a read operation beginning at page 0, address 0. The processor can then start clocking data out of the TSC2301. The TSC2301 automatically increments its address pointer to the end of the page; if the host processor continues clocking data out past the end of a page, the TSC2301 simply sends back the value 0xFFFF.

Continuous writing is generally not recommended for the control registers, but for the coefficients of bass-boost filter coefficient registers, continuous writing works. Writing to these registers consists of the processor writing the command 0x10E0, which specifies a write operation, with PG1 set to 1, and the ADDR bits set to 07h. This results in the address pointer pointing at the location of the first bass-boost coefficient in memory see Table 3 (Page 2). See the section on the TSC2301 memory map for details of register locations

Table 2. TSC2301 Command Word

Bit 15 M	SBBit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
R/W*	PG3	PG2	PG1	PG0	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	X	X	X	X	X

Figure 50 shows an example of a complete data transaction between the host processor and the TSC2301.

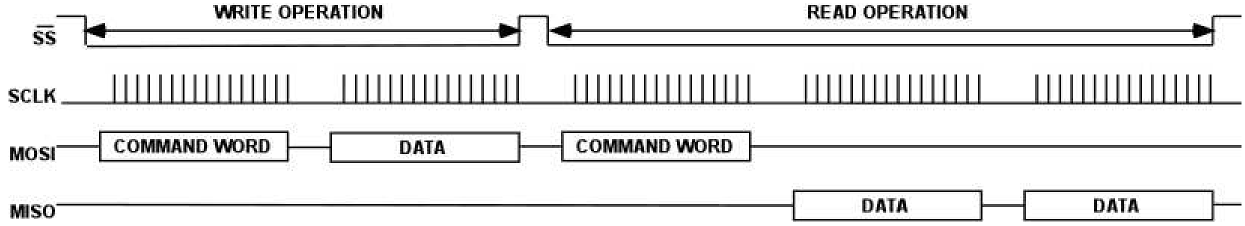


Figure 50. Write and Read Operation of TSC2301 Interface, POL = 1

TSC2301 MEMORY MAP

The TSC2301 has several 16-bit registers that allow control of the device as well as providing a location for results from the TSC2301 to be stored until read by the host microprocessor. These registers are separated into three pages of memory in the TSC2301: a data page (Page 0), a control page (Page 1), and an audio control page (Page 2). The memory map is shown in Table 3.

Table 3. TSC2301 Memory Map

Page 0: Data Registers			Page 1: Control Registers			Page 2: AudioControl Registers	
Addr	Register		Addr	Register		Addr	Register
00	X		00	ADC		00	Audio control
01	Y		01	KEY		01	ADC volume control
02	Z1		02	DACCTL		02	DAC volume control
03	Z2		03	REF		03	Analog audio bypass volume control
04	KPData		04	RESET		04	Keyclick control
05	BAT1		05	CONFIG		05	Audio power/ crystal oscillator control
06	BAT2		06	CONFIG2		06	GPIO control
07	AUX1		07	reserved		07	DAC bass-boost filter coefficients
08	AUX2		08	reserved		08	DAC bass-boost filter coefficients
09	TEMP1		09	reserved		09	DAC bass-boost filter coefficients
0A	TEMP2		0A	reserved		0A	DAC bass-boost filter coefficients
0B	DAC		0B	reserved		0B	DAC bass-boost filter coefficients
0C	reserved		0C	reserved		0C	DAC bass-boost filter coefficients
0D	reserved		0D	reserved		0D	DAC bass-boost filter coefficients
0E	reserved		0E	reserved		0E	DAC bass-boost filter coefficients
0F	reserved		0F	reserved		0F	DAC bass-boost filter coefficients
10	reserved		10	KPMask		10	DAC bass-boost filter coefficients
11	reserved		11	reserved		11	DAC bass-boost filter coefficients
12	reserved		12	reserved		12	DAC bass-boost filter coefficients
13	reserved		13	reserved		13	DAC bass-boost filter coefficients
14	reserved		14	reserved		14	DAC bass-boost filter coefficients
15	reserved		15	reserved		15	DAC bass-boost filter coefficients
16	reserved		16	reserved		16	DAC bass-boost filter coefficients
17	reserved		17	reserved		17	DAC bass-boost filter coefficients
18	reserved		18	reserved		18	DAC bass-boost filter coefficients
19	reserved		19	reserved		19	DAC bass-boost filter coefficients
1A	reserved		1A	reserved		1A	DAC bass-boost filter coefficients
1B	reserved		1B	reserved		1B	reserved
1C	reserved		1C	reserved		1C	reserved
1D	reserved		1D	reserved		1D	reserved
1E	reserved		1E	reserved		1E	reserved
1F	reserved		1F	reserved		1F	reserved

TSC2301 REGISTER OVERVIEW

Table 4. Register Summary for TSC2301

PAGE	ADDR (HEX)	REGISTER NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	RESET VALUE (HEX)
0	00	X	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	01	Y	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	02	Z1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	03	Z2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	04	KPDATA	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0	0000
0	05	BAT1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	06	BAT2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	07	AUX1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	08	AUX2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	09	TEMP1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	0A	TEMP2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	0B	DAC	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0080
0	0C	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	0D	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	0E	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	0F	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	10	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	11	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	12	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	13	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	14	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	15	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	16	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	17	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	18	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	19	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1A	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1B	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1C	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1D	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1E	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1F	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	00	ADC	PSM	STS	AD3	AD2	AD1	AD0	RS1	RS0	AV1	AV0	CL1	CL0	PV2	PV1	PV0	0	4000
1	01	KEY	STC	SCS	DB2	DB1	DB0	0	0	0	0	0	0	0	0	0	0	0	4000
1	02	DACCTL	DPD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000
1	03	REF	0	0	0	0	0	0	0	0	0	0	0	INT	DL1	DL0	PDN	RFV	0002
1	04	RESET	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	FFFF
1	05	CONFIG	1	1	1	1	1	1	1	1	1	1	PR2	PR1	PR0	SN2	SN1	SN0	FFC0
1	06	CONFIG2	SDA/V/KBC1	KBC0	PLLO	PCTE	PDC3	PDC2	PDC1	PDC0	A3	A2	A1	A0	N3	N2	N1	N0	FFFF
1	07	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	08	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	09	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0A	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0B	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0C	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0D	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0E	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF

Table 4. Register Summary for TSC2301 (continued)

PAGE	ADDR (HEX)	REGISTER NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	RESET VALUE (HEX)
1	0F	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	10	KPMASK	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	0000
1	11	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	12	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	13	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	14	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	15	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	16	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	17	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	18	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	19	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1A	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1B	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1C	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1D	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1E	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1F	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
2	00	AUDCNTL	HPF 1	HPF 0	INML 1	INML 0	INM R1	INM R0	MIC G1	MIC G0	MCL K1	MCL K0	I2SF S3	I2SF S2	I2SF S1	I2SF S0	I2SF M1	I2SF M0	C003
2	01	ADCVOL	ADM UL	ADV L6	ADV L5	ADV L4	ADV L3	ADV L2	ADV L1	ADV L0	ADM UR	ADV R6	ADV R5	ADV R4	ADV R3	ADV R2	ADV R1	ADV R0	D7D7
2	02	DACVOL	DAM UL	DAV L6	DAV L5	DAV L4	DAV L3	DAV L2	DAV L1	DAV L0	DAM UR	DAV R6	DAV R5	DAV R4	DAV R3	DAV R2	DAV R1	DAV R0	FFFF
2	03	BPVOL	BPM UL	BPV L6	BPV L5	BPV L4	BPV L3	BPV L2	BPV L1	BPV L0	BPM UR	BPV R6	BPV R5	BPV R4	BPV R3	BPV R2	BPV R1	BPV R0	E7E7
2	04	KEYCLICK	KEY ST	KCA M2	KCA M1	KCA M0	0	KCF R2	KCF R1	KCF R0	KCL N3	KCL N2	KCL N1	KCL N0	0	MON S	SSR TE	SST EP	4411
2	05	PD/MISC	APD	AVP D	ABP D	HAP D	MOP D	DAP D	ADP DL	ADP DR	PDS TS	MIBP D	OSC C	BCK C	SMP D	OTS YN	BAS S	DEE MP	FFC4
2	06	GPIO	0	0	IO5	IO4	IO3	IO2	IO1	IO0	0	0	GPI O5	GPI O4	GPI O3	GPI O2	GPI O1	GPI O0	0000
2	07	BBCFN0L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	6BE2
2	08	BBCFN1L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	9667
2	09	BBCFN2L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	675D
2	0A	BBCFN3L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	6BE2
2	0B	BBCFN4L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	9667
2	0C	BBCFN5L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	675D
2	0D	BBCFD1L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	7D82
2	0E	BBCFD2L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	84EF
2	0F	BBCFD4L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	7D82
2	10	BBCFD5L	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	84EF
2	11	BBCFN0R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	6BE2
2	12	BBCFN1R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	9667
2	13	BBCFN2R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	675D
2	14	BBCFN3R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	6BE2
2	15	BBCFN4R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	9667
2	16	BBCFN5R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	675D
2	17	BBCFD1R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	7D82
2	18	BBCFD2R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	84EF
2	19	BBCFD4R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	7D82
2	1A	BBCFD5R	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	84EF

Table 4. Register Summary for TSC2301 (continued)

PAGE	ADDR (HEX)	REGISTER NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	RESET VALUE (HEX)
2	1B	ADCLKCFG	0	0	0	0	0	1	0	0	0	0	0	0	PLPN	COMK	0	0	0400
2	1C	reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
2	1D	reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
2	1E	reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
2	1F	reserved	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000

TSC2301 TOUCH SCREEN CONTROL REGISTERS

This section describes each of the registers shown in the memory map of Figure 54. The registers are grouped according to the function they control. In the TSC2301, bits in control registers can refer to slightly different functions depending upon whether you are reading the register or writing to it. A summary of all registers and bit locations is shown in Table 4.

TSC2301 ADC Control Register (Page 1, Address 00H)

The ADC in the TSC2301 is shared between all the different functions. A control register determines which input is selected, as well as other options. The result of the conversion is placed in one of the result registers in Page 0 of memory, depending upon the function selected.

The ADC control register controls several aspects of the ADC. The register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
PSM	STS	AD3	AD2	AD1	AD0	RS1	RS0	AV1	AV0	CL1	CL0	PV2	PV1	PV0	X

Bit 15 — PSM

Pen Status/Control Mode. Reading this bit allows the host to determine if the screen is touched. Writing to this bit determines the mode used to read coordinates: host controlled or under control of the TSC2301 responding to a screen touch. When reading, the PENSTS bit indicates if the pen is down or not. When writing to this register, this bit determines if the TSC2301 controls the reading of coordinates, or if the coordinate conversions are host-controlled. The default state is host-controlled conversions (0).

Table 5. PSM Bit Operation

PSM		
Read/Write	**Value**	**Description**
Read	0	No screen touch detected (default)
Read	1	Screen touch detected
Write	0	Conversions controlled by host
Write	1	Conversions controlled by TSC2301

Bit 14 — STS

ADC Status. Reading this bit indicates if the converter is busy. Writing a 0 to this bit causes the touch screen scans to continue until either the pen is lifted or the process is stopped. Continuous scans or conversions can be stopped by writing a 1 to this bit. This immediately halts a conversion (even if the pen is still down) and causes the ADC to power down. The default state is continuous conversions, but if this bit is read after a reset or power-up, it reads 1.

Table 6. STS Bit Operation

STS		
Read/Write	**Value**	**Description**
Read	0	Converter is busy
Read	1	Converter is not busy (default)
Write	0	Normal operation
Write	1	Stop conversion and power down

Bits [13:10] — AD3 - AD0

ADC Function Select bits. These bits control which input is to be converted, and what mode the converter is placed in. These bits are the same whether reading or writing. See Table 7 for a complete listing of how these bits are used.

Table 7. ADC Function Select

A/D3	A/D2	A/D1	A/D0	Function
0	0	0	0	Invalid. No registers are updated. This is the default state after a reset.
0	0	0	1	Touch screen scan function: X and Y coordinates converted and the results returned to X and Y data registers. Scan continues until either the pen is lifted or a stop bit is sent.
0	0	1	0	Touch screen scan function: X, Y, Z1 and Z2 coordinates converted and the results returned to X, Y, Z1 and Z2 data registers. Scan continues until either the pen is lifted or a stop bit is sent.
0	0	1	1	Touch screen scan function: X coordinate converted and the results returned to X data register.
0	1	0	0	Touch screen scan function: Y coordinate converted and the results returned to Y data register.
0	1	0	1	Touch screen scan function: Z1 and Z2 coordinates converted and the results returned to Z1 and Z2 data registers.
0	1	1	0	Battery input 1 converted and the results returned to the BAT1 data register.
0	1	1	1	Battery input 2 converted and the results returned to the BAT2 data register.
1	0	0	0	Auxiliary input 1 converted and the results returned to the AUX1 data register.
1	0	0	1	Auxiliary input 2 converted and the results returned to the AUX2 data register.
1	0	1	0	A temperature measurement is made and the results returned to the temperature measurement 1 data register.
1	0	1	1	Port scan function: Battery input 1, Battery input 2, Auxiliary input 1, and Auxiliary input 2 measurements are made and the results returned to the appropriate data registers
1	1	0	0	A differential temperature measurement is made and the results returned to the temperature measurement 2 data register.
1	1	0	1	Turn on X+, X- drivers
1	1	1	0	Turn on Y+, Y- drivers
1	1	1	1	Turn on Y+, X- drivers

Bits[9:8] — RS1, RS0

Resolution Control. The ADC resolution is specified with these bits. SeeTable 8 for a description of these bits. These bits are the same whether reading or writing.

Table 8. ADC Resolution Control

RS1	RS0	Function
0	0	12-bit resolution. Power up and reset default.
0	1	8-bit resolution
1	0	10-bit resolution
1	1	12-bit resolution

Bits[7:6] — AV1, AV0

Converter Averaging Control. These two bits (see Table 9) allow you to specify the number of averages the converter performs. Note that when averaging is used, the STS/STP bit and the DAV output indicates that the converter is busy until all conversions necessary for the averaging are complete. The default state for these bits is 00, selecting no averaging. These bits are the same whether reading or writing.

Table 9. ADC Conversion Averaging Control

AV1	AV0	Function
0	0	None (one conversion) (default)
0	1	4 data averages
1	0	8 data averages
1	1	16 data averages

Bits[5:4] — CL1, CL0

Conversion Clock Control. These two bits specify the internal clock rate which the ADC uses when performing a conversion. See Table 10. These bits are the same whether reading or writing.

Table 10. ADC Conversion Clock Control

CL1	CL0	Function
0	0	8-MHz internal clock rate - 8-bit resolution only (default)
0	1	4-MHz internal clock rate - 8- or 10-bit resolution only
1	0	2-MHz internal clock rate
1	1	1-MHz internal clock rate

Bits [3:1] — PV2 - PV0

Panel Voltage Stabilization Time Control. These bits allow the user to specify a delay time from when a driver is turned on to the time sampling begins and a conversion is started. In self-controlled mode, when a pen touch is detected, the part first turns on a driver, waits a programmed delay time set by PV2-PV0, and then begins sampling and A/D conversion. See Table 11 for settings of these bits. The default state is 000, indicating a 0µs stabilization time. These bits are the same whether reading or writing.

Table 11. Panel Voltage Stabilization Time Control

PV2	PV1	PV0	Stabilization Time
0	0	0	0 µs (default)
0	0	1	100 µs
0	1	0	500 µs
0	1	1	1 ms
1	0	0	5 ms
1	0	1	10 ms
1	1	0	50 ms
1	1	1	100 ms

Bit 0

This bit is reserved. When read, it always reads as a zero.

DAC Control Register (Page 1, Address 02H)

The single bit in this register controls the power down control of the onboard digital-to-analog converter (DAC). This register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
DPD	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit 15 — DPD

DAC Power Down. This bit controls whether the DAC is powered up and operational, or powered down. If the DAC is powered down, the AOUT pin neither sinks nor sources current.

Table 12. DPD Bit Operation

DPD	
Value	**Description**
0	DAC is powered and operational
1	DAC is powered down. (default)

Reference Register (Page 1, Address 03H)

This register controls whether the TSC2301 uses an internal or external reference, and if the internal reference is used, the value of the reference voltage, whether it powers down between conversions and the programmable settling time after reference power-up. This register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	X	X	X	X	X	X	X	X	X	X	INT	DL1	DL0	PDN	RFV

Bit 4 —INT

Internal Reference Mode. If this bit is written to a 1, the TSC2301 uses its internal reference; if this bit is a 0, the part assumes an external reference is being supplied. The default state for this bit is to select an external reference (0). This bit is the same whether reading or writing.

Table 13. INT Bit Operation

INT	
Value	**Description**
0	External reference selected (default)
1	Internal reference selected

Bits [3:2] — DL1, DL0

Reference Power-Up Delay. When the internal reference is powered up, a finite amount of time is required for the reference to settle. If measurements are made before the reference has settled, these measurements are in error. These bits allow for a delay time for measurements to be made after the reference powers up, thereby assuring that the reference has settled. Longer delays are necessary depending upon the capacitance present at the VREFIN pin (see Typical Curves). The delays are shown in Table 14. The default state for these bits is 00, selecting a 0 microsecond delay. These bits are the same whether reading or writing.

Table 14. Reference Power-Up Delay Settings.

DL1	DL0	DELAY TIME
0	0	0us (default)
0	1	100 µs
1	0	500 µs
1	1	1000 µs

Bit 1 —PDN

Reference Power Down. If a 1 is written to this bit, the internal reference are powered down between conversions. If this bit is a zero, the internal reference is powered at all times. The default state is to power down the internal reference, so this bit will be a 1. This bit is the same whether reading or writing.

Table 15. PDN Bit Operation

PDN	
Value	**Description**
0	Internal reference is powered at all times
1	Internal reference is powered down between conversions. (default)

Note that the PDN bit, in concert with the INT bit, creates a few possibilities for reference behavior. These are detailed in Table 16.

Table 16. Reference Behavior Possibilities

INT	PDN	Reference Behavior
0	0	External reference used, internal reference powered down.
0	1	External reference used, internal reference powered down.
1	0	Internal reference used, always powered up
1	1	Internal reference used, powers up during conversions and then powers down.

Bit 0 — RFV

Reference Voltage Control. This bit selects the internal reference voltage, either 1.2 V or 2.5 V. The default value is 1.2 V. This bit is the same whether reading or writing.

Table 17. RFV Bit Operation

RFV	
Value	**Description**
0	1.2-V reference voltage (default)
1	2.5-V reference voltage

TSC2301 Configuration Control Register (Page 1, Address 05H)

This control register controls the configuration of the precharge and sense times for the touch detect circuit. The register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	PRE2	PRE1	PRE0	SNS2	SNS1	SNS0

Bits [5:3] — PRE[2:0]

Precharge time selection bits. These bits set the amount of time allowed for precharging any pin capacitance on the touch screen prior to sensing if the screen is being touched.

Table 18. Precharge Times

PRE[2:0]			
PRE2	**PRE1**	**PRE0**	**Time**
0	0	0	20 µs (default)
0	0	1	84 µs
0	1	0	276 µs
0	1	1	340 µs
1	0	0	1.044 ms
1	0	1	1.108 ms
1	1	0	1.300 ms
1	1	1	1.364 ms

Bits [2:0] — SNS[2:0]

Sense time selection bits. These bits set the amount of time the TSC2301 waits to sense a screen touch between coordinate axis conversions in self-controlled mode.

Table 19. Sense Times

SNS[2:0]			
SNS2	**SNS1**	**SNS0**	**Time**
0	0	0	32 µs (default)
0	0	1	96 µs
0	1	0	544 µs
0	1	1	608 µs
1	0	0	2.080 ms
1	0	1	2.144 ms
1	1	0	2.592 ms
1	1	1	2.656 ms

TSC2301 KEYPAD REGISTERS

The keypad scanner hardware in the TSC2301 is controlled by two registers: the keypad control register and the keypad mask register. The keypad control register controls general keypad functions such as scanning and de-bouncing, while the keypad mask register allows you to mask certain keys from being detected at all.

Keypad Control Register (Page 1, Address 01H)

The Keypad Control register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
STC	SCS	DB2	DB1	DB0	X	X	X	X	X	X	X	X	X	X	X

Bit 15 — STC

Keypad Status. This bit reflects the operation of the $\overline{\text{KBIRQ}}$ pin, with inverted logic. This bit goes high when a key is pressed and debounced. The default value for this bit is 0.

Table 20. STC Bit Operation

STC	
Value	**Description**
0	No keys are pressed (default)
1	Key pressed and debounced

Bit 14 — SCS

Keypad Scan Status. When reading, this bit indicates if the scanner or de-bouncer is busy. Writing a 0 to this bit causes keypad scans to continue until either the key is lifted or the process is stopped. Continuous scans can be stopped by writing a 1 to this bit. This immediately halts a conversion (even if a key is still down). The default value for this bit when read is 1.

Table 21. SCS Bit Operation

SCS		
Read/Write	**Value**	**Description**
Read	0	Scanner or de-bouncer busy
Read	1	Scanner not busy (default)
Write	0	Normal operation
Write	1	Stop scans

Bits [13:11] — KBDB2-KBDB0

Keypad De-bounce Control. These bits set the length of the de-bounce time for the keypad, as shown in Table 22. The default setting is a 2-ms de-bounce time (000).

Table 22. Keypad De-Bounce Control

KBDB2	KBDB1	KBDB0	Function
0	0	0	De-bounce: 2 ms (default)
0	0	1	De-bounce: 10 ms
0	1	0	De-bounce: 20 ms
0	1	1	De-bounce: 50 ms
1	0	0	De-bounce: 60 ms
1	0	1	De-bounce: 80 ms
1	1	0	De-bounce: 100 ms
1	1	1	De-bounce: 120 ms

Keypad Mask Register (Page 1, Address 10H)

The Keypad Mask register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

This is the same format as used in the keypad data register (Page 0, Address 04H). Each bit in these registers represents one key on the keypad. In the mask register, if a bit is set (1), then that key is not detected in keypad scans. Pressing that key on the keypad also does not cause a $\overline{\text{KBIRQ}}$, if the bit is set. If the bit is cleared (0), the corresponding key is detected when pressed. A 16-key keypad is mapped into the keypad mask (and keypad data) register as shown in Table 23. The default value for this register is 0000H, detecting all key presses.

Table 23. Keypad to Key Bit Mapping

	C1	C2	C3	C4
R1	K0	K1	K2	K3
R2	K4	K5	K6	K7
R3	K8	K9	K10	K11
R4	K12	K13	K14	K15

The result of a keypad scan appears in the keypad data register. Each bit is set in this register, corresponding to the key(s) actually pressed. For example, if only key 1 was pressed on a particular scan, the data in the register would read as 0x0002; however, if keys 6, 8, and 13 were all pressed simultaneously on that scan, the data would read as 0x2140.

Multiple keys can be pressed simultaneously and are generally decoded correctly by the keypad scan circuitry. However, keys that land on three corners of a rectangle can cause a false reading of a key on the fourth corner of the rectangle. For example, if keys 0, 3, and 11 were pressed simultaneously, the KEY0, KEY3, and KEY11 bits are set, but the KEY8 bit is also set. Thus, when considering using multiple-key combinations in an application, try to avoid combinations that put three keys on the corners of a rectangle.

Secondary Configuration Register (Page 1, Address 06H):

This register allows the user to read the status of the $\overline{\text{DAV}}$ pin through the SPI interface. It controls the behavior of the $\overline{\text{KBIRQ}}$ signal, as well as provides control of the audio codec PLL.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
SDAV/KBC1	KBC0	PLLO	PCTE	PDC3	PDC2	PDC1	PDC0	A3	A2	A1	A0	N3	N2	N1	N0

Bit 15 — SDAV (write only)

SPI Data Available. This read-only bit mirrors the function of the DAV pin. This bit is provided so that the host processor can poll the SPI interface to see whether data is available, without dedicating a GPIO pin from the host processor to the TSC2301 DAV pin. This bit is normally high, goes low when touch screen or keypad data is available, and is reset high when all the new data has been read. When written to, this bit becomes KBC1, operation detailed below.

Table 24. SPI Data Available (Read Only)

SDAV	Description
0	Touchscreen data is available.
1	No new data available (default)

Bits [15:14] — KBC1-KBC0 (write mode)

KBIRQ Control (write-only mode). These bits control the behavior of the KBIRQ signal. There are four possible ways to de-assert the KBIRQ signal once it goes low. These bits control which particular events cause the KBIRQ signal to be de-asserted (go high). The four de-assertion possibilities are:

A. Hardware or software reset. Hardware reset—RESET pin asserted (high) and subsequently de-asserted. Software reset—writing BB00h to register 04h, page 1.

B. Writing 1 to the SCS bit. Bit 14 of register 01h, page 1

C. Releasing the pressed key on the keypad.

D. Reading the keypad data register (register 04h, page0).

Refer to the table below to see which settings of the KBC1 - KBC0 correspond to the KBIRQ reset events. When read, KBC1 becomes SDAV operation detailed above. KBC0 operates the same as in read and write modes.

Table 25. KBIRQ Behavior Possibilities

KBC1	KBC0	KBIRQ Reset Event
0	0	De-assertion possibility A or B or C.
0	1	De-assertion possibility A or B.
1	0	De-assertion possibility A or B or C or D.
1	1	De-assertion possibility A or B or D (default).

Bit 13 — PLLO

PLL Output on GPIO_0. This bit allows the user to receive the output of the audio codec internal PLL. This bit is provided so the host processor can use the output of the PLL, to generate its I^2S signals in sync with an external MCLK or crystal oscillator. Writing a 0 to this bit connects the output of the PLL to the GPIO_0 pin. Otherwise, the GPIO_0 pin operates as normal.

Table 26. PLL Output

PLLO	Description
0	Output PLL on GPIO_0.
1	GPIO_0 operates as normal (default).

Bit 12 — PCTE

PLL Control Enable. This bit allows the user to manually control the audio codec internal PLL. This allows the user to modify the contents of bits [11-0] to control the audio codec PLL. Writing a 0 to this bit enables manual control of the PLL. Otherwise, the PLL is set automatically based on the settings of MCLK [1:0] and I2SFS[3:0] in the audio control register (bits 7-2 in register 00h, page 2).

Table 27. PLL Control Enable

PLLO	Description
0	Allows modification of bits [11:0].
1	PLL operates as normal, no manual override (default).

Bit [11:8] — PDC3 - PDC0

PLL Predivider Control. This bit controls the predivider to the internal PLL. These bits represent a 4-bit straight binary number corresponding to the variable P in the PLL control equation discussed later in this section. The legal range of these bits is 1h to Fh. The default of these bits is Fh.

Bit [7:4] — A3 - A0

A Control. This bit represent a 4-bit straight binary number corresponding to the variable A in the PLL control equation discussed later in this section. The legal range of these bits is 0h to Fh. The default of these bits is Fh.

Bit [3:0] — N3 - N0

N Control. This bit represents a 4-bit straight binary number corresponding to the variable N in the PLL control equation discussed later in this section. The legal range of these bits is 0h to Fh. The default of these bits is Fh.

When using a nonaudio standard MCLK frequency or crystal that is not covered by any of the automatic PLL settings in MCLK[1:0], the user must manually configure the TSC2301 PLL to generate the proper clock for the audio data converters. The proper clock for any sampling rates that are submultiples of 44.1 kHz is 512 x 44.1 kHz = 22.5792 MHz. This frequency is valid for 44.1 kHz, 22.05 kHz, and 11.025 kHz. The proper clock for any sampling rates that are submultiples of 48 kHz is 512 x 48 kHz = 24.576 MHz. This frequency is valid for 48 kHz, 32 kHz, 24 kHz, 16 kHz, 12 kHz, and 8 kHz. Equation 3 is used to obtain the proper frequency. Since variables *P, N*, and *A* are integers, the exact proper clock frequencies can not always be obtained. However, examples are provided for common MCLK/crystal frequencies that minimize the error of the PLL output. One constraint is the *N* must always be greater than or equal to *A*. Another constraint is that the output of the MCLK predivider (the MCLK/P term) should be greater than 1 MHz. *P* can be any integer from 1 to 15, inclusive. *N* and *A* can be any integer from 0 to 15, inclusive. In some situations, settings outside of these constraints may work, but should be verified by the user beforehand. Table 28 shows some settings that have been tested and confirmed to work by TI.

$$F_{OUT} = \frac{MCLK}{P} \times \frac{(4N + A)}{3}, (N \geq A), \left(\frac{MCLK}{P} > 1MHz\right) \tag{3}$$

Table 28. PLL Settings

MCLK (MHz)	Desired F_{out}(MHz)	P	A	N	Actual F_{out}(MHz)	% Error
12	24.576	7	7	9	24.57143	-0.019
13	24.576	9	7	11	24.55556	-0.083
16	24.576	13	12	12	24.61538	0.160
19.2	24.576	13	10	10	24.61538	0.160
19.68	24.576	12	9	9	24.60000	0.097
3.6869	22.5792	3	7	12	22.53106	-0.213
12	22.5792	11	10	13	22.54545	-0.149
13	22.5792	14	13	15	22.59524	0.071
16	22.5792	13	11	11	22.56410	-0.067
19.2	22.5792	15	9	11	22.61333	0.151

Table 28. PLL Settings (continued)

MCLK (MHz)	Desired F_{out}(MHz)	P	A	N	Actual F_{out}(MHz)	% Error
19.68	22.5792	9	3	7	22.59556	0.072

TSC2301 DATA REGISTERS

The data registers of the TSC2301 hold data results from conversions or keypad scans, or the value of the DAC output current. All of these registers default to 0000H upon reset, except the DAC register, which is set to 0080H, representing the midscale output of the DAC.

X, Y, Z1, Z2, BAT1, BAT2, AUX1, AUX2, TEMP1, and TEMP2 REGISTERS

The results of all A/D conversions are placed in the appropriate data register, as described in Table 5 and Table 3. The data format of the result word, R, of these registers is right-justified, as follows (assuming a 12-bit conversion):

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
0	0	0	0	R11 MSB	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0 LSB

Keypad Data Register (Page 0, Address 04H)

The keypad data register (Page 0, Address 04H) is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0

This is the same format as used in the keypad mask register (Page 1, Address 10H). Each bit in these registers represents one key on the keypad. A 16-key keypad is mapped into the keypad data register as shown in Table 23.

DAC Data Register (Page 0, Address 0BH)

The data to be written to the DAC is written into the DAC data register, which is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
RES	RES	RES	RES	RES	RES	RES	RES	D7	D6	D5	D4	D3	D2	D1	D0

There are three different touch screen conversion modes available in the TSC2301: self-controlled or $\overline{PENIRQ}$-Initiated, host-initiated, and host-controlled. These three modes are described below.

OPERATION - TOUCH SCREEN MEASUREMENTS

Conversion Controlled by TSC2301 Initiated at Touch Detect

In this mode, the TSC2301 detects when the touch panel is touched and causes the $\overline{PENIRQ}$ line to go low. At the same time, the TSC2301 powers up its internal clock. It then turns on the Y-drivers, and after a programmed panel voltage stabilization time, powers up the ADC and convert the Y coordinate. If averaging is selected, several conversions may take place; when data averaging is complete, the Y coordinate result is stored in the Y register.

> This mode is recommended to fully utilize the integrated touch screen processing of the TSC2301 and reduce the processing overhead and number of interrupts to the host processor. In this mode, the host processor does not need to monitor $\overline{PENIRQ}$, instead the host needs only to configure the TSC2301 once at power-up, and then monitor $\overline{DAV}$ and read back data after a falling edge on $\overline{DAV}$.

If the screen is still touched at this time, the X-drivers are enabled, and the process repeats, but measures instead the X coordinate, storing the result in the X register.

If only X and Y coordinates are to be measured, then the conversion process is complete. Figure 51 shows a flowchart for this process. The time it takes to go through this process depends upon the selected resolution, internal conversion clock rate, averaging selected, panel voltage stabilization time, and precharge and sense times.

The time needed to get a complete X/Y coordinate reading can be calculated by:

$$t_{coordinate} = 2.5\ \mu s + 2\left(t_{PVS} + t_{PRE} + t_{SNS}\right) + 2N_{AVG}\left(N_{BITS}\frac{1}{f_{conv}} + 4.4\ \mu s\right) \qquad (4)$$

where:

- $t_{coordinate}$ = time to complete X/Y coordinate reading;
- t_{PVS} = panel voltage stabilization time, as given in Table 11;
- t_{PRE} = precharge time, as given in Table 18;
- t_{SNS} = sense time, as given in Table 19;
- N_{AVG} = number of averages, as given in Table 9; for no averaging, NAVG = 1;
- N_{BITS} = number of bits of resolution, as given in Table 8;
- f_{conv} = A/D converter clock frequency, as given in Table 10.

If the pressure of the touch is also to be measured, the process continues after the X-conversion is complete, measuring the Z1 and Z2 values, and placing them in the Z1 and Z2 registers. This process is illustrated in Figure 52. As before, this process time depends upon the settings described above. The time for a complete X/Y/Z1/Z2 coordinate reading is given by:

$$t_{coordinate} = 4.75\ \mu s + 3\left(t_{PVS} + t_{PRE} + t_{SNS}\right) + 4N_{AVG}\left(N_{BITS}\frac{1}{f_{conv}} + 4.4\ \mu s\right) \qquad (5)$$

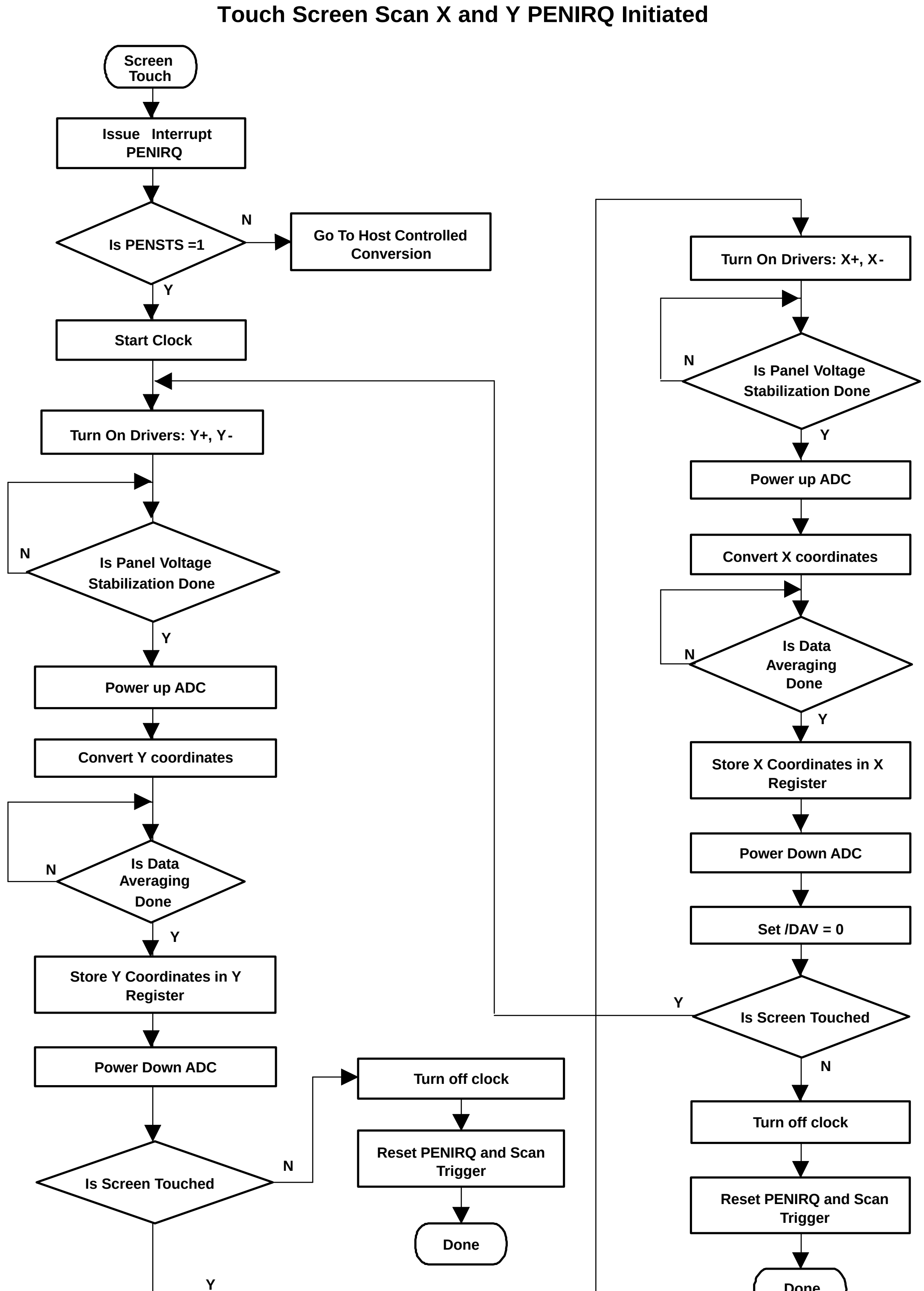


Figure 51. X & Y Coordinate Touch Screen Scan, Initiated by Touch

Touch Screen Scan X, Y and Z PENIRQ Initiated

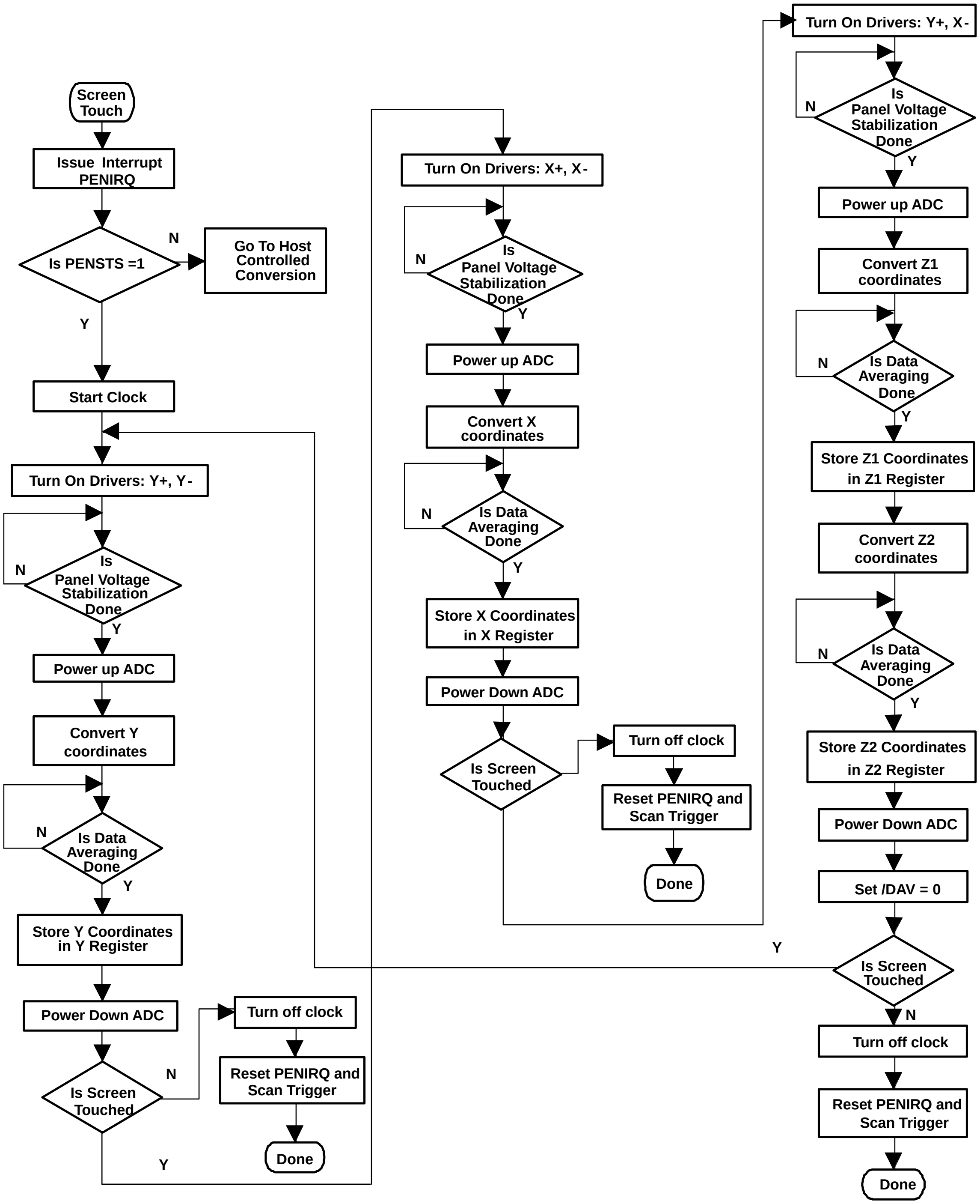


Figure 52. X,Y and Z Coordinate Touch Screen Scan, Initiated by Touch

Conversion Controlled by TSC2301 Initiated By Host Responding to PENIRQ

This mode is provided for users who want more control over the A/D conversion process. This mode requires more overhead from the host processor, so it is generally not recommended.

In this mode, the TSC2301 detects when the touch panel is touched and causes the PENIRQ line to go low. The host recognizes the interrupt request, and then writes to the ADC control register to select one of the touch screen scan functions (single X-, Y-, or Z-conversions, continuous X/Y or X/Y/Z1/Z2 Conversions). The conversion process then proceeds as described above, and as outlined in Figure 53 through Figure 57.

The main difference between this mode and the previous mode is that the host, not the TSC2301, decides when the touch screen scan begins after responding to a $\overline{\text{PENIRQ}}$. In this mode, the host must either monitor both $\overline{\text{PENIRQ}}$ and $\overline{\text{DAV}}$, or wait a minimum time after writing to the A/D converter control register. This wait time can be calculated from Equation 6 in the case of single conversions, or from Equation 4 or Equation 5 in the case of multiple conversions. The nominal conversion times calculated by these equations should be extended by approximately 12% to account for variation in the internal oscillator frequency.

Touch Screen Scan X and Y Host Initiated

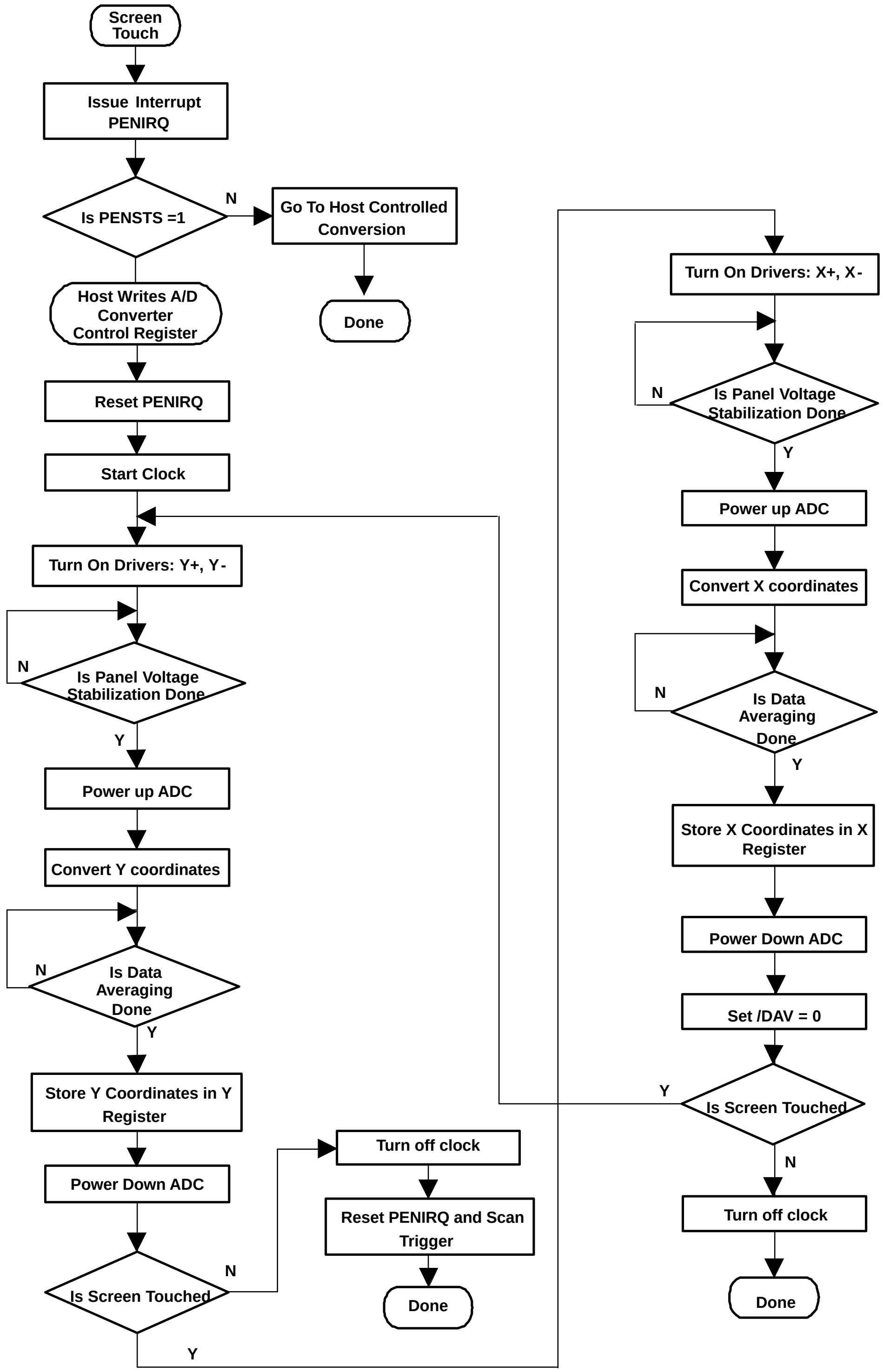


Figure 53. X and Y Coordinate Touch Screen Scan, Initiated by Host

Touch Screen Scan X, Y and Z Host Initiated

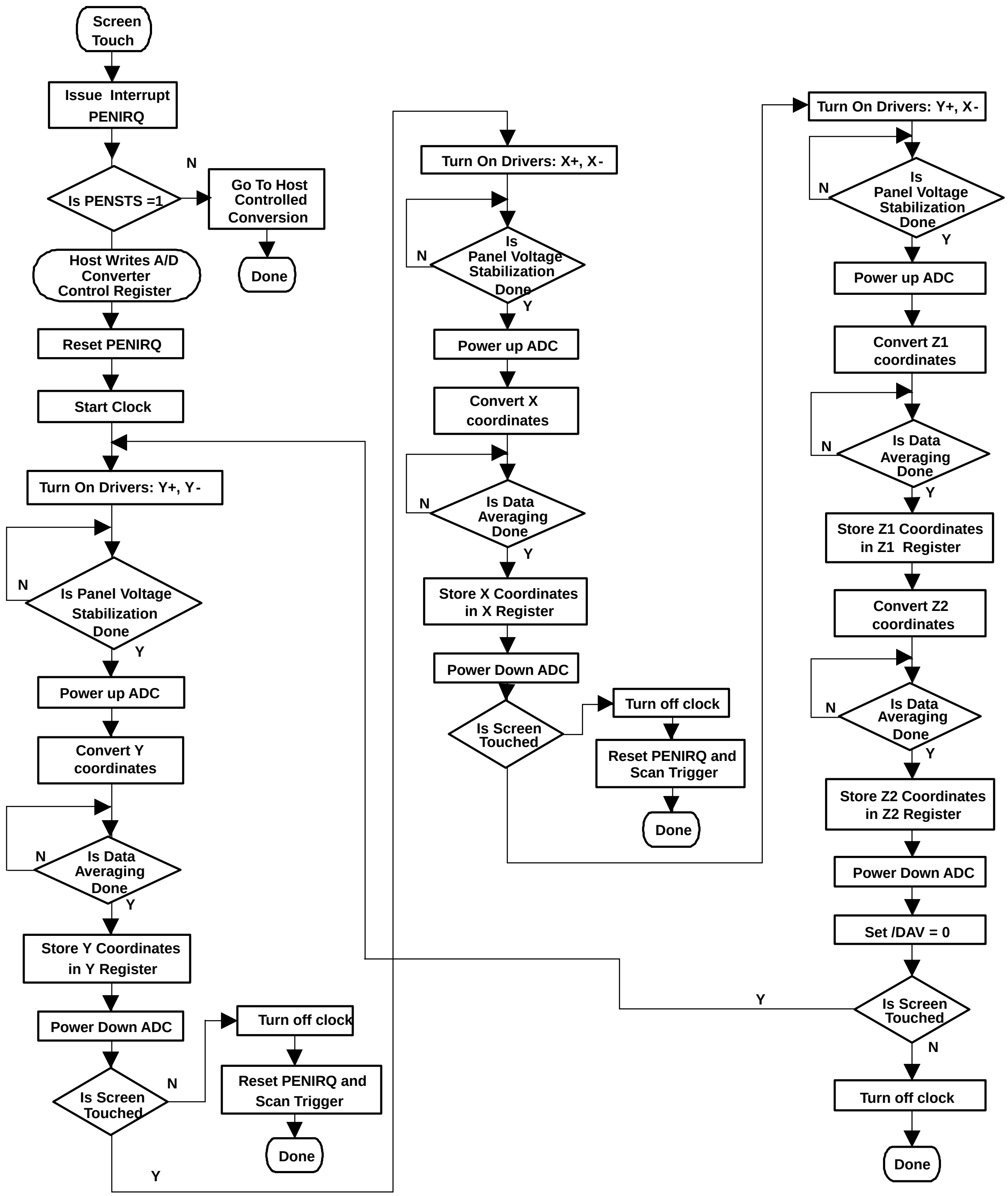


Figure 54. X,Y and Z Coordinate Touch Screen Scan, Initiated by Host

Touch Screen Scan X Coordinate Host Initiated

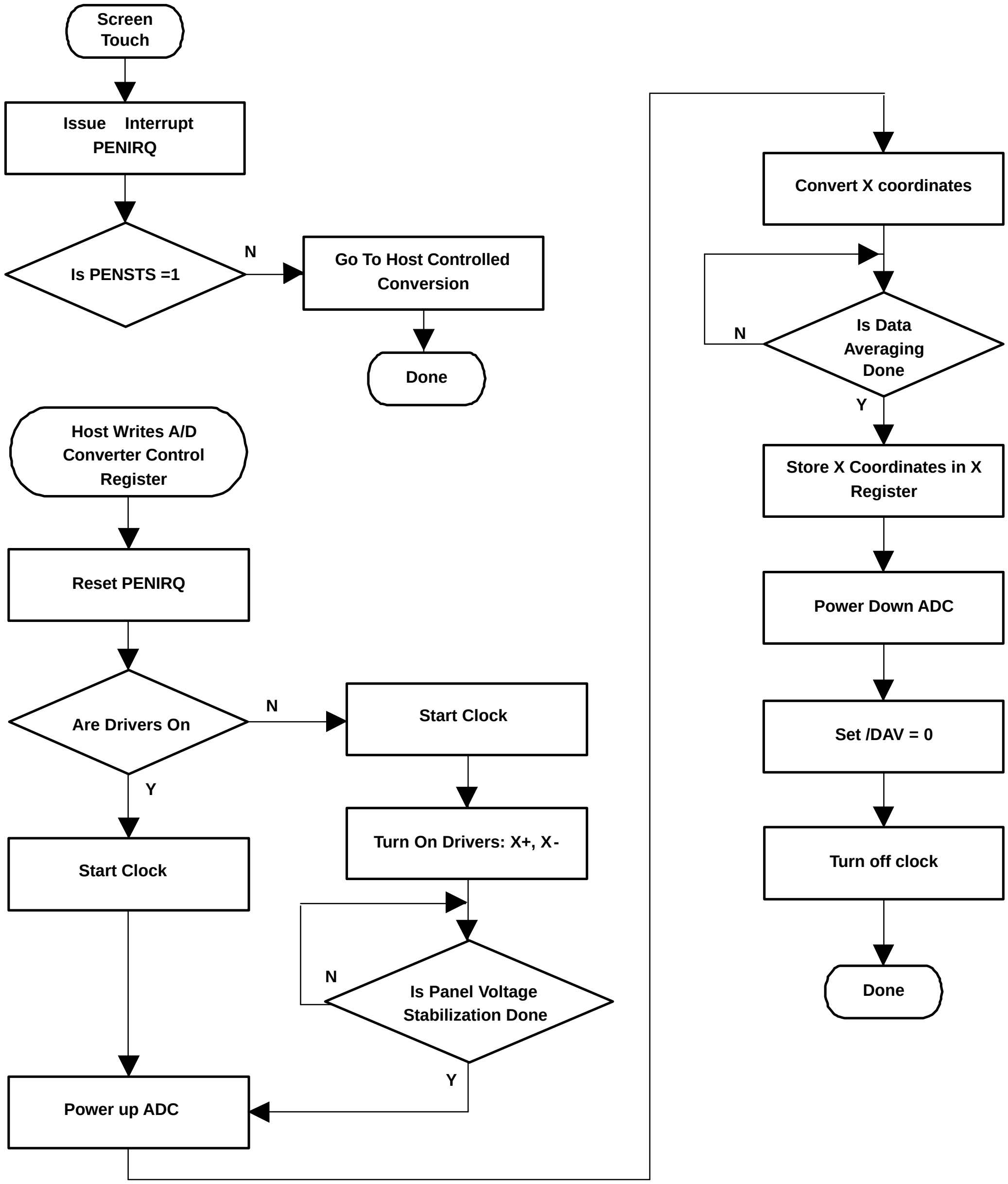


Figure 55. X Coordinate Reading Initiated by Host

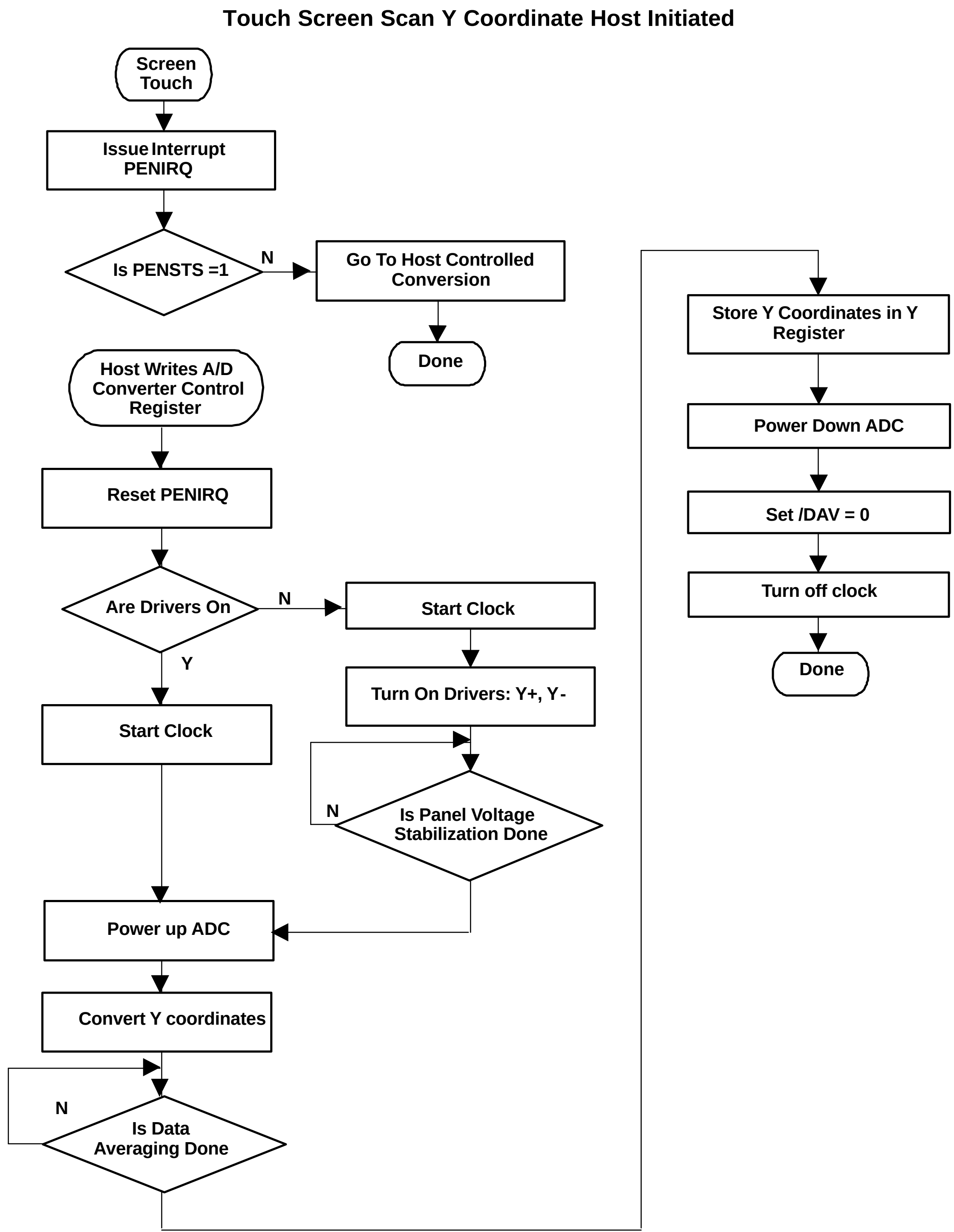


Figure 56. Y Coordinate Reading Initiated by Host

Touch Screen Scan Z Coordinate Host Initiated

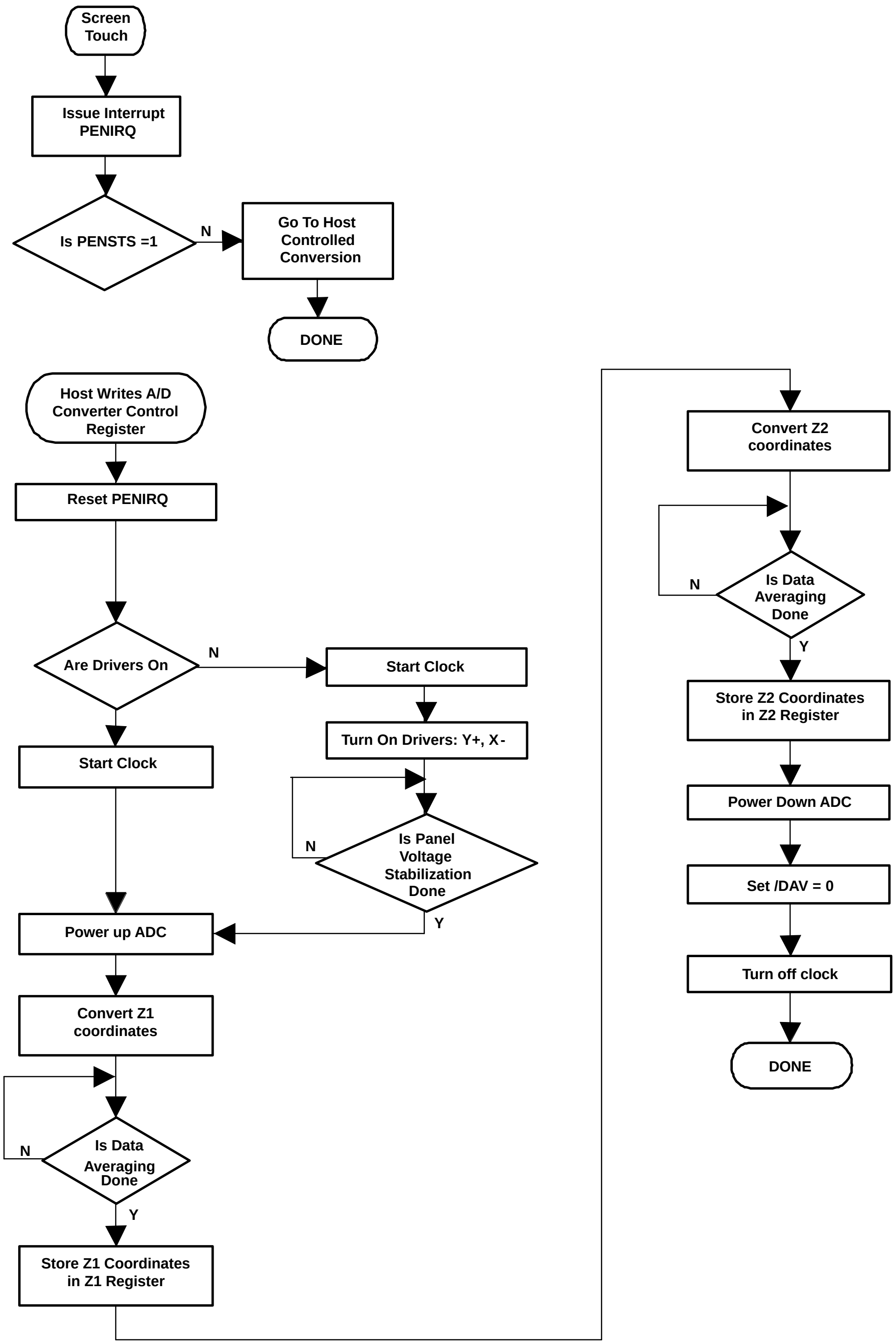


Figure 57. Z Coordinate Reading Initiated by Host

Conversion Controlled by the Host

In this mode, the TSC2301 detects when the touch panel is touched and causes the $\overline{\text{PENIRQ}}$ line to go low. The host recognizes the interrupt request. Instead of starting a sequence in the TSC2301, which then reads each coordinate in turn, the host now must control all aspects of the conversion. An example sequence would be: (a) $\overline{\text{PENIRQ}}$ goes low when screen is touched. (b) Host writes to TSC2301 to turn on X-drivers. (c) Host waits a desired delay for panel voltage stabilization. (d) Host writes to TSC2301 to begin X-conversion. After waiting for the settling time, the host then addresses the TSC2301 again, this time requesting an X coordinate conversion.

The process is then repeated for Y and Z coordinates. The processes are outlined in Figure 58 through Figure 60.

The time needed to convert any single coordinate under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{coordinate} = 2.125\ \mu s + t_{PVS} + N_{AVG}\left(N_{BITS}\frac{1}{f_{conv}} + 4.4\ \mu s\right) \tag{6}$$

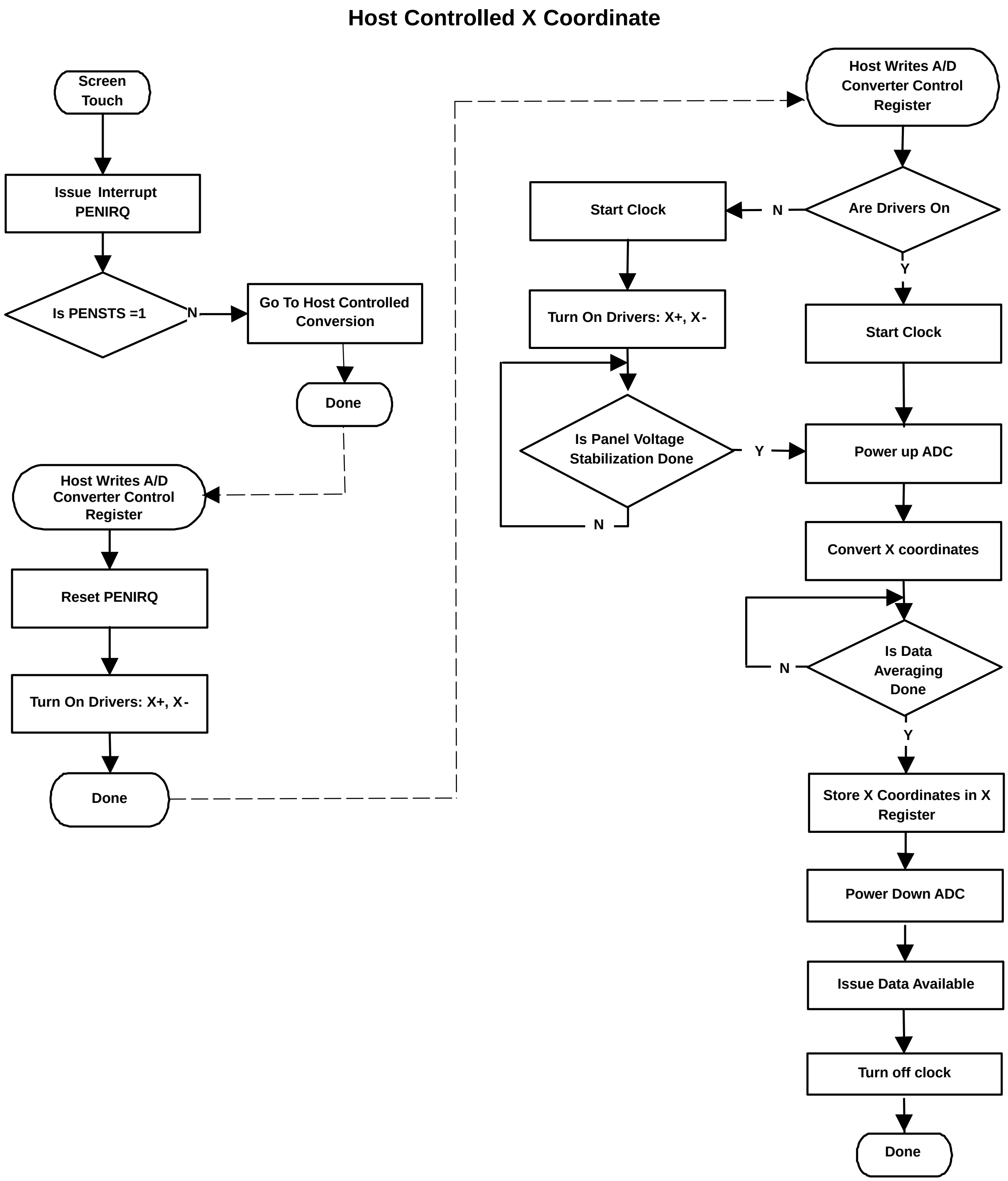


Figure 58. X Coordinate Reading Controlled by Host

Host Controlled Y Coordinate

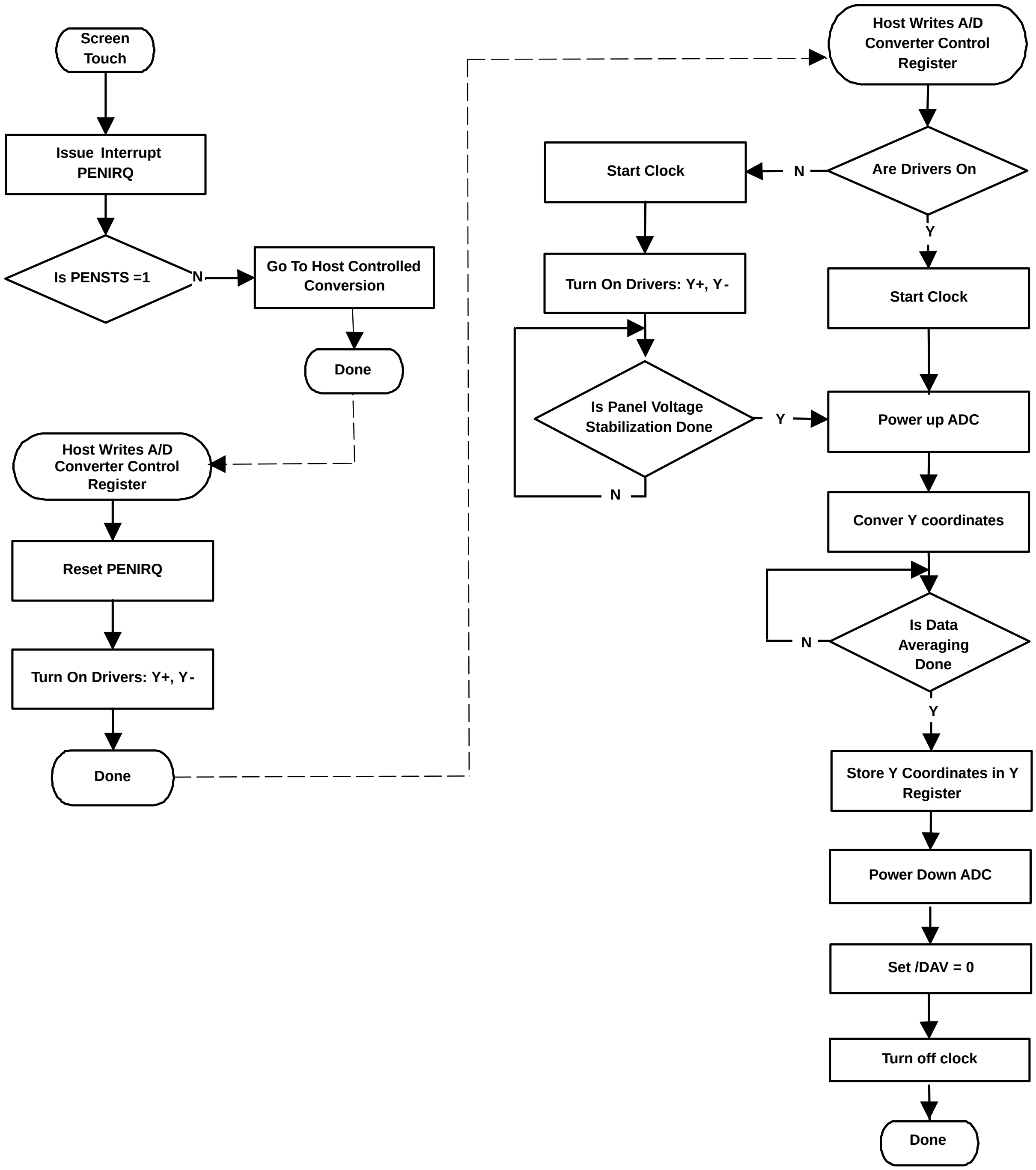


Figure 59. Y Coordinate Reading Controlled by Host

Host Controlled Z Coordinate

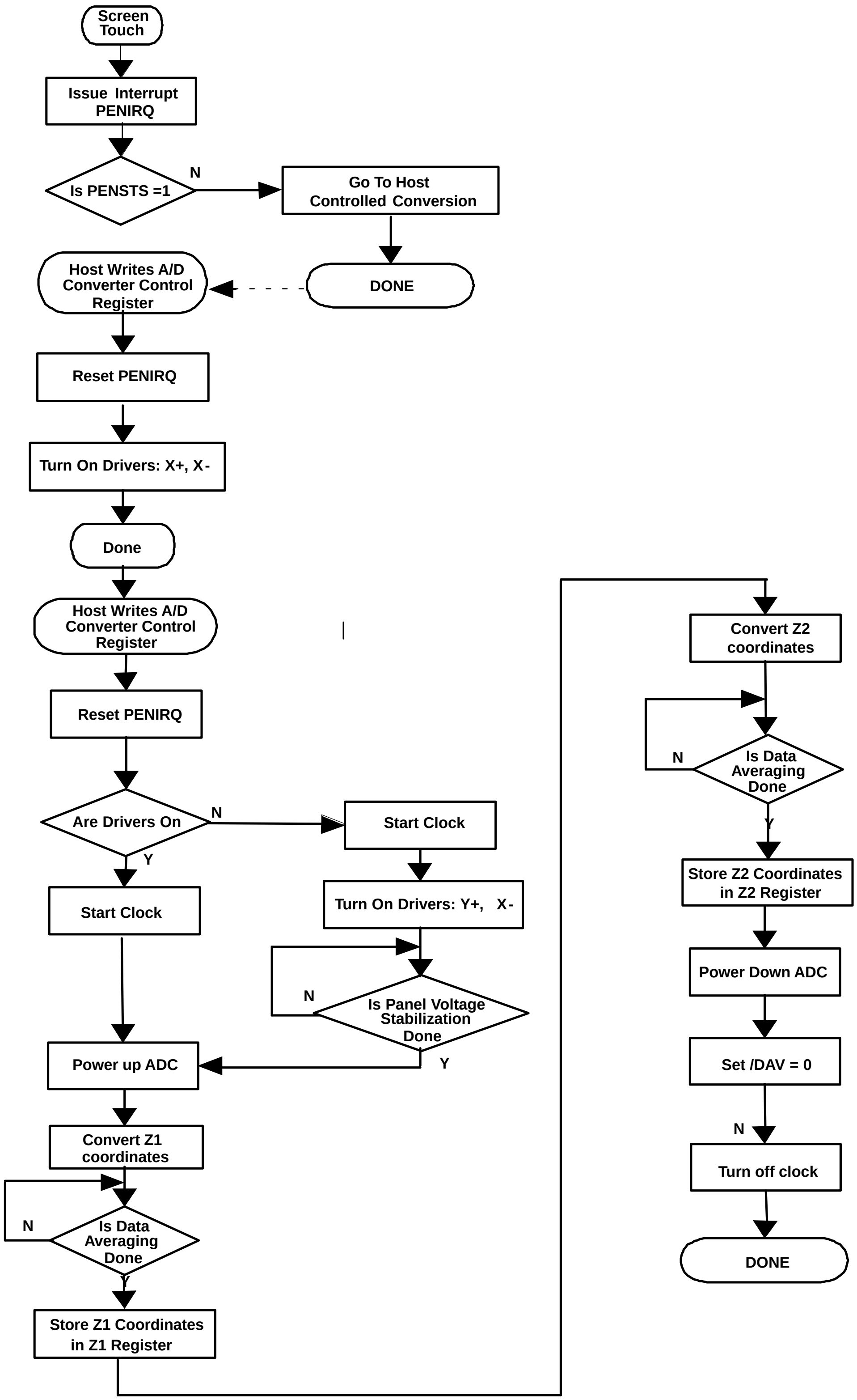


Figure 60. Z Coordinate Reading Controlled by Host

OPERATION - TEMPERATURE MEASUREMENT

In some applications, such as estimating remaining battery life or setting RAM refresh rate, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2301 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the 25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2301 offers two modes of temperature measurement. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. A diode, as shown in Figure 61, is used during this measurement cycle. The voltage across this diode is typically 600 mV at 25°C while conducting a 20-µA current. The absolute value of this diode voltage can vary several millivolts, but the temperature coefficient (TC) of this voltage is very consistent at -2.1 mV/°C. During the final test of the end product, the diode voltage would be measured by the TSC2301 ADC at a known room temperature, and the corresponding digital code stored in system memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB. This measurement of what is referred to as Temperature 1 is illustrated in Figure 62.

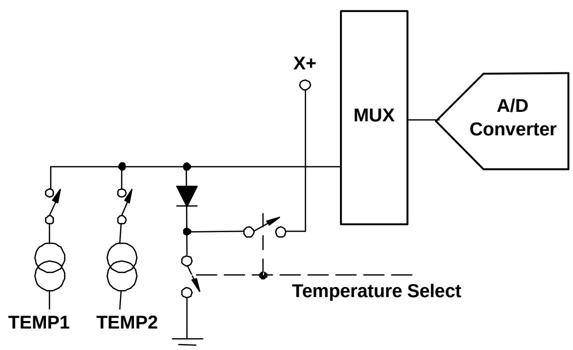


Figure 61. Functional Block Diagram of Temperature Measurement Mode

The second mode does not require a test temperature calibration, but uses a two-measurement (differential) method to eliminate the need for absolute temperature calibration, and achieves a 2°C/LSB accuracy. This mode requires a second conversion with a current 82 times larger than the first 20-µA current. The voltage difference between the first (TEMP1) and second (Temp2) conversion, using 82 times the bias current, is represented by kT/q ln (N), where N is the current ratio = 82, k = Boltzmann's constant (1.38054×10^{-23} electron volts/degree Kelvin), q = the electron charge (1.602189×10^{-19} C), and T = the temperature in degrees Kelvin. This method can provide much improved absolute temperature measurement without calibration, with resolution of 2°C/LSB. The resultant equation for solving for °K is:

$$°K = \frac{q\,\Delta V}{k\,\ell n(N)} \quad (7)$$

where:

$$\Delta V = V\left(I_{82}\right) - V\left(I_1\right) \quad (8)$$

(in mV)

$$°K = \frac{q\,\Delta V}{k\,\ell n(N)} \quad (9)$$

Temperature 2 measurement is illustrated in Figure 63.

Temperature Input 1

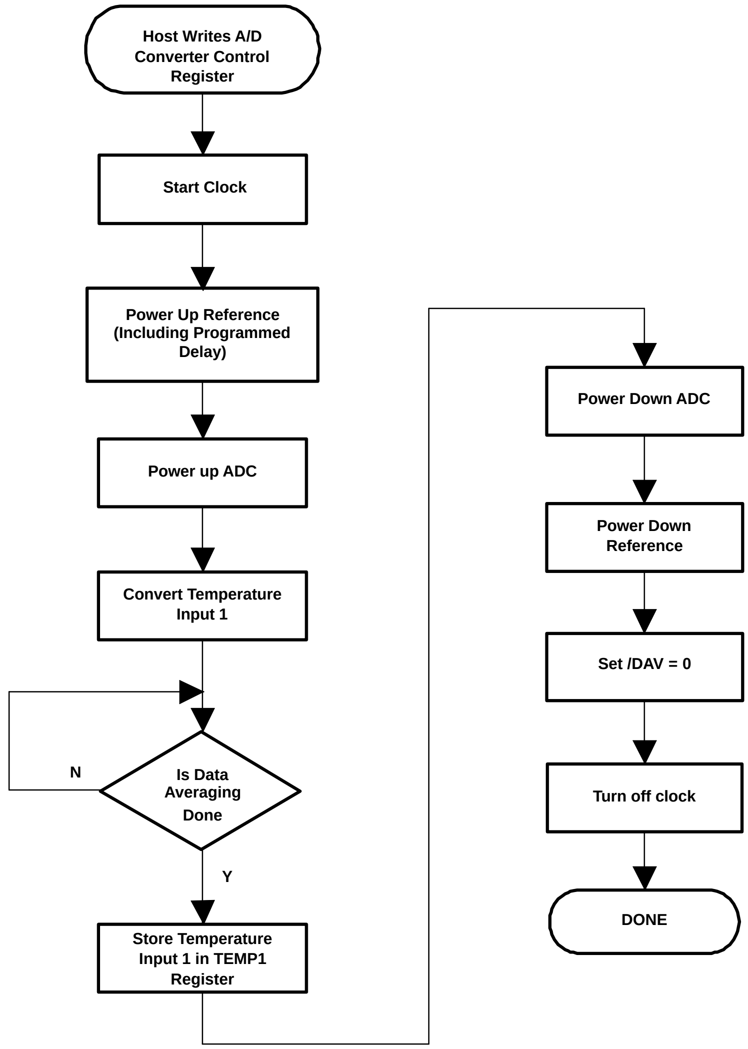


Figure 62. Single Temperature Measurement Mode

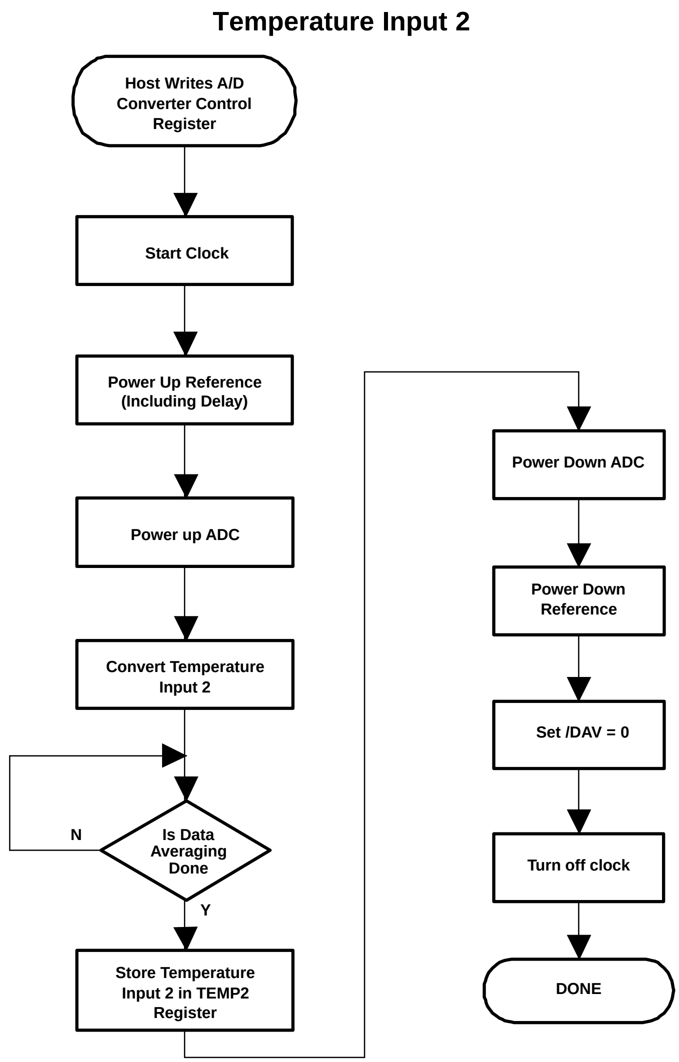
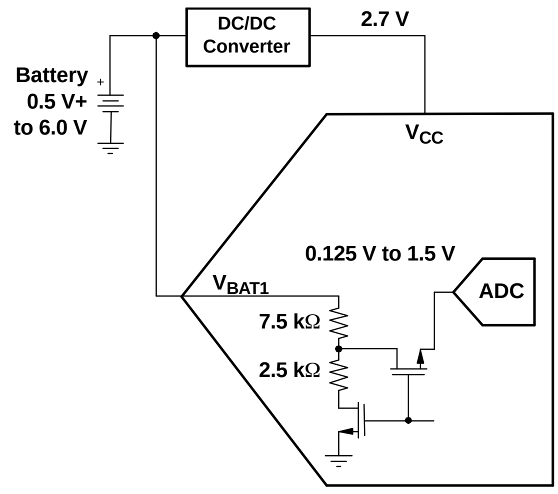


Figure 63. Additional Temperature Measurement for Differential Temperature Reading

OPERATION - BATTERY MEASUREMENT

An added feature of the TSC2301 is the ability to monitor the battery voltage which may be much larger than the supply voltage of the TSC2301. An example of this is shown in Figure 64, where a battery voltage ranging up to 6 V may be regulated by a dc/dc converter or low-dropout regulator to provide a lower supply voltage to the TSC2301. The battery voltage can vary from 0.5 V to 6 V while maintaining the voltage to the TSC2301 at a level of 2.7 V-3.6 V. The input voltage on V_{BAT1} is divided down by 4 so that a 6.0-V battery voltage is represented as 1.5 V to the A/D, while the input voltage on V_{BAT2} is divided by 2 so that 3.0-V battery voltage is represented as 1.5 V to the A/D. If the battery voltage is low enough, the 1.2 V internal reference can be used to decrease LSB size, potentially improving accuracy. The battery voltage on V_{BAT1} must be below 4* V_{REF}, and the voltage on V_{BAT2} must be below 2* V_{REF}. Due to constraints of the internal switches, the input to the A/D after the voltage divider cannot be above 1.5 V or V_{REF}, whichever is lower. In order to minimize the power consumption, the divider is only ON during the sampling of the battery input.



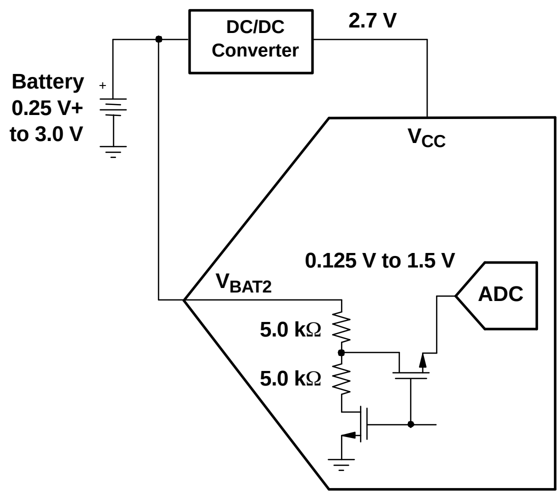


Figure 64. VBAT Example Battery Measurement Functional Block Diagrams, VDD = 2.7 V, V_{REF} = 2.5 V

Flowcharts which detail the process of making a battery input reading are shown in Figure 65 and Figure 66.

The time needed to make temperature, auxiliary, or battery measurements is given by:

$$t_{coordinate} = 2.625\ \mu s + t_{REF} + N_{AVG}\left(N_{BITS}\frac{1}{f_{conv}} + 4.4\ \mu s\right) \tag{10}$$

where t_{REF} is the reference delay time as given in Table 14.

Battery Input 1

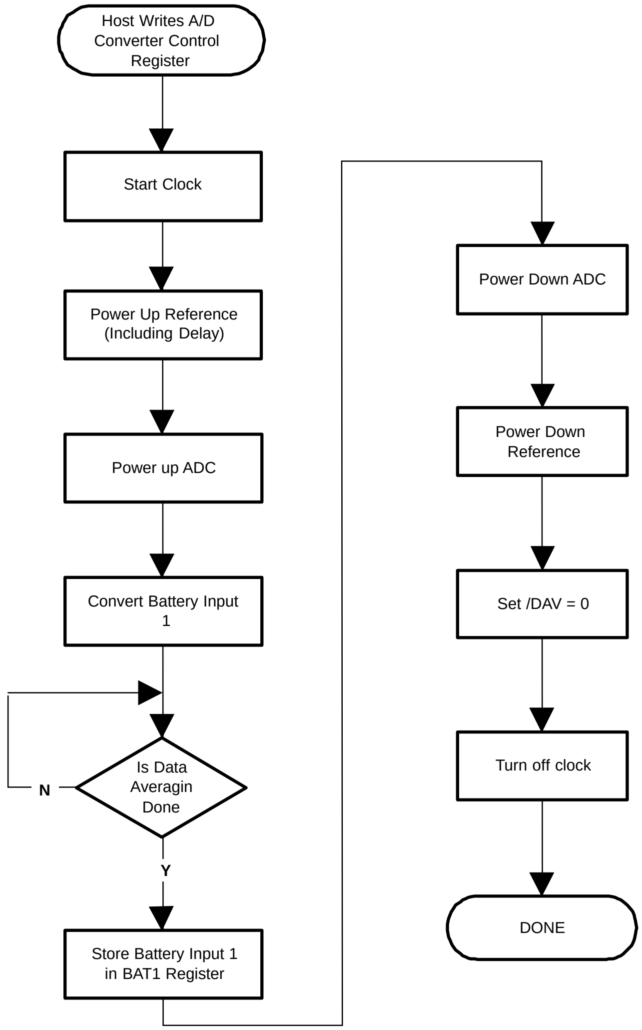


Figure 65. V_{BAT1} Measurement Process

This assumes the reference control register is configured to power up the internal reference when needed.

Battery Input 2

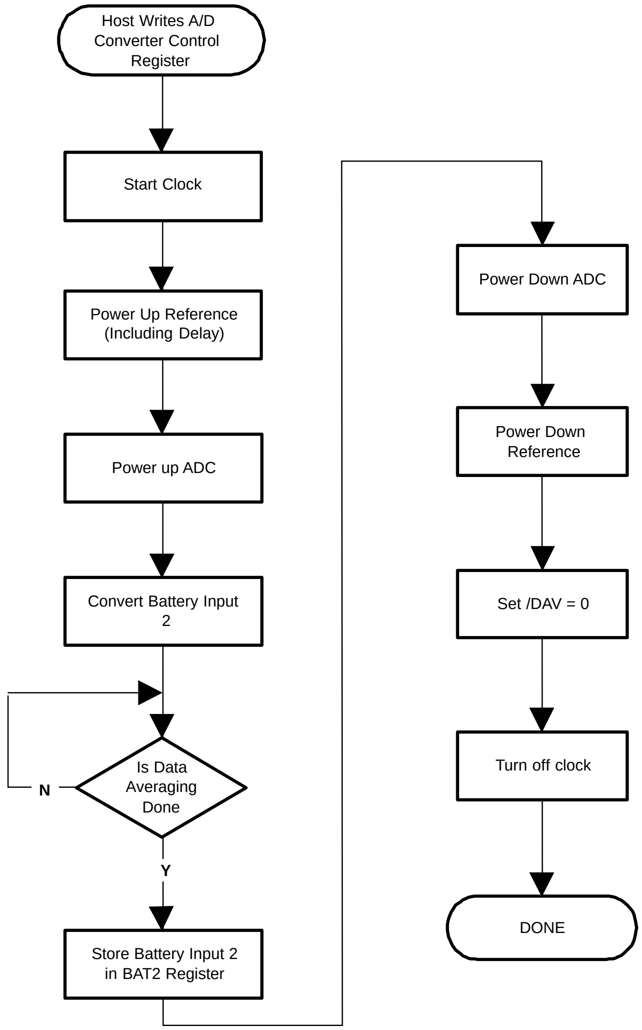


Figure 66. V_{BAT2} Measurement Process

OPERATION - AUXILIARY MEASUREMENT

The two auxiliary voltage inputs can be measured in similar fashion to the battery inputs, with no voltage dividers. The input range of the auxiliary inputs is 0 V to V_{REF}. Figure 67 and Figure 68 illustrate the process. Applications for this feature may include external temperature sensing, ambient light monitoring for controlling an LCD back-light, or sensing the current drawn from the battery.

Auxiliary Input 1

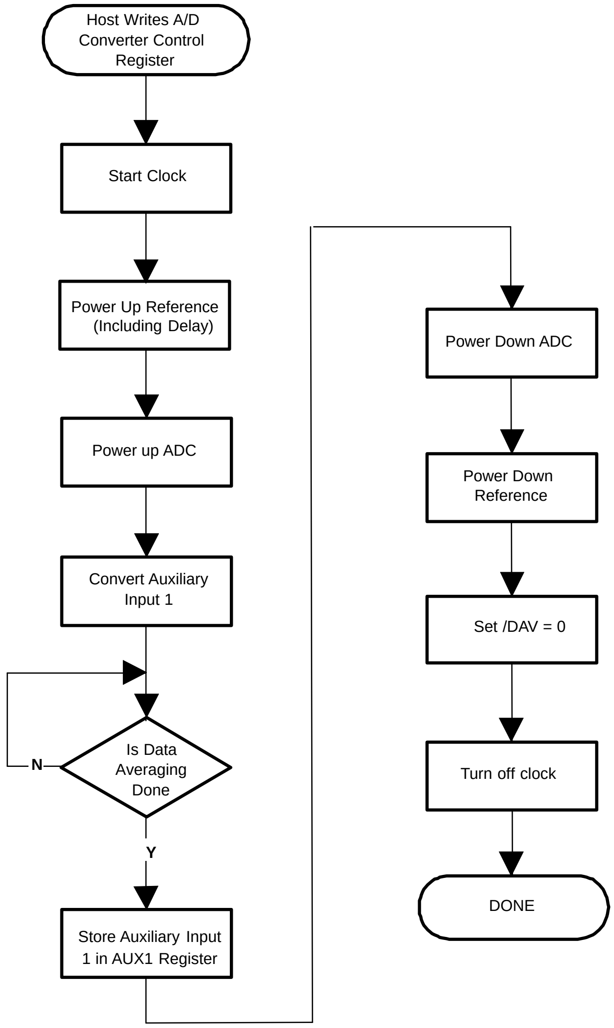


Figure 67. AUX1 Measurement Process

Auxiliary Input 2

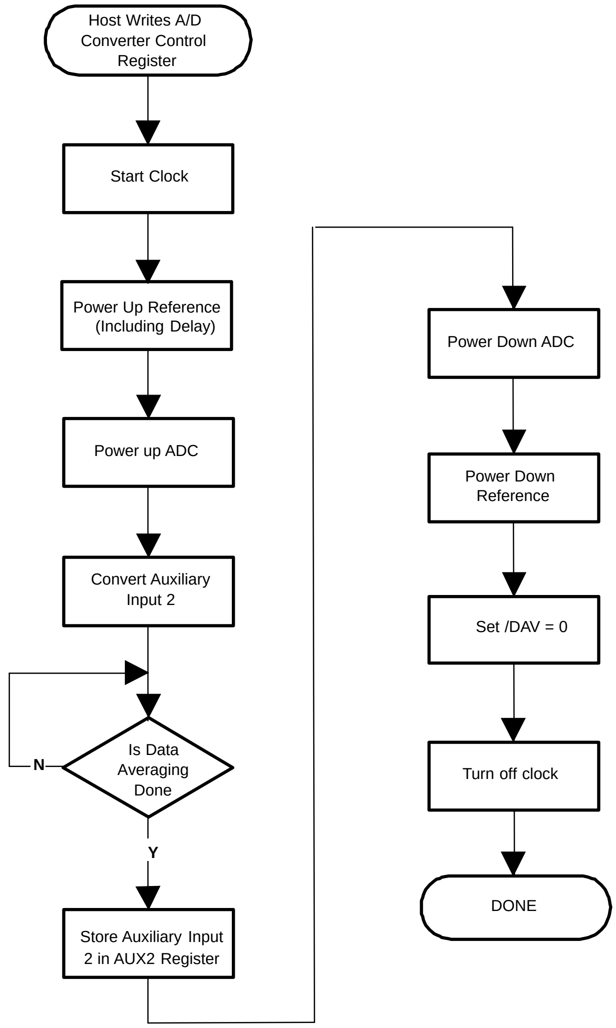


Figure 68. AUX2 Measurement Process

OPERATION - PORT SCAN

If measurements of all the battery and auxiliary inputs are required, the port scan mode can be used. This mode causes the TSC2301 to sample and convert both battery inputs and both auxiliary inputs. At the end of this cycle, the battery and auxiliary data registers contain the updated values, and the DAV pin is asserted low, signaling the host to read the data. Thus, with one write to the TSC2301, the host can cause four different measurements to be made. Because the battery and auxiliary data registers are consecutive in memory, all four registers can be read in one SPI transaction, as described in Figure 50.

The flowchart for this process is shown in Figure 69. The time needed to make a complete port scan is given by:

$$t_{coordinate} = 7.5\ \mu s + t_{REF} + 4N_{AVG}\left(N_{BITS}\frac{1}{f_{conv}} + 4.4\ \mu s\right) \qquad (11)$$

Port Scan

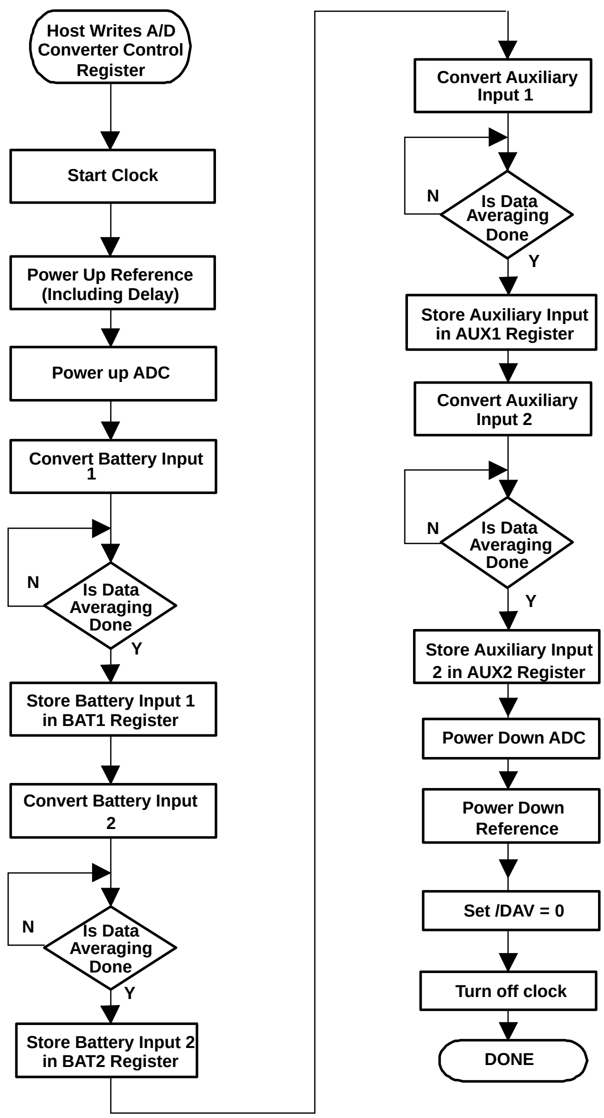


Figure 69. Port Scan Mode

OPERATION - D/A CONVERTER

The TSC2301 has an onboard 8-bit DAC, configured as shown in Figure 70. This configuration yields a current sink (AOUT) controlled by the value of a resistor connected between the ARNG pin and ground. The D/A converter has a control register, which controls whether or not the converter is powered up. The eight-bit data is written to the DAC through the DAC data register.

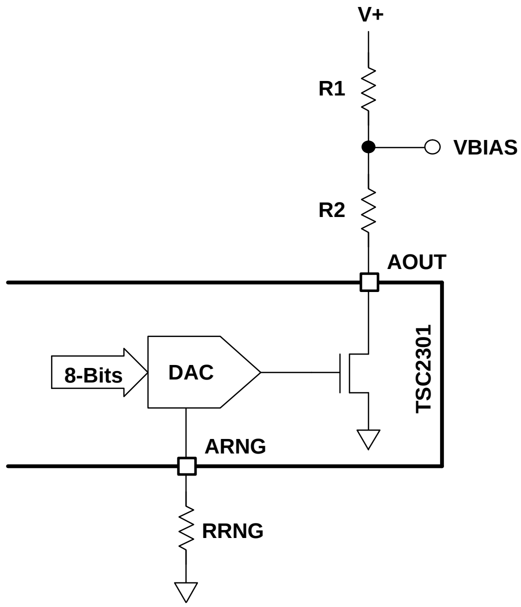


Figure 70. D/A Converter Configuration

This circuit is designed for flexibility in the output voltage at the VBIAS point shown in Figure 70 to accommodate the widely varying requirements for LCD contrast control bias. V+ can be a higher voltage than the supply voltage for the TSC2301. The only restriction is that the voltage on the AOUT pin can never go above the absolute maximum ratings for the device, and should stay above 1.5 V for linear operation.

The DAC has an output sink range which is limited to approximately 1 mA. This range can be adjusted by changing the value of RRNG shown in Figure 70. As this DAC is not designed to be a precision device, the actual value of the output current range can vary as much as ±20%. Furthermore, the current output changes due to variations in temperature; the DAC has a temperature coefficient of approximately 0.9 uA/°C.

To set the full-scale current, RRNG can be determined from the graph shown in Figure 71.

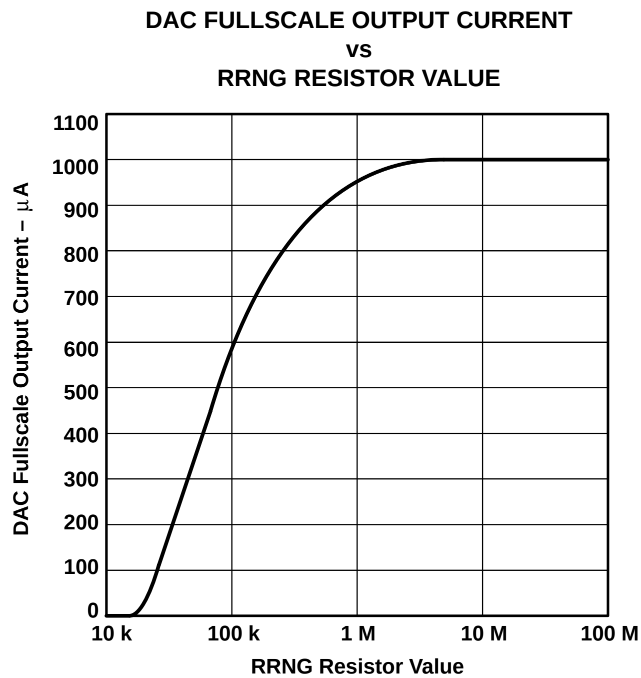


Figure 71. DAC Output Current Range vs RRNG Resistor Value

For example, consider an LCD that has a contrast control voltage VBIAS that can range from 2 V to 4 V, that draws 400 µA when used, and has an available 5-V supply. This is higher than the TSC2301 supply voltage, but it is within the absolute maximum ratings.

The maximum VBIAS voltage is 4 V, and this occurs when the D/A converter current is 0, so only the 400-µA load current ILOAD is flowing from 5 V to VBIAS. This means 1 V is dropped across R1, so R1 = 1 V/400 µA = 2.5 kΩ.

The minimum VBIAS is 2 V, which occurs when the D/A converter current is at its full scale value, IMAX. In this case, 5 V - 2 V = 3 V is dropped across R1, so the current through R1 is 3 V/2.5 kΩ = 1.2 mA. This current is IMAX + ILOAD = IMAX + 400 uA, so IMAX must be set to 800 µA. Looking at Figure 73, this means that RRNG should be around 1 MΩ.

Since the voltage at the AOUT pin must not go below 1.5 V, this limits the voltage at the bottom of R2 to be 1.5-V minimum; this occurs when the D/A converter is providing its maximum current, IMAX. In this case, IMAX +ILOAD flows through R1, and IMAX flows through R2. Thus,

R2 x IMAX + R1(IMAX + ILOAD) = 5 V - 1.5 V = 3.5 V

W R1 = 2.5 kΩ IMAX = 800 µA, ILOAD = 400 µA, thus allowing R2 to be solved as 625 Ω.

In the previous example, when the DAC current is zero, the voltage on the AOUT pin rises above the TSC2301 supply voltage. This is not a problem, however, since V+ was within the absolute maximum ratings of the TSC2301, so no special precautions are necessary. Many LCD displays require voltages much higher than the absolute maximum ratings of the TSC2301. In this case, the addition of an NPN transistor, as shown in Figure 72, protects the AOUT pin from damage.

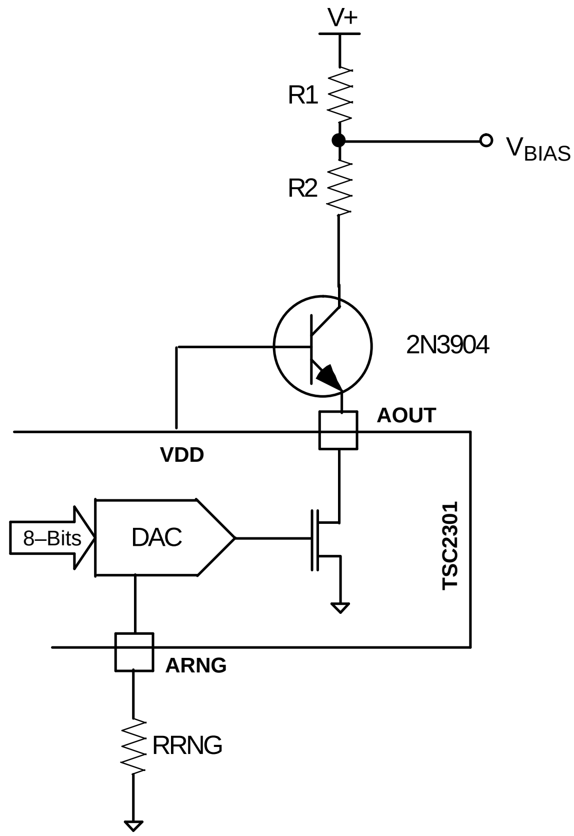


Figure 72. DAC Circuit When Using V+ Higher Than V_{supply}.

OPERATION - KEYPAD INTERFACE

The TSC2301 contains a keypad interface that is suitable for use with matrix keypads up to 4 x 4 keys. A control register, the keypad control register, is used to set the scan rate for the keypad and de-bounce times. There is also a keypad mask register which allows certain keys to be masked from being read, or from causing the TSC2301 to detect a key-press on selected keys. The results of keypad scans are placed in the keypad data register.

When a column line (keypad input) is tied to logic high, pressing on all four keys connected to that column is sensed. For example, if C1 is tied high, pressing on keys 0, 4, 8, and 12 is detected in the keypad data register. This capability is used to extend the keypad interface beyond 4 x 4 keypads.

When a key-press is detected by the TSC2301, it automatically scans the keypad and de-bounces the key-press. It then drives $\overline{KBIRQ}$ low. All keys pressed at the time of the scan are then reflected in the keypad data register. This mode is shown in Figure 73.

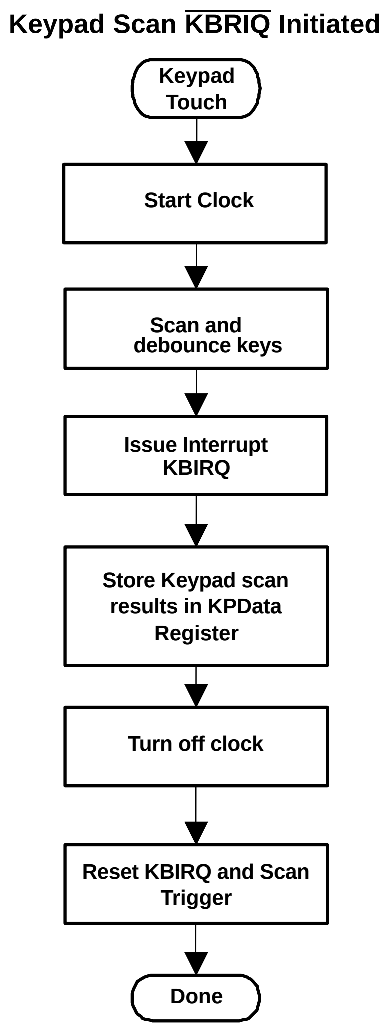


Figure 73. Keypad Scan Initiated by Keypress

AUDIO CODEC

Audio Analog I/O

The TSC2301 has one pair of stereo inputs, LLINEIN and RLINEIN, and one mono audio input, MICIN. The part also has one pair of stereo line outputs capable of driving a 10-kΩ load, VOUTL and VOUTR, as well as a stereo headphone output amplifier capable of driving a 16-Ω load at up to 30 mW/channel, HPL and HPR. Finally, the part includes a differential mono output capable of driving a 10-kΩ load per side, MONO+ and MONO-.

A special circuit has also been included for inserting a keyclick sound into the analog output signal path based on register control. This functionality is intended for generating keyclick sounds for user feedback. This function is controlled by Reg 04h, Pg 2, and is available when either of the DAC or analog bypass paths are enabled.

The common-mode voltage, VCM, used by the audio section can be powered up independently by the AVPD bit (Bit 14, Reg 05h, Pg 2). Because the audio outputs are biased to this voltage, this voltage is slowly ramped up when powered on, and there is an internally programmed delay of approximately 500 ms between powering up this voltage and unmuting the analog audio signals of the TSC2301, in order to avoid pops and clicks on the outputs. It is recommended to keep VCM powered up if the 500-ms delay is not tolerable.

Audio Digital I/O

Digital audio data samples can be transmitted between the TSC2301 and the CPU via the I^2S bus (BCLK, LRCLK, I2SDIN, I2SDOUT). However, all registers, including those pertaining to audio functionality, are only accessible via the SPI bus. The I^2S bus operates only in slave mode, meaning the BCLK and LRCLK must be provided as inputs to the part. Four programmable modes for this serial bus are supported and can be set through the I2SFM bits (Bits[1:0], Reg 00h, Pg 2) .

PCM Audio Interface

The 4-wire digital audio interface for TSC2301 is comprised of BCLK (pin 24), LRCLK (pin 25), I2SDIN (pin 26), and I2SDOUT (pin 27). For the TSC2301, these formats are selected through the I2SFM bits in Reg 00h, Pg 2. The following figures illustrate audio data input/output formats and timing.

The TSC2301 can accept 32-, 48-, or 64-bit clocks (BCKIN) in one clock of LRCIN. Only 16-bit data formats can be selected when 32-bit clocks/LRCIN are applied.

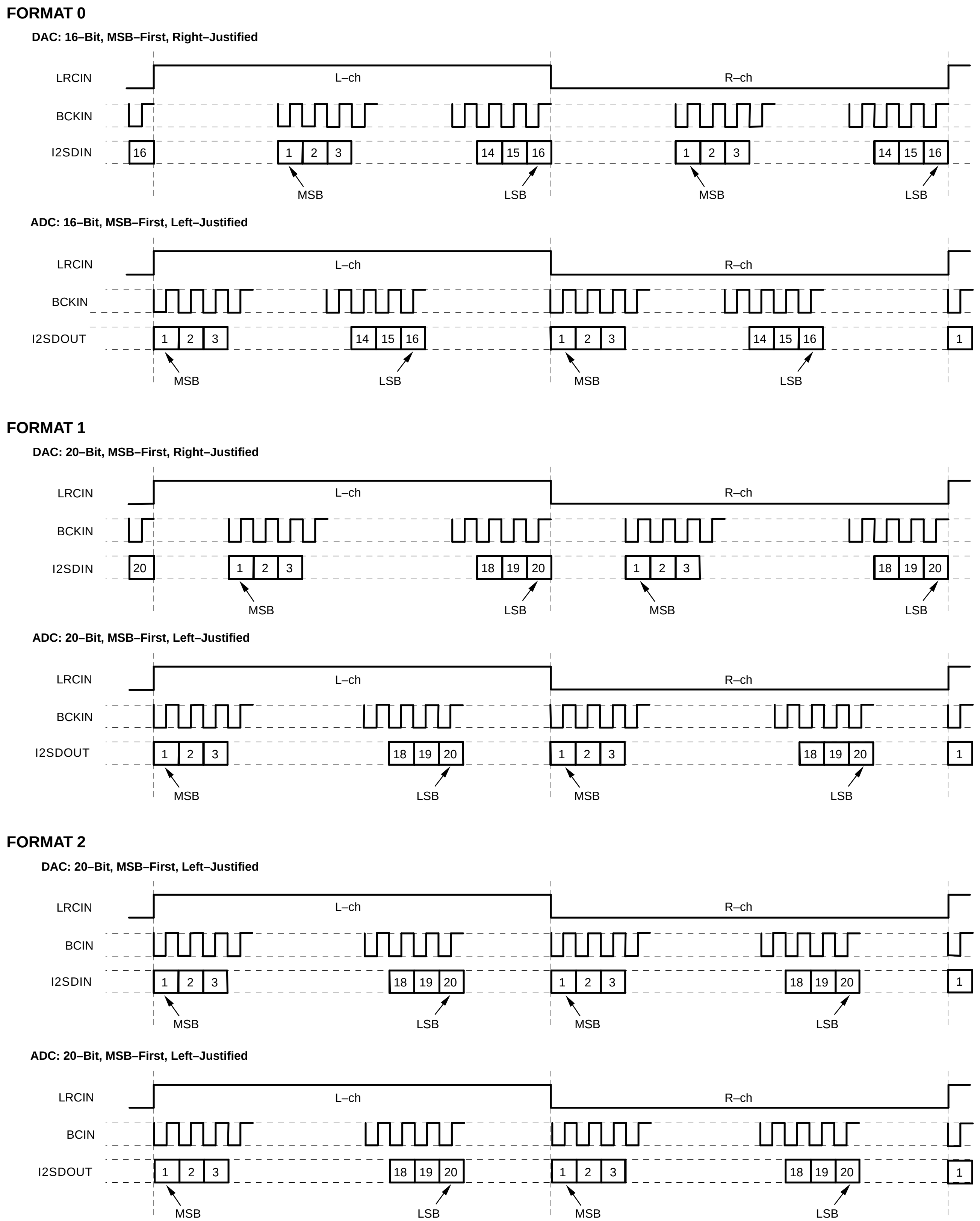


Figure 74. Audio Data Input/Output Format

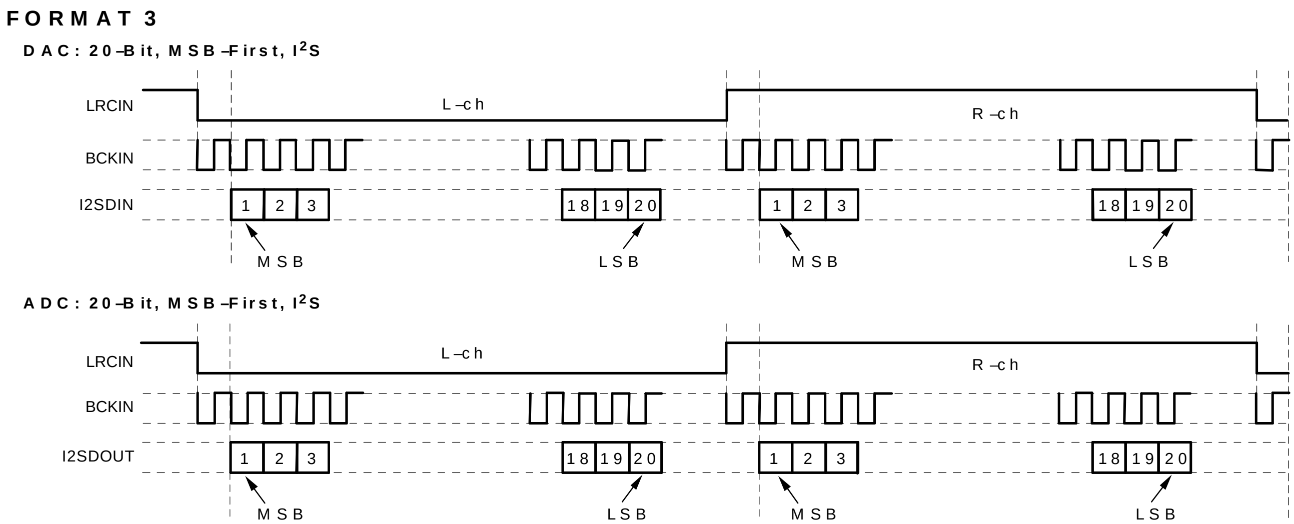


Figure 75. Audio Data Input/Output Format

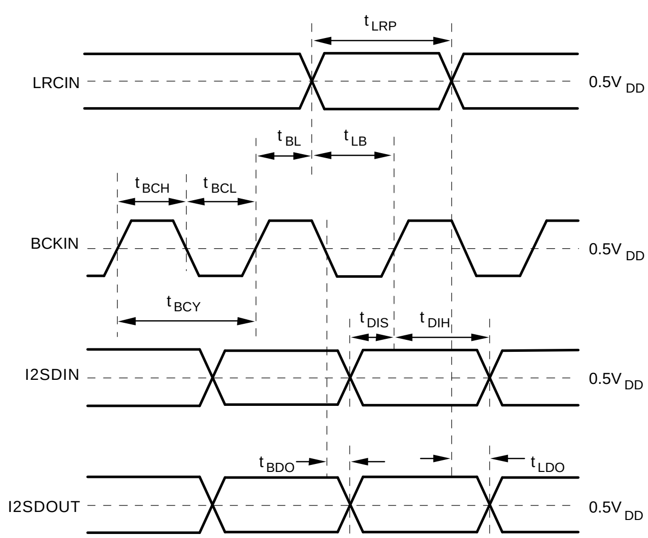


Figure 76. Audio Data Input/Output Timing

Table 29. Audio Data Input/Output Timing

Parameter	Symbol	Min	Max
BCKIN pulse cycle time	t_{BCY}	300 ns	
BCKIN pulse width high	t_{BCH}	120 ns	
BCKIN pulse width low	t_{BCL}	120 ns	
BCKIN rising edge to LRCIN edge	t_{BL}	40 ns	
LRCIN edge to BCKIN rising edge	t_{LB}	40 ns	
LRCIN pulse width	t_{LRP}	t_{BCY} ns	
I2SDIN setup time	t_{DIS}	40 ns	
I2SDIN hold time	t_{DIH}	40 ns	
I2SDOUT delay time to BCKIN falling edge	t_{BDO}		40 ns
I2SDOUT delay time to LRCIN edge	t_{LDO}		40 ns
Rising time to all signals	t_{RISE}		20 ns

Table 29. Audio Data Input/Output Timing (continued)

Parameter	Symbol	Min	Max
Falling time to all signals	t_{FALL}		20 ns

Audio Data Converters

The TSC2301 includes a stereo 20-bit audio DAC and a stereo 20-bit audio ADC. The DAC and ADC are both capable of operating at 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz. The DAC and ADC must operate at the same sampling rate.

When the ADC or DAC is operating, the part requires an audio MCLK input, which should be synchronous to the I^2S bus clock. The MCLK can be 256/384/512 times the I^2S LRCLK rate. An internal PLL takes any of these possible input clocks and generates a digital clock for use by the internal circuitry of either 44.1 kHz x 512 = 22.5792 MHz (when 44.1 kHz submultiple sample-rates are selected) or 48 kHz x 512 = 24.576 MHz (when 48 kHz submultiple sample-rates are selected). The user is required to set the MCLK bits (Bits[7:6], Reg 00h, Pg 2) to tell the part the ratio between MCLK and the I^2S LRCLK rate (there is no specific phase alignment requirement between MCLK and BCLK). The user is also required to set the I2SFS bits (Bits[5:2], Reg 00h, Pg 2) to tell the part what sample rate is in use. When the user is using either 44.1 kHz or 48-kHz sampling rates, and providing a 512 x Fs MCLK, the internal PLL is powered down, as MCLK can be used directly to clock the internal circuitry. This reduces power consumption.

If the user wishes to change sampling rates, the data converters (both DACs and ADCs) must be muted, then powered down. The LRCLK and BCLK rates must then be changed. Next the user must write the appropriate settings to the MCLK, I2SFS, and I2SFM bits, then power up the data converters. Finally, the data converters can be unmuted.

Due to the wide supply range over which this part must operate, the audio does not operate on an internal reference voltage. The common-mode voltage that the single-ended audio signals are referenced to is set by a divider between the analog supplies and is given by 0.4 x AVDD. The reference voltages used by the audio codec must be provided as inputs to the part at the Vref+/Vref- pins and are intended to be connected to the same voltage levels as AVDD and AGND, respectively. Because of this arrangement, the voltages applied to AVDD, AGND, Vref+, and Vref- should be kept as clean and noise-free as possible.

DAC Digital Volume Control

The DAC digital effects processing block implements a digital volume control that can be set through the SPI registers. The volume level can be varied from 0 dB to -63.5 dB in 0.5-dB steps independently for each channel. The user can mute each channel independently by setting the mute bits in the DAC volume control register (Reg 02h, Pg 2). There is a soft-stepping algorithm included in this block, which only changes the actual volume every 20 µs, either up or down, until the desired volume is reached. This speed of soft-stepping can be slowed to once every 40 µs through the SSRTE bit (Bit 1, Reg 04h, Pg 2).

Because of this soft-stepping, the host does not know whether the DAC has actually been fully muted or not. This may be important if the host wishes to mute the DAC before making a significant change, such as changing sample rates. In order to help with this situation, the part provides a flag back to the host via a read-only SPI register bit (Bit 0, Reg 04h, Pg 2) that alerts the host when the part has completed the soft-stepping, and the actual volume has reached the desired volume level.

The part also includes functionality to detect when the user switches on or off the de-emphasis or bass-boost functions, and to first soft-mute the DAC volume control, then change the operation of the digital effects processing, then soft-unmute the part. This avoids any possible pop/clicks in the audio output due to instantaneous changes in the filtering. A similar algorithm is used when first powering up or down the DAC/ADC. The circuit begins operation at power-up with the volume control muted, then soft-steps it up to the desired volume level slowly. At power-down, the logic first soft-steps the volume down to a mute level, then powers down the circuitry.

Stereo DAC Overview

The stereo DAC consists of a digital block to implement digital interpolation filter, volume control, de-emphasis filter and programmable digital effects/bass-boost filter for each channel. These are followed by a fifth-order single-bit digital delta-sigma modulator, and switched capacitor analog reconstruction filter. The DAC has been designed to provide enhanced performance at low sample rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed in the full audio band of 20 Hz-20 kHz, even at low sample rates such as 8 kHz. This is realized by keeping the upsampled rate approximately constant and changing the oversampling ratio as the input sample rate is reduced. For rates of 8/12/16/24/32/48 kHz, the digital delta-sigma modulator always operates at a rate of 6.144 MHz, giving oversampling ratios of 768/512/384/256/192/128, respectively. This ensures that quantization noise generated within the delta-sigma modulator stays low within the frequency band below 20 kHz at all sample rates. Similarly, for rates of 11.025/22.05/44.1 kHz, the digital delta-sigma modulator always operates at a rate of 5.6448 MHz, yielding oversampling ratios of 512/256/128, respectively.

Conventional audio DAC designs utilize high-order analog filtering to remove quantization noise that falls within the audio band when operating at low sample rates. Here, however, the increased oversampling at low sample rates keeps the noise above 20 kHz, yielding a similar noise floor out to 20 kHz whether the sample rate is 8 kHz or 48 kHz. If the audio bypass path is not in use when the stereo DAC is in use, the user should power down the bypass path, as this improves DAC SNR and reduces power consumption.

In addition, the digital interpolation filter provides enhanced image filtering to reduce signal images caused by the upsampling process that land below 20 kHz. For example, upsampling an 8-kHz signal produces signal images at multiples of 8 kHz, i.e., 8 kHz, 16 kHz, 24 kHz, etc. The images at 8 kHz and 16 kHz are below 20 kHz and thus are still audible to the listener, therefore they must be filtered heavily to maintain a good quality output. The interpolation filter is designed to maintain at least 65-dB rejection of signal images landing between 0.55 Fs and 3.5 Fs, for all sample rates, including any images that land within the audio band (20 Hz-20 kHz). Passband ripple for all sample-rate cases (from 20 Hz to 0.4535 Fs) is +/-0.1-dB maximum.

The analog reconstruction filter design consists of a switched-capacitor filter with one pole and three zeros. The single-bit data operates at 128 x 48 kHz = 6.144 MHz (for selected sample-rates that are submultiples of 48 kHz) or at 128 x 44.1 kHz = 5.6448 MHz (for selected sample-rates that are submultiples of 44.1 kHz). The interpolation filter takes data at the selected sample-rate from the effects processing block, then performs upsampling and image filtering, yielding a 6.144-MHz or 5.6448-MHz data stream, which is provided to the digital delta-sigma modulator.

Audio DAC SNR performance is 98-dB-A typical over 20 Hz–20 kHz bandwidth in 44.1/48-kHz mode at the line-outputs with a 3.3-V supply level.

DAC Digital De-Emphasis

The DAC digital effects processing block can perform several operations on the audio data before it is passed to the interpolation filter. One such operation is a digital de-emphasis, which can be enabled or disabled by the user via the DEEMP bit (Bit 0, Reg 05h, Pg 2). This is only available for sample rates of 32 kHz, 44.1 kHz, and 48 kHz. The transfer function consists of a pole with time constant of 50 µs and a zero with time constant of 15 µs.

DAC Programmable Digital Effects Filter

The DAC digital effects processing block also includes a fourth order digital IIR filter with programmable coefficients (independently programmable per channel). The filter transfer function is given by:

$$\left(\frac{N0 + 2\,N1\,Z^{-1} + N2\,Z^{-2}}{32768 - 2\,D1\,Z^{-1} - D2\,Z^{-2}}\right)\left(\frac{N3 + 2\,N4\,Z^{-1} + N5\,Z^{-2}}{32768 - 2\,D4\,Z^{-1} - D5\,Z^{-2}}\right) \tag{13}$$

The N and D coefficients are set via SPI registers, and this filter can be enabled or disabled via the BASS bit (Bit 1, Reg 05h, Pg 2). This functionality can implement a number of different functions, such as bass-boost (default), treble-boost, mid-boost, or other equalization. This transfer function(s) can be determined by the user and loaded to the TSC2301 at power-up, and the feature can then be switched on or off by the user during normal operation. If a filter with gain over 0 dB is designed and used, and large-scale signals are played at high amplitude through the DAC, overloading and undesirable effects can occur.

The default coefficients at reset are given by:

N0 = N3 = 27618 D1 = D4 = 32130

N1 = N4 = -27033 D2 = D5 = -31505

N2 = N5 = 26461

which implements the bass-boost transfer function shown in Figure 77, having a 3-dB attenuation for signals above approximately 150 Hz when operating at a 48-kHz sampling rate. All coefficients are represented by 16-bit twos complement integers with values ranging from -32768 to 32767.

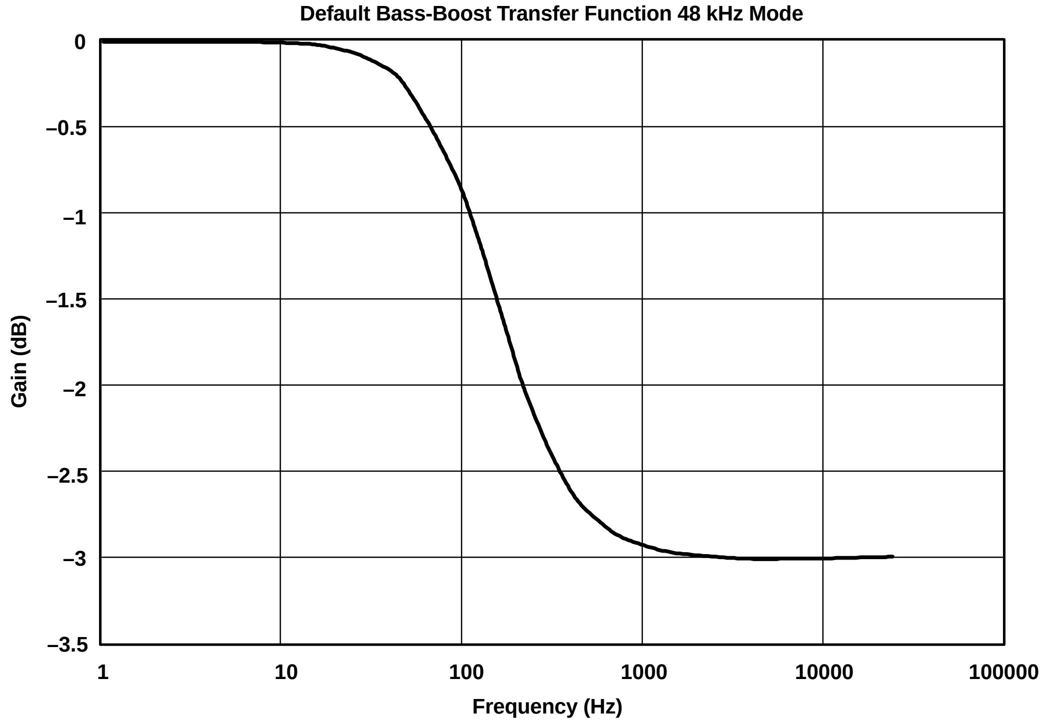


Figure 77. Transfer Function of Default Bass-Boost Filter Coefficients at 48-kHz Sampling Rate

Audio ADC

The audio ADC consists of a 4th order multi-bit analog delta-sigma modulator, followed by a digital decimation filter. The digital output data is then passed to the bus interface for transmission back to the CPU.

The analog modulator is a fully differential switched-capacitor design with multi-bit quantizer and dynamic element matching to avoid mismatch errors. The modulator operates at an oversampling ratio of 128 for all sample rates. The input to the ADC is filtered by a single-pole analog filter with -3-dB point at approximately 500 kHz for antialiasing. This analog filter uses a single off-chip 1 nF cap per ADC (at the AFILT pins) and on-chip resistor.

The digital decimation filter block includes a high-pass IIR filter for the purpose of removing any dc or sub-audio-frequency component from the signal. Since such a low frequency filter can have significant settling time, the filter has an adjustable cutoff frequency, in order to allow the host to set a faster settling time initially, then later switch it back to a level that does not affect the audio band. The settings for this high-pass filter are:

HPF -3-dB frequency: 0.000019 Fs (0.912 Hz at Fs = 48 kHz)

0.000078 Fs (3.744 Hz at Fs = 48 kHz)

0.1 Fs (4.8 kHz at Fs = 48 kHz)

The filter block provides an audio passband ripple of +/-0.03 dB over a passband from 0 Hz to 0.454 sampling frequency (Fs), and 70-dB minimum stopband attenuation from 0.548 Fs to 64 Fs.

The ADC modulator and digital filter operate on a clock that changes directly with Fs. This is in contrast to the DAC, which keeps the modulator running at a high rate of 128 x 44.1 kHz or 128 x 48 kHz even if the incoming data rate is much lower, such as 8 kHz. Group delay of the ADC path varies with sampling frequency and is given by 28.7/Fs.

Audio ADC SNR performance is 88-dB-A typical over 20-Hz - 20-kHz bandwidth in 44.1/48-kHz mode with a 3.3-V supply level.

Each audio ADC is preceded by an analog volume control with gain programmable from 20 dB to -40 dB or mute in 0.5-dB steps using Reg 01h, Pg 2. The input to these volume controls are selected as LLINEIN, RLINEIN, MICIN, or a mono mix of LLINEIN and RLINEIN through the INML bits (Bits [13:12], Reg 00h, Pg 2). An additional preamp gain is selectable on the MICIN input as 0 dB, 6 dB, or 12 dB using the MICG bits (Bits [9:8], Reg 00h, Pg 2).

Audio Bypass Mode

In audio bypass mode, the L/RLINEIN analog inputs can be routed to mix with the DAC output and play to the line-outputs (VOUTL/R) as well as the headphone outputs (HPL/R) and mono output (MONO+/-). This path has a stereo analog volume control associated with it, with range settings from 12.0 dB to -35.5 dB in 0.5-dB steps. If the audio ADCs and DACs are not used while the bypass path is in use, the ADCs and DAC must be powered down to improve noise performance and reduce power consumption.

This analog volume control has soft-stepping logic associated with it, so that when a volume change is made via the SPI bus, the logic changes the actual volume incrementally, single-stepping the actual volume up or down once every 20 µsec until it reaches the desired volume level.

This volume control also has similar algorithms as the ADC/DAC volume controls, in that the volume starts at mute upon power-up, then is slowly single-stepped up to the desired level. At a power-down request, the volume is slowly single-stepped down to mute before the circuit is actually powered down.

Differential Monophonic Output (MONO+/-)

The differential mono output of the TSC2301 can be used to drive a power amplifier which drives a low-impedance speaker. This block can output either a mono mix of the stereo line outputs, or the analog input to the left-channel ADC. This is selected through the MONS bit (Bit 2, Reg 04h, Pg 2). The mono mix of the line outputs is represented by the equation VOUTL/2 + VOUTR/2. Similarly, the mono mix of the analog line inputs is represented by LLINEIN/2 + RLINEIN/2.

Microphone Bias Voltage (MICBIAS)

The TSC2301 provides an output voltage suitable for biasing an electret microphone capsule. This voltage is always 1 V below the supply voltage of the part. This output can be disabled through the MIBPD bit (Bit 6, Reg 05h, Pg 2) to reduce power consumption if not used.

Power Consumption

The TSC2301 provides maximum flexibility to the user for control of power consumption. Towards that end, every section of the TSC2301 audio codec can be independently powered down. The power down status of the different sections is controlled by Reg 05h in Pg 2. The analog bypass path, headphone amplifier, mono output, stereo DAC, left channel ADC, right channel ADC, microphone bias, crystal oscillator, and oscillator clock buffer sections can all be powered down independently. It is recommended that the end-user power down all unused sections whenever possible in order to minimize power consumption. Below is a table showing power consumption in different modes of operation.

Table 30. Power Consumption by Mode of Operation

Operating Mode Description	Register 05h Bit Values											Power Consumption	
												Typ	Units
	15	14	13	12	11	10	9	8	6	5	4		
Stereo Record and Playback													
Mono record, line playback, 48 kHz	0	0	1	1	1	0	0	1	1	0	0	45	mW
Mono record, line playback, 8 kHz	0	0	1	1	1	0	0	1	1	0	0	38	mW
Stereo record, line playback, 48 kHz	0	0	1	1	1	0	0	0	1	0	0	60	mW
Stereo record, line playback, 8 kHz	0	0	1	1	1	0	0	0	1	0	0	48	mW
Stereo Playback Only													
Line playback only, 48 kHz	0	0	1	1	1	0	1	1	1	0	0	28	mW
Headphone playback only, 48 kHz	0	0	1	0	1	0	1	1	1	0	0	34	mW
Record Only													
Stereo line record only, 48 kHz	0	0	1	1	1	1	0	0	1	0	0	34	mW
Stereo line record only, 8 kHz	0	0	1	1	1	1	0	0	1	0	0	26	mW
Mono record, 48 kHz	0	0	1	1	1	1	0	1	1	0	0	19	mW
Mono record only, 8 kHz	0	0	1	1	1	1	0	1	1	0	0	15	mW
Analog Bypass													
Line in to line out	0	0	0	1	1	1	1	1	1	0	0	10	mW
Line in to headphone out	0	0	0	0	1	1	1	1	1	0	0	13	mW
Power Down													
Power down all	1	1	X	X	X	X	X	X	X	0	0	0.5	µW
Power down, VCM enabled	1	0	X	X	X	X	X	X	X	0	0	0.8	µW

TSC2301 AUDIO CONTROL REGISTERS

TSC2301 Audio Control Register (Page 2, Address 00H)

The audio control register of the TSC2301 controls the digital audio interface, the microphone preamp gain, the record multiplexer settings, and the ADC highpass filter pole. This register determines which ADC high pass filter response is selected, as well as which audio inputs are connected to the stereo ADCs. The gain of the MIC input (0 to 12 dB) is also selected. This register is also used to tell the data converters the frequency of MCLK, along with the frequency of LRCLK (ADC and DAC sample rates). The format of the audio data is also selected.

The audio control register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
HPF1	HPF0	INML1	INML0	INMR1	INMR0	MICG 1	MICG 0	MCLK 1	MCLK 0	I2SFS 3	I2SFS 2	I2SFS 1	I2SFS 0	I2SFM 1	I2SFM0

Bits [15:14] — HPF1-HPF0

ADC High Pass Filter. These two bits select the pass-band for the high-pass filter or disable the filter. The default state of the filter is enabled, with -3-dB frequency at 0.000019xFs.

Table 31. High-Pass Filter Operation

HPF[1:0]		
HPF1	**HPF0**	**Description**
0	0	HPF Disabled, signal passes through unaltered
0	1	HPF -3-dB frequency = 0.1xFs
1	0	HPF -3-dB frequency = 0.000078xFs
1	1	HPF -3-dB frequency = 0.000019xFs (default)

Bits [13:12] — INML1-INML0

Left Audio ADC Input Multiplexer. These two bits select the analog input for the left channel ADC. The input to the left channel ADC can come from the microphone input, right line input, left line input, or from a *mono mix* of the left and right line inputs. The default input to the left channel ADC is the microphone input.

Table 32. Left Audio ADC Input Selection

INML[1:0]		
INML1	**INML0**	**Description**
0	0	ADCL input = MIC (default)
0	1	ADCL input = LLINEIN
1	0	ADCL input = RLINEIN
1	1	ADCL input = (RLINEIN+LLINEIN)/2

Bits [11:10] — INMR1-INMR0

Right Audio ADC Input Multiplexer. These two bits select the analog input for the right channel ADC. The input to the right channel ADC can come from the microphone input, right line input, left line input, or from a *mono mix* of the left and right line inputs. The default input to the right channel ADC is the microphone input.

Table 33. Right Audio ADC Input Selection

INMR[1:0]		
INMR1	**INMR0**	**Description**
0	0	ADCR input = MIC (default)
0	1	ADCR input = LLINEIN
1	0	ADCR input = RLINEIN
1	1	ADCR input = (RLINEIN+LLINEIN)/2

Bits [9:8] — MICG1-MICG0

Microphone Preamp Gain. These two bits select the gain of the microphone input channel. The gain of the microphone input channel can be 0 dB, 6 dB, or 12 dB. The default gain of the microphone input channel is 0 dB.

Table 34. Microphone Input Gain Selection

MICG[1:0]		
MICG1	**MICG0**	**Description**
0	0	MIC gain = 0 dB (default)
0	1	MIC gain = 0 dB
1	0	MIC gain = 6 dB
1	1	MIC gain = 12 dB

Bits [7:6] — MCLK1-MCLK0

Master Clock Ratio. These two bits select the ratio of the audio master clock frequency to the audio sampling frequency. The ratio can be 256 Fs, 384 Fs, or 512 Fs. The default master clock frequency is 256 Fs.

Table 35. Master Clock Ratio Selection

MCLK[1:0]		
MCLK1	**MCLK0**	**Description**
0	0	Master clock (MCLK) = 256 x Fs (default)
0	1	Master clock (MCLK) = 384 x Fs
1	0	Master clock (MCLK) = 512 x Fs
1	1	Master clock (MCLK) = 256 x Fs

Bits [5:2] — I2SFS3-I2SFS0

I^2S Sample Rate. These bits tell the internal PLL what the audio sampling rate is so that it provides the proper clock rate to the data converters and the digital filters. The default sample rate is 48 kHz. See Table 36 for a complete listing of available sampling rates. All combinations of I2SFS[3:0] not in Table 36 are not valid.

Table 36. I^2S Sample Rate Select

I2SFS3	I2SFS2	I2SFS1	I2SFS0	Function
0	0	0	0	Fs = 48 kHz (default)
0	0	0	1	Fs = 44.1 kHz
0	0	1	0	Fs = 32 kHz
0	0	1	1	Fs = 24 kHz
0	1	0	0	Fs = 22.05 kHz
0	1	0	1	Fs = 16 kHz
0	1	1	0	Fs = 12 kHz
0	1	1	1	Fs = 11.05 kHz
1	0	0	0	Fs = 8 kHz

Bits [1:0] — I2SFM1-I2SFM0

I^2S Format. These two bits select the I^2S interface format. Both 16-bit and 20-bit data formats are supported. The default format is 20-bit I^2S.

Table 37. I^2S Format Selection

I2SFM [1:0]		
I2SFM1	**I2SFM0**	**Description**
0	0	DAC: 16-bit, MSB-first, right justified ADC: 16-bit, MSB-first, left justified
0	1	DAC: 20-bit, MSB-first, right justified ADC: 20-bit, MSB-first, left justified
1	0	DAC: 20-bit, MSB-first, left justified ADC: 20-bit, MSB-first, left justified
1	1	DAC: 20-bit, MSB-first, I^2S (default) ADC: 20-bit, MSB-first, I^2S (default)

ADC VOLUME CONTROL REGISTER (Page 2, Address 01h)

The ADC volume control register controls the independent programmable gain amplifiers (PGA's) on the left and right channel inputs to the audio ADCs of the TSC2301. The gain of these PGAs can be adjusted from

-40 dB to 20 dB in 0.5-dB steps. The ADC inputs can also be *hard-muted*, or internally shorted to VCM so that no input signal is seen.

The ADC volume control register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
ADMUL	ADVL6	ADVL5	ADVL4	ADVL3	ADVL2	ADVL1	ADVL0	ADMUR	ADVR6	ADVR5	ADVR4	ADVR3	ADVR2	ADVR1	ADVR0

Bit 15 — ADMUL

Left ADC Mute. This bit is used to mute the input to the left channel ADC volume control. The user can set this bit to mute the ADC while retaining the previous gain setting in ADVL[6:0], so that the PGA returns to the previous gain setting when ADMUL is cleared. When the ADMUL bit is set, the left ADC PGA soft-steps down to its lowest level, then mutes. This procedure is used to reduce any audible artifacts (*pops or clicks*) during the mute operation. This soft-stepping process is reversed when the ADMUL bit is cleared (unmute).

Table 38. Left ADC Mute

ADMUL	Description
0	Left channel ADC is active.
1	Left channel ADC is mute. (default)

Bits [14:8] — ADVL6- ADVL0

Left ADC Volume Control. These 7 bits control the gain setting of the left channel ADC volume control. This volume control can be programmed from -40 dB to 20 dB in 0.5-dB steps. Full volume (+20 dB) corresponds to a setting of 7Fh. Unity gain (0 dB) corresponds to 57h. Full attenuation (-40 dB) corresponds to 07h. Any value lower than 07h engages the mute function described above. Volume control changes are always soft-stepped, as described above. The default volume setting is 0 dB.

ADVL[6:0] = 1010111 (087d) = 0 dB (default)

ADVL[6:0] = 1111111 (127d) = +20 dB (Max)

ADVL[6:0] = 0000111 (007d) = -40 dB (Min)

ADVL[6:0] = 0d-6d = mute

Bit 7 — ADMUR

Right ADC Mute. This bit is used to mute the input to the right channel ADC. The user can set this bit to mute the ADC while retaining the previous gain setting in ADVR[6:0], so that the PGA returns to the previous gain setting when ADMUR is cleared. When the ADMUR bit is set, the right ADC PGA soft-steps down to its lowest level, then mutes. This procedure is used to reduce any audible artifacts (*pops or clicks*) during the mute operation. This soft-stepping process is reversed when the ADMUR bit is cleared (unmute).

Table 39. Right ADC Mute

ADMUR	Description
0	Right channel ADC is active.
1	Right channel ADC is mute. (default)

Bits [6:0] — ADVR6- ADVR0

Right ADC Volume Control. These 7 bits control the gain setting of the right channel ADC volume control PGA. This volume control can be programmed from -40 dB to 20 dB in 0.5-dB steps. Full volume (20 dB) corresponds to a setting of 7Fh. Unity gain (0 dB) corresponds to 57h. Full attenuation (-40 dB) corresponds to 07h. Any value lower than 07h engages the mute function described above. Volume control changes are always soft-stepped, as described above. The default volume setting is 0 dB.

ADVR[6:0] = 1010111 (087d) = 0 dB (default)

ADVR[6:0] = 1111111 (127d) = +20 dB (Max)

ADVR[6:0] = 0000111 (007d) = -40 dB (Min)

ADVR[6:0] = 0d-6d = mute

DAC VOLUME CONTROL REGISTER (Page 02, Address 02h)

The DAC volume control register controls the independent digital gain controls on the left and right channel audio DAC's of the TSC2301. The gain of the DACs can be adjusted from -63.5 dB to 0 dB in 0.5-dB steps. The DAC inputs can also be muted, so that all zeroes are sent to the DAC interpolation filters.

The DAC volume control register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
DAMUL	DAVL6	DAVL5	DAVL4	DAVL3	DAVL2	DAVL1	DAVL0	DAMUR	DAVR6	DAVR5	DAVR4	DAVR3	DAVR2	DAVR1	DAVR0

Bit 15 — DAMUL

Left DAC Mute. This bit is used to mute the input to the left channel DAC. The user can set this bit to mute the DAC while retaining the previous gain setting in DAVL[6:0], so that the gain control returns to the previous gain setting when DAMUL is cleared. When the DAMUL bit is set, the left DAC digital gain control soft-steps down to its lowest level, then all zeroes are sent to the interpolation filter of this DAC. This procedure is used to reduce any audible artifacts (*pops or clicks*) of the mute procedure. This soft-stepping process is reversed when the DAMUL bit is cleared (unmute).

Table 40. Left DAC Mute

DAMUL	Description
0	Left channel DAC is active.
1	Left channel DAC is mute. (default)

Bits [14:8] — DAVL6- DAVL0

Left DAC Volume Control. These 7 bits control the gain setting of the left channel DAC volume control PGA. This volume control can be programmed from -63.5 dB to 0dB in 0.5-dB steps. Full volume (0dB) corresponds to a setting of 7Fh. Full attenuation (-63.5 dB) corresponds to 00h. The default volume setting is 0 dB.

DAVL[6:0] = 1111111 (127d) = 0 dB (default)

DAVL[6:0] = 0000000 (000d) = -63.5 dB (Min)

1LSB = 0.5 dB

Bit 7 — DAMUR

Right DAC Mute. This bit is used to mute the input to the right channel DAC. The user can set this bit to mute the DAC while retaining the previous gain setting in DAVR[6:0], so that the gain control returns to the previous gain setting when DAMUR is cleared. When the DAMUR bit is set, the left DAC digital gain control soft-steps down to its lowest level, then all zeroes are sent to the interpolation filter of this DAC. This procedure is used to reduce any audible artifacts (*pops or clicks*) of the mute procedure. This soft-stepping process is reversed when the DAMUR bit is cleared (unmute).

Table 41. Right DAC Mute

DAMUR	Description
0	Right channel DAC is active.
1	Right channel DAC is mute. (default)

Bits [6:0] — DAVR6- DAVR0

Right DAC Volume Control. These 7 bits control the gain setting of the right channel DAC volume control. This volume control can be programmed from -63.5 dB to 0 dB in 0.5-dB steps. Full volume (0 dB) corresponds to a setting of 7Fh. Full attenuation (-63.5 dB) corresponds to 00h. The default volume setting is 0 dB.

DAVR[6:0] = 1111111 (127d) = 0 dB (default)

DAVR[6:0] = 0000000 (000d) = -63.5 dB (Min)

1LSB = 0.5 dB

ANALOG AUDIO BYPASS PATH VOLUME CONTROL REGISTER (Page 02, Address 03h)

The bypass path volume control register controls the independent programmable gain amplifiers (PGA's) on the left and right channel analog audio bypass paths of the TSC2301. These bypass paths direct the line inputs directly to the line and headphone outputs entirely in the analog domain, with no A/D or D/A conversion. This feature can be used for playback of an external analog source, such as an FM stereo tuner through the TSC2301's headphone amplifier. The gain of these PGA's can be adjusted from -35.5 dB to 12 dB in 0.5 dB steps. The bypass paths can also be muted, so that no signal is transmitted.

The bypass path volume control register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
BPMUL	BPVL6	BPVL5	BPVL4	BPVL3	BPVL2	BPVL1	BPVL0	BPMUR	BPVR6	BPVR5	BPVR4	BPVR3	BPVR2	BPVR1	BPVR0

Bit 15 — BPMUL

Left Channel Audio Bypass Mute. This bit is used to mute the bypass path from the left channel line input (LLINEIN) to the left channel line and headphone outputs (VOUTL and HPL). The user can set this bit to mute the bypass path while retaining the previous gain setting in BPVL[6:0], so that the PGA returns to the previous gain setting when BPMUL is cleared. When the BPMUL bit is set, the PGA soft-steps down to its lowest level, then the bypass path is muted. This procedure is used to reduce any audible artifacts (*pops or clicks*) during the mute operation. This soft-stepping process is reversed when the BPMUL bit is cleared (unmute).

Table 42. Left Channel Audio Bypass Mute

BPMUL	Description
0	Left channel audio bypass path is active.
1	Left channel audio bypass path is mute. (default)

Bits [14:8] — BPVL6- BPVL0

Left Channel Audio Bypass Path Volume Control. These 7 bits control the gain setting of the left channel bypass path volume control PGA. This volume control can be programmed from -35.5 dB to 12 dB in 0.5 dB steps. Full volume (+12 dB) corresponds to a setting of 7Fh. Unity gain (0 dB) corresponds to 67h. Full attenuation (-35.5 dB) corresponds to 20h. Any value lower than 20h engages the mute function described above. The default volume setting is 0 dB.

BPVL[6:0] = 1100111 (103d) = 0 dB (default)

BPVL[6:0] = 1111111 (127d) = 12 dB (Max)

BPVL[6:0] = 0100000 (032d) = -35.5 dB (Min)

BPVL[6:0] = 0d-31d = mute

Bit 7 — BPMUR

Right Channel Audio Bypass Mute. This bit is used to mute the bypass path from the right channel line input (RLINEIN) to the right channel line and headphone outputs (VOUTR and HPR). The user can set this bit to mute the bypass path while retaining the previous gain setting in BPVR[6:0], so that the PGA returns to the previous gain setting when BPMUR is cleared. When the BPMUR bit is set, the PGA soft-steps down to its lowest level, then the bypass path is muted. This procedure is used to reduce any audible artifacts (*pops or clicks*) during the mute operation. This soft-stepping process is reversed when the BPMUR bit is cleared (unmute).

Table 43. Right Channel Audio Bypass Mute

BPMUR	Description
0	Right channel audio bypass path is active.
1	Right channel audio bypass path is mute. (default)

Bits [6:0] — BPVR6- BPVR0

Right Channel Audio Bypass Path Volume Control. These 7 bits control the gain setting of the right channel bypass path volume control PGA. This volume control can be programmed from -35.5 dB to +12 dB in 0.5-dB steps. Full volume (+12 dB) corresponds to a setting of 7Fh. Unity gain (0 dB) corresponds to 67h. Full attenuation (-35.5 dB) corresponds to 20h. Any value lower than 20h engages the mute function described above. The default volume setting is 0 dB.

BPVR[6:0] = 1100111 (103d) = 0 dB (default)

BPVR[6:0] = 1111111 (127d) = +12 dB (Max)

BPVR[6:0] = 0100000 (032d) = -35.5 dB (Min)

BPVR[6:0] = 0d-31d = mute

KEYCLICK CONTROL REGISTER (Page 2, Address 04H)

The Keyclick Control Register of the TSC2301 controls the setup of the internal keyclick sound generator. This register is used to initiate and set the frequency, amplitude, and duration of the internally generated keyclick sound. This register also controls the input to the differential mono output, and the soft-stepping function of the TSC2301 volume controls.

The keyclick control register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
KEYST	KCAM 2	KCA M1	KCAM 0	RESV	KCFR 2	KCFR 1	KCFR 0	KCLN3	KCLN2	KCLN1	KCLN0	RESV	MONS	SSRT E	SSTE P

Bit 15 — KEYST

Keyclick Start. This bit initiates a keyclick sound.

Table 44. Keyclick Start

KEYST	Description
0	No keyclick sound (default)
1	Initiate a keyclick sound

Bits [14:12] — KCAM2-KCAM0

Keyclick Amplitude. These bits set the amplitude of the keyclick sound with eight amplitude levels provided.

KCAM[2:0] = 100 = Medium amplitude (default)

KCAM[2:0] = 111 = Maximum amplitude

KCAM[2:0] = 000 = Minimum amplitude

Bit 11 — RESERVED

This bit is reserved, and should be written to 0. If read, it reads back as 0.

Bits [10:8] — KCFR2-KCFR0

Keyclick Frequency. These bits set the frequency of the keyclick sound (frequencies are approximate).

Table 45. Keyclick Frequency

KCFR2	KCFR1	KCFR0	Keyclick Tone Frequency
0	0	0	62.5 Hz
0	0	1	125 Hz
0	1	0	250 Hz
0	1	1	500 Hz
1	0	0	1 k Hz (default)
1	0	1	2 k Hz
1	1	0	4 k Hz
1	1	1	8 k Hz

Bits [7:4] — KCLN3-KCLN0

Keyclick Length. These bits set the approximate duration of the keyclick sound, 16 settings for duration are provided. The formula for the number of periods heard is:

$$N_{periods} = (KCLN + 1) \times 2 \qquad (14)$$

KCLN[3:0] = 0000 = 2 periods of the keyclick sound (min)

KCLN[3:0] = 0001 = 4 periods of the keyclick sound (default)

KCLN[3:0] = 0010 = 6 periods of the keyclick sound

KCLN[3:0] = 0011 = 8 periods of the keyclick sound

KCLN[3:0] = 1111 = 32 periods of the keyclick sound (max)

Bit 3 — RESERVED

This bit is reserved, and should be written as 0. If read, it is read back as 0.

Bit 2 — MONS

Mono Select. This bit determines the position of the mono multiplexer. This multiplexer allows either the left channel ADC Input or the mono mix of the stereo line outputs to be played out the differential mono output (MONO+/-).

Table 46. Mono Select

MONS	Description
0	Mono output comes from left ADC input (default).
1	Mono output comes from mono mix of line outputs.

Bit 1 — SSRTE

Volume Soft-stepping Rate Select. This bit selects the speed of the soft-stepping function of the TSC2301 volume controls. At normal speed, the actual volume is updated approximately once every 20 µs. At half speed, the actual volume is updated approximately once every 40 µs.

Table 47. Volume Soft-Stepping Rate Select

SSRTE	Description
0	Normal step rate used (default).
1	Half step rate used.

Bit 0 — SSTEP

Soft-step Flag. This read-only bit indicates that the TSC2301 volume control soft-stepping is completed.

Table 48. Soft-Step Flag

SSTEP	Description
0	Soft-stepping is not complete.
1	Soft-stepping is complete (default).

AUDIO POWER CONTROL REGISTER (Page 2, Address 05H)

The audio power / miscellaneous control register of the TSC2301 controls the powering down of various audio blocks of the TSC2301. The default state of the TSC2301 has all audio blocks powered down. Before using any of the audio blocks, they must be powered up by writing to this register. This register also controls the crystal oscillator clock and buffer, the bass-boost filter, and the de-emphasis filter.

The audio power / miscellaneous control register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
APD	AVPD	ABPD	HAPD	MOPD	DAPD	ADPDL	ADPDR	PDSTS	MIBPD	OSCC	BCKC	SMPD	OTSYN	BASS	DEEMP

For bits 15 through 8 of this register, writing a 1 to a selected bit powers down the affected section, writing a 0 powers up the section.

Bit 15 — APD

Audio Power Down. This bit powers down the entire audio section if set, regardless of the settings of the other bits in this register. When this bit is cleared, the individual sections of the audio codec still need to be powered up individually. The settings of the other bits in the register are retained when this bit is set and cleared. The default is 1 (powered down).

Bit 14 — AVPD

Audio VCM Power Down. If this is set to 1, the VCM powers up whenever it is needed (such as when the audio ADC, DAC, or bypass path is enabled) and powers down when no longer needed. If this bit is set to 0, after an audio component is powered up and causes VCM to power up, it no longer powers down, even if all audio components are powered down. This is intended to avoid the 500 µs delay needed for VCM to power up slowly. The default is 1 (powered down).

Bit 13 — ABPD

Audio Bypass Path Power Down. This is used to power up (set to 0) or power down (set to 1) the audio bypass path. The default is 1 (powered down).

Bits 12 — HAPD

Headphone Amplifier Power Down. This is used to power up (set to 0) or power down (set to 1) the headphone amplifier. The default is 1 (powered down).

Bit 11 — MOPD

Mono Driver Power Down. This is used to power up (set to 0) or power down (set to 1) the mono output driver. If only playback of the line or Mic inputs through the mono output is needed, the user need only power up the mono section, and not the DAC or ADCs. The line inputs, Mic preamp, left channel ADC multiplexer and left channel volume control all power up if the mono output is powered up. The default is 1 (powered down).

Bit 10 — DAPD

DAC Power Down. This is used to power up (set to 0) or power down (set to 1) the entire stereo DAC. The default is 1 (powered down).

Bit 9 — ADPDL

Left Channel ADC Power Down. This is used to power up (set to 0) or power down (set to 1) the entire left channel ADC. The line inputs, Mic preamp, left channel ADC multiplexer and left channel volume control all automatically power up when the left channel ADC is powered up. The default is 1 (powered down).

Bit 8 — ADPDR

Right Channel ADC Power Down. This is used to power up (set to 0) or power down (set to 1) the entire right channel ADC. The line inputs, Mic preamp, right channel ADC multiplexer and right channel volume control all automatically power up when the right channel ADC is powered up. The default is 1 (powered down).

Bit 7 — PDSTS

Power Up/Down Done. This read-only bit indicates that all power-up or power-down processes requested are completed.

Table 49. Power Up/Down Flag

PDSTS	Description
0	Power up/down is not complete.
1	Power up/down is complete (default).

Bit 6 — MIBPD

Microphone Bias Power Down. This is used to power up (set to 0) or power down (set to 1) the microphone bias output.

Table 50. Microphone Bias Power Down

OSCC	Description
0	Microphone bias is on.
1	Microphone bias is off (default).

Bit 5 — OSCC

Crystal Oscillator Control. This bit turns ON/OFF the crystal Oscillator.

Table 51. Crystal Oscillator Control

OSCC	Description
0	Crystal oscillator is off (default).
1	Crystal oscillator is on.

Bit 4 — BCKC

Oscillator Clock Buffer Control. This bit turns ON/OFF the output clock buffer.

Table 52. Oscillator Clock Buffer Control

BCKC	Description
0	The output clock buffer is off (default).
1	The output clock buffer is on.

Bit 3 — SMPD

Synchronization Monitor Power Down. This bit turns ON/OFF the I^2S bus sync monitor.

Table 53. Synchronization Monitor Power Down

SMPD	Description
0	The I^2S bus sync monitor is on (default).
1	The I^2S bus sync monitor is off.

Bit 2 — OTSYN

I^2S Out Of Sync. This read-only *sticky bit* reflects the sync status of the I^2S bus. It always resets to zero after being read.

Table 54. I^2S Out of Sync

OTSYN	Description
0	The I^2S bus is in sync (default).
1	The I^2S bus is out of sync.

Bit 1 — BASS

Digital-effects filter control. This bit turns ON/OFF the digital-effects filter. If the digital-effects filter is off, the signal passes through with no filtering performed.

Table 55. Digital-Effects Filter Control

BASS	Description
0	The digital-effects filter is off (default).
1	The digital-effects filter is on.

Bit 0 — DEEMP

De-emphasis control. This bit turns ON/OFF the de-emphasis function.

Table 56. De-Emphasis Control

DEEMP	Description
0	De-emphasis is off (default).
1	De-emphasis is on.

GPIO CONTROL REGISTER (Page 02, Address 06h)

The GPIO control register controls the GPIO pins of the TSC2301. The direction of each GPIO pin can be set independently. For GPIOs configured as output pins, the data to be driven is written to this register. For GPIO's configured as inputs, the input data can be read from this register. This register also contains a bit, SDAVB which mirrors the state of the DAVB output line.

The GPIO Control Register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
RESV	RESV	IO5	IO 4	IO 3	IO 2	IO 1	IO 0	RESV	RESV	GPIO5	GPIO4	GPIO3	GPIO2	GPIO 1	GPIO 0

Bits 15,14 — RESERVED

These bits are reserved and should be written to 0. If read, they read back as 0.

Bits [13:8] — IO5- IO0

GPIO Directional Control. These 6 bits control the direction of the TSC2301s six GPIO pins. When one of these bits is set to one, the corresponding GPIO pin is configured as an output. When one of these bits is set to zero, the corresponding GPIO pin is configured as an input. The default setting of these bits is zero (all inputs).

Bits 7,6 — RESERVED

These bits are reserved, and should be written to 0. If read, they read back as 0.

Bits [5:0] — GPIO5- GPIO0

GPIO Data. These bits control the data on the GPIO pins. When a GPIO pin is configured as an output, the data written to one of these bits is driven on the corresponding GPIO pin. When a GPIO pin is configured as an input, the data input on the GPIO pin is returned to the corresponding register bit, and can be read by the host processor.

DAC BASS-BOOST FILTER COEFFICIENT REGISTERS (Page 02, Addresses 07h-1Ah)

The DAC bass-boost coefficient registers implement the transfer function described. The coefficients are represented by 16-bit twos complement integers with values ranging from -32768 to 32767.

The DAC bass-boost coefficient registers are formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 57. DAC Bass-Boost Coefficient Registers

Address	DAC Channel	Coefficient	Default
07h	Left	N0	6BE2
08h	Left	N1	9667
09h	Left	N2	675D
0Ah	Left	N3	6BE2
0Bh	Left	N4	9667
0Ch	Left	N5	675D
0Dh	Left	D1	7D82
0Eh	Left	D2	84EF
0Fh	Left	D4	7D82
10h	Left	D5	84EF
11h	Right	N0	6BE2
12h	Right	N1	9667
13h	Right	N2	675D
14h	Right	N3	6BE2
15h	Right	N4	9667
16h	Right	N5	675D
17h	Right	D1	7D82
18h	Right	D2	84EF
19h	Right	D4	7D82
1Ah	Right	D5	84EF

AUDIO CLOCK CONFIGURATION REGISTER (Page 02, Address 1Bh)

This register allows the user to use the output of the crystal oscillator as MCLK, and receive the PLL output on the $\overline{\text{PENIRQ}}$ pin.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	X	X	X	X	X	X	X	X	X	X	X	PLPN	COMK	X	X

Bits [15:4] — RESERVED

These bits are reserved, and should be written to 040h. If read, they read back as 040h.

Bits 3 — PLPN

Output PLL on the $\overline{\text{PENIRQ}}$ pin. This bit allows the user to receive the output of the audio codec internal PLL. This bit is provided so the host processor can use the output of the PLL, to generate its I^2S signals in sync with an external MCLK or crystal oscillator. Writing a 1 to this bit connects the output of the PLL to the $\overline{\text{PENIRQ}}$ pin. Otherwise, the $\overline{\text{PENIRQ}}$ pin operates as normal. The user must take care in using this function, as $\overline{\text{PENIRQ}}$ signals are overridden.

Table 58. Output PLL on $\overline{\text{PENIRQ}}$ Pin

DEEMP	Description
0	$\overline{\text{PENIRQ}}$ operates as normal (default).
1	Output PLL on $\overline{\text{PENIRQ}}$.

Bits 2 — COMK

Crystal Oscillator as MCLK. This bit allows the user to use the output of the internal crystal oscillator as the MCLK for the audio codec. In this case, the MLCK pin must be grounded. In this case, the output of the crystal oscillator replaces MCLK in all functions.

Table 59. Crystal Oscillator as MCLK

DEEMP	Description
0	Crystal oscillator and MCLK operates as normal (default).
1	Use crystal oscillator output as MCLK.

Bits [1:0] — RESERVED

These bits are reserved, and must be written to 0. If read, they read back as 0.

LAYOUT

The following layout suggestions provide optimum performance from the TSC2301. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly *clean* power and grounds because most of the internal components are very low power. This situation means less bypassing for the converter power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care must be taken with the physical layout of the TSC2301 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n-bit* SAR converter, there are n *windows* in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the internal conversion clock. The touch screen circuitry, as well as the audio headphone amplifiers, uses the HPVDD/HPGND supplies for its power, and any noise on this supply may adversely affect performance in these blocks.

As described earlier, the audio common-mode voltage VCM is derived directly through an internal resistor divider between AVDD and AGND. Therefore, noise that couples onto AVDD/AGND is translated onto VCM and can adversely impact audio performance. The reference pins for the audio data converters, VREF+/VREF-, should also be kept as clean and noise-free as possible, since noise here affects audio DAC/ADC quality. Decoupling capacitors are recommended between VREF+ and VREF-, in addition to a series resistance between VREF+ and the source of the voltage (such as connecting to the source providing AVDD).

With this in mind, power to the TSC2301 must be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible on each supply pin to its respective ground pin. A 1-µF to 10-µF capacitor may also be needed if the impedance of the connection between a supply and the power supply is high.

A bypass capacitor on the SAR Vref pin may not be absolutely necessary because this reference is buffered by an internal op amp, but a 0.1uF bypass capacitor may reduce noise on this reference. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2301 SAR converter architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high frequency noise can be filtered out, voltage variation due to line frequency (50 Hz or 60 Hz) can be difficult to remove.

The HPGND pin must be connected to a clean ground point. In many cases, this is the analog ground for the SAR converter. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care must be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (e.g., applications that require a back-lit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause *flickering* of the converted data. Several things can be done to reduce this error, such as utilizing a touch screen with a bottom-side metal layer connected to ground. This couples the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y-, X+, and X- to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires longer panel voltage stabilization times, as well as increased precharge and sense times for the touch screen control circuitry of the TSC2301.

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
TSC2301IGQZ	ACTIVE	BGA MI CROSTA R JUNI OR	GQZ	120	250	TBD	SNPB	Level-2A-235C-4 WKS
TSC2301IGQZR	ACTIVE	BGA MI CROSTA R JUNI OR	GQZ	120	2500	TBD	SNPB	Level-2A-235C-4 WKS
TSC2301IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TSC2301IPAGG4	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TSC2301IPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TSC2301IPAGRG4	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TSC2301IZQZ	ACTIVE	BGA MI CROSTA R JUNI OR	ZQZ	120	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
TSC2301IZQZR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQZ	120	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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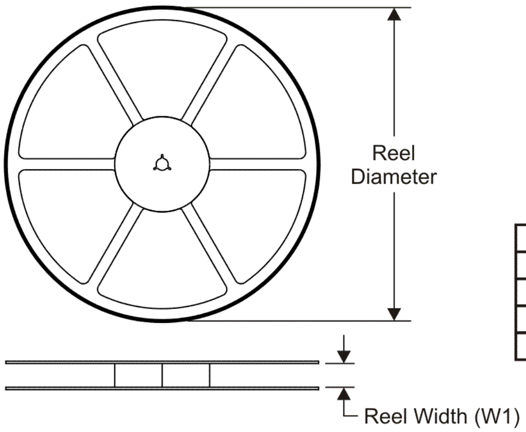
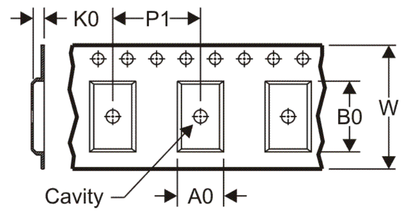
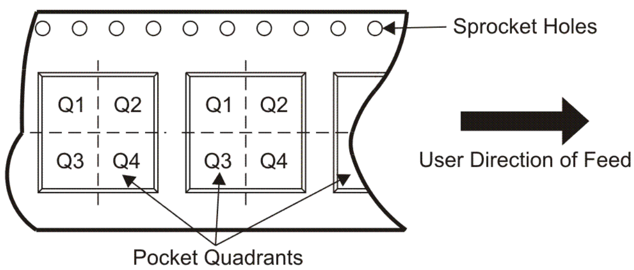
TAPE AND REEL INFORMATION





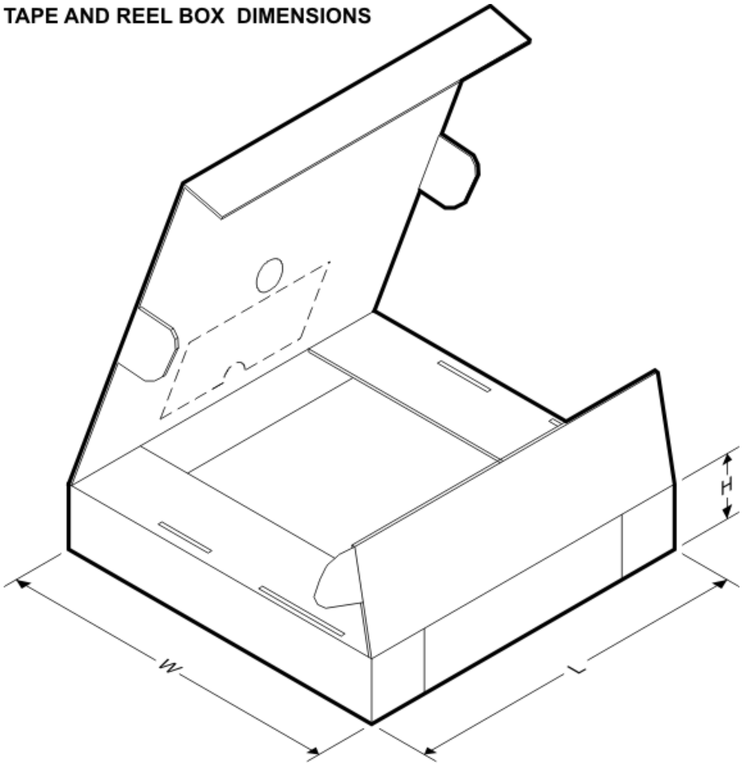
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2301IGQZR	BGA MICROSTAR JUNIOR	GQZ	120	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
TSC2301IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
TSC2301IZQZR	BGA MICROSTAR JUNIOR	ZQZ	120	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

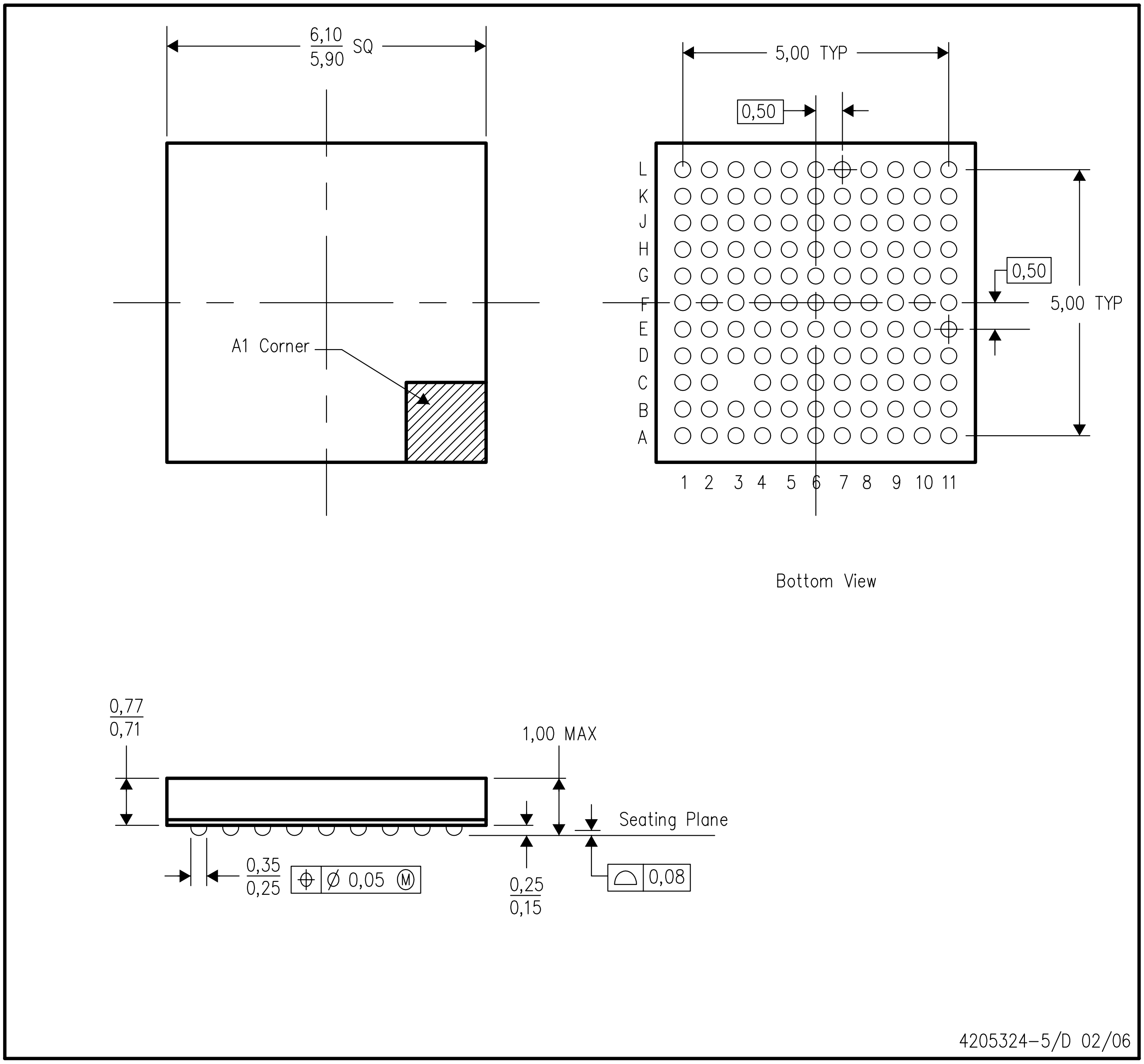
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

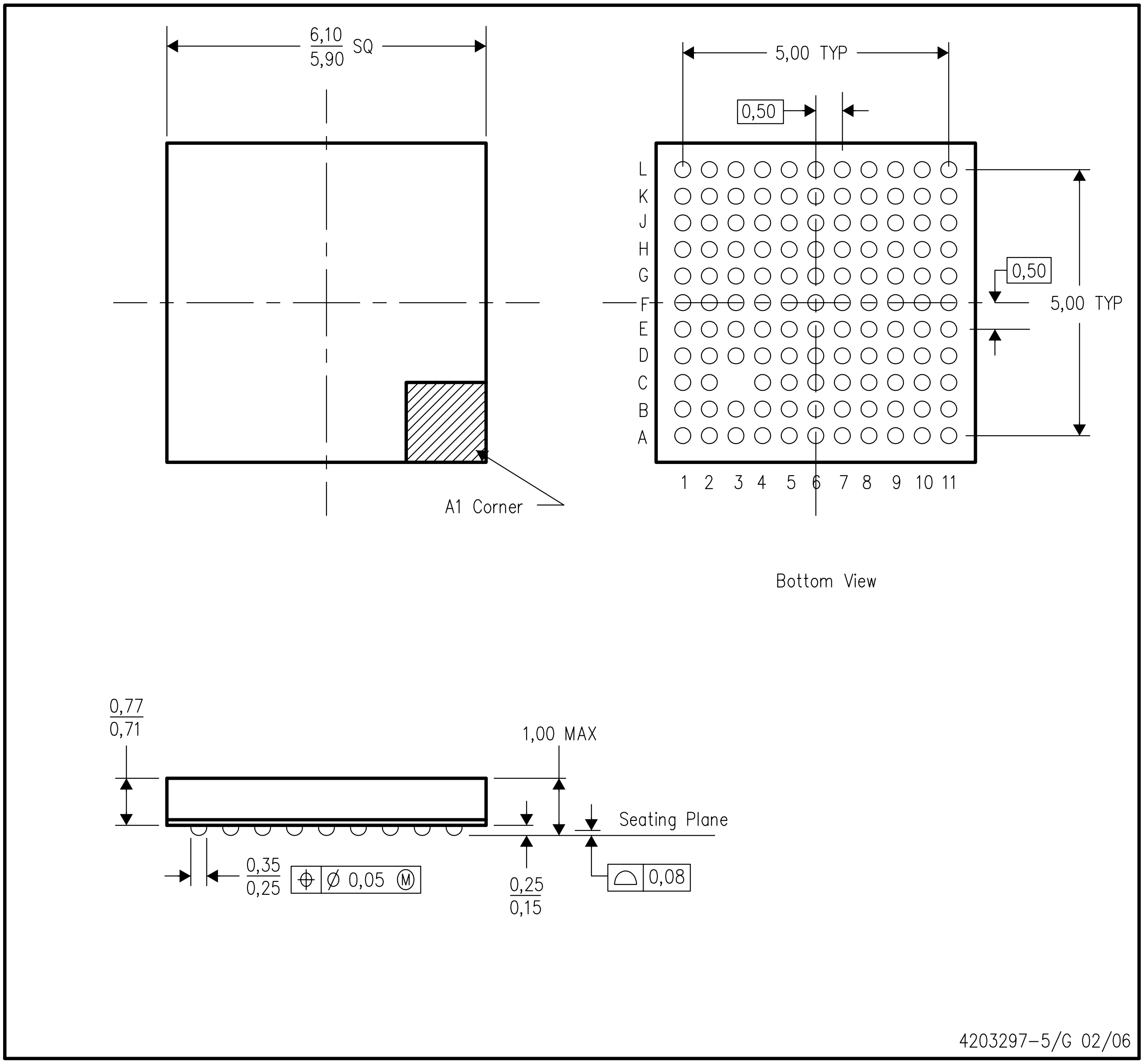
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2301IGQZR	BGA MICROSTAR JUNIOR	GQZ	120	2500	333.2	345.9	28.6
TSC2301IPAGR	TQFP	PAG	64	1500	346.0	346.0	41.0
TSC2301IZQZR	BGA MICROSTAR JUNIOR	ZQZ	120	2500	333.2	345.9	28.6

ZQZ (S-PBGA-N120) PLASTIC BALL GRID ARRAY



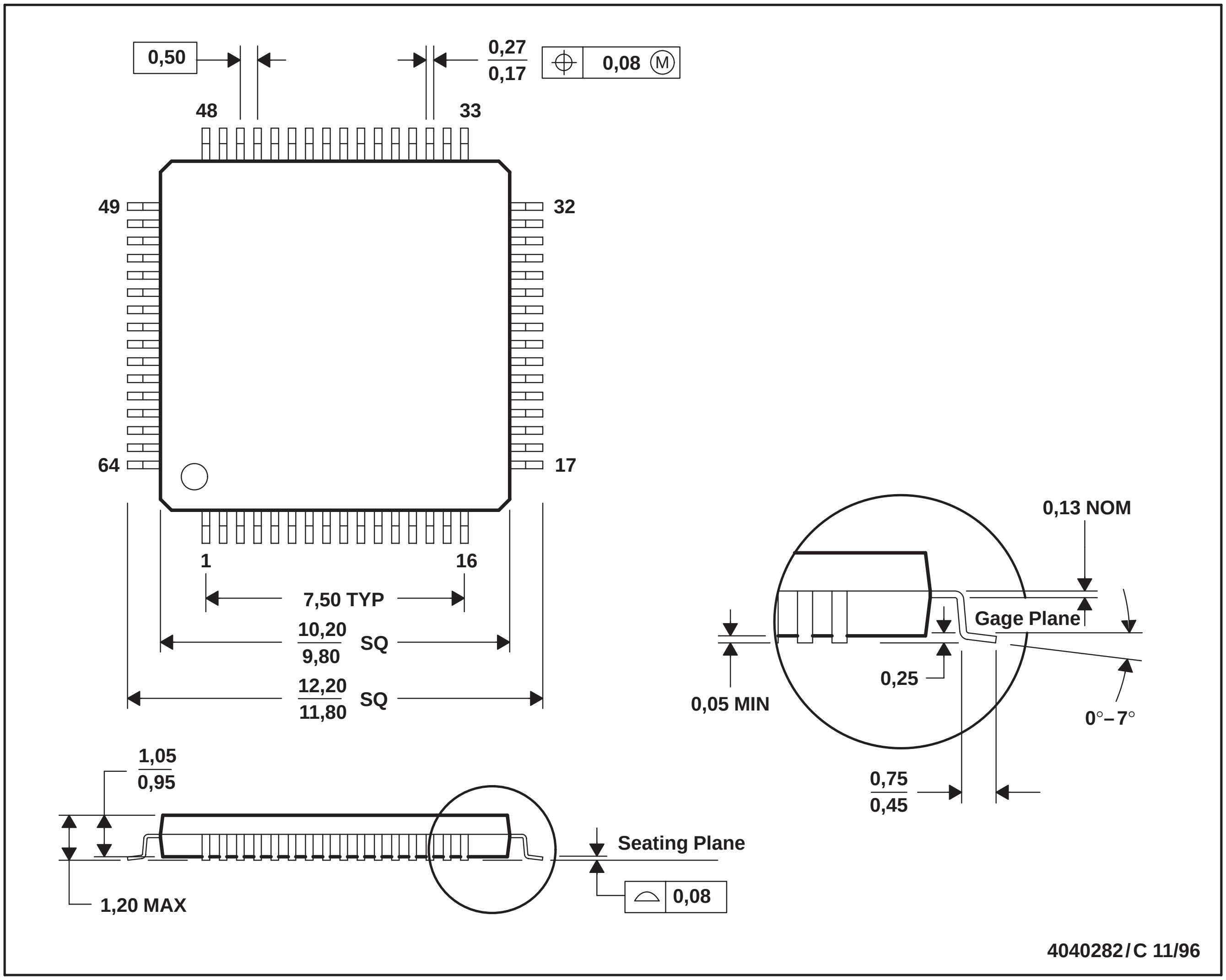
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-225
D. This package is lead-free.

GQZ (S–PBGA–N120) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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