TEXAS INSTRUMENTS

LDO Linear Regulator Design Using the Universal SOT23 EVM

User's Guide

August 1999

Mixed Signal Products

SLVU019

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Preface

Read This First

About This Manual

This user's guide describes techniques for designing low dropout voltage linear regulators (LDO) using TI's SLVP125 evaluation modules (EVM) and TPS 76933 LDOs.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 Introduction
- Chapter 2 EVM Adjustments and Test Points
- Chapter 3 Circuit Design
- Chapter 4 Test Results

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

- TPS760xx, TPS761xx, TPS763xx, TPS764xx, TPS769xx, TPS770xx data sheets (literature numbers SLVS144B, SLVS178A, SLVS181D, SLVS180A, SLVS203B, SLVS210B)

Contents

Figures

Tables

Chapter 1

Introduction

This user's guide describes techniques for designing low dropout (LDO) voltage linear regulators using TI's SLVP125 evaluation module (EVM) and TPS76933 LDO. LDOs provide ideal power supplies for rapidly transitioning DSP loads such as the Texas Instruments TMS320C54x and similar processors, and fast memory. Low quiescent current and very low dropout voltage compared to standard LDOs makes the TPS76933 particularly suitable in battery applications requiring extended lifetime and low cost.

Low noise power supplies, fast transient response, improved efficiency, low component count, and easy design make LDOs popular in solutions where switched converters are too noisy and standard linear regulators are too inefficient.

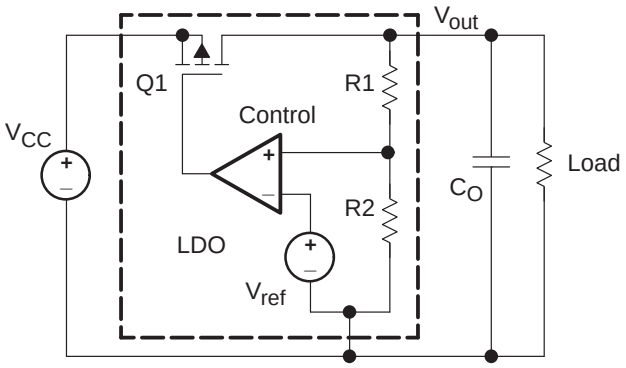
Topic **Page**

1.1 Low Dropout Voltage Linear Regulator Circuit Operation

In the low dropout voltage linear regulator topology, a PMOS transistor acts as a pass element that reduces the normal 1.5-V to 2.5-V collector-to-emitter drop to about 0.3 V or less. This improvement results in lower power dissipation and higher efficiency when compared to other regulator designs.

The basic LDO regulator circuit includes the LDO and an output capacitor for stabilization. Figure 1–1 shows the circuit of a typical LDO application.

Figure 1–1. Typical LDO Application



In the LDO application shown in Figure 1–1, the LDO regulates the output voltage V_{out}.

If V_{out} falls below the regulation level, the controller increases the V_{GS} differential and the PMOS conducts more current, resulting in an increase of V_{out}. If V_{out} exceeds the regulation level, the controller decreases the V_{GS} differential and the PMOS conducts less current, resulting in a decrease of V_{out}. The PMOS pass element acts like an adjustable resistor. The more negative the gate becomes versus the source, the less the source-drain resistance becomes, resulting in higher current flow through the PMOS.

1.2 Design Strategy

The TI SLVP125 EVM provides a circuit to simultaneously compare the performance of two LDOs in a SOT23 package. The EVM provides proven, demonstrated reference designs and test modes to aid in choosing and evaluating LDOs. A programmable high speed transient generator generates either line or load transients. The transient slew rate, and the impact of the transients on the load/line are adjustable. A 10x amplifying operational amplifier (op amp) makes measurements of the dropout voltages easier and more accurate. To avoid influencing each other, each LDO can be powered by its own power supply. Jumpers allow settings of minimum/maximum load as well as device-enable and transient impact functions. There is enough room on the EVM to evaluate different types of output capacitors including ESR behaviors. Many test points allow the measuring of input, output, and dropout voltage.

The EVM is shipped with a TPS76933 that provides a 3.3-V output voltage. The maximum output current is 100 mA. The 100 mA-output power level is a reasonable selection criteria for powering DSPs and battery-supplied applications such as mobile phones and laptop cards.

The TPS760xx, TPS761xx, TPS763xx, TPS764xx, TPS769xx, TPS770xx LDO family provides several output currents and voltages combined with options like very low noise or high accuracy.

Table 1–1 summarizes the LDO families and their features.

Table 1–1. Summary of LDO Families and Their Features

	TPS760xx	**TPS761xx**	**TPS763xx**	**TPS764xx**	**TPS769xx**	**TPS770xx**
Maximum input voltage range [V]	16 (PNP)		10 (PMOS)		13.5(PMOS)	
Maximum output current [mA]	50	100	150	150	100	50
Typical quiescent current [μA]	850	2600	85		17	
Typical dropout voltage [mV]	120	210	300		71	35
Typical output noise [μVrms]	190		140	30	190	
Accuracy over line, load, and temperature	3%				2%	
PSRR (at 1 kHz, C_O = 10 μF, T_J = 25°C)	60 dB					
Package	SOT23					
External cap	> 4.7 μF					
Available Voltage Option [V]	3, 3.2, 3.3, 3.8, and 5		1.6, 1.8, 2.5, 2.7, 2.8, 3, 3.3, 3.8, 5, and adj	2.5, 2.7, 2.8, 3, 3.3	1.2, 1.5, 1.8, 2.5, 2.7, 2.8, 3, 3.3, 5, and adj.	
Performance Advantage	Low dropout		Low quiescent current, low noise		Low dropout, ultra low quiescent current, high accuracy	

1.3 Schematic

Figure1–2 shows the SLVP125 EVM Universal LDO Tester (3.3 V output with TPS76933 as U1) schematic diagram.

Figure 1–2. SLVP125 EVM Universal LDO Tester Schematic Diagram

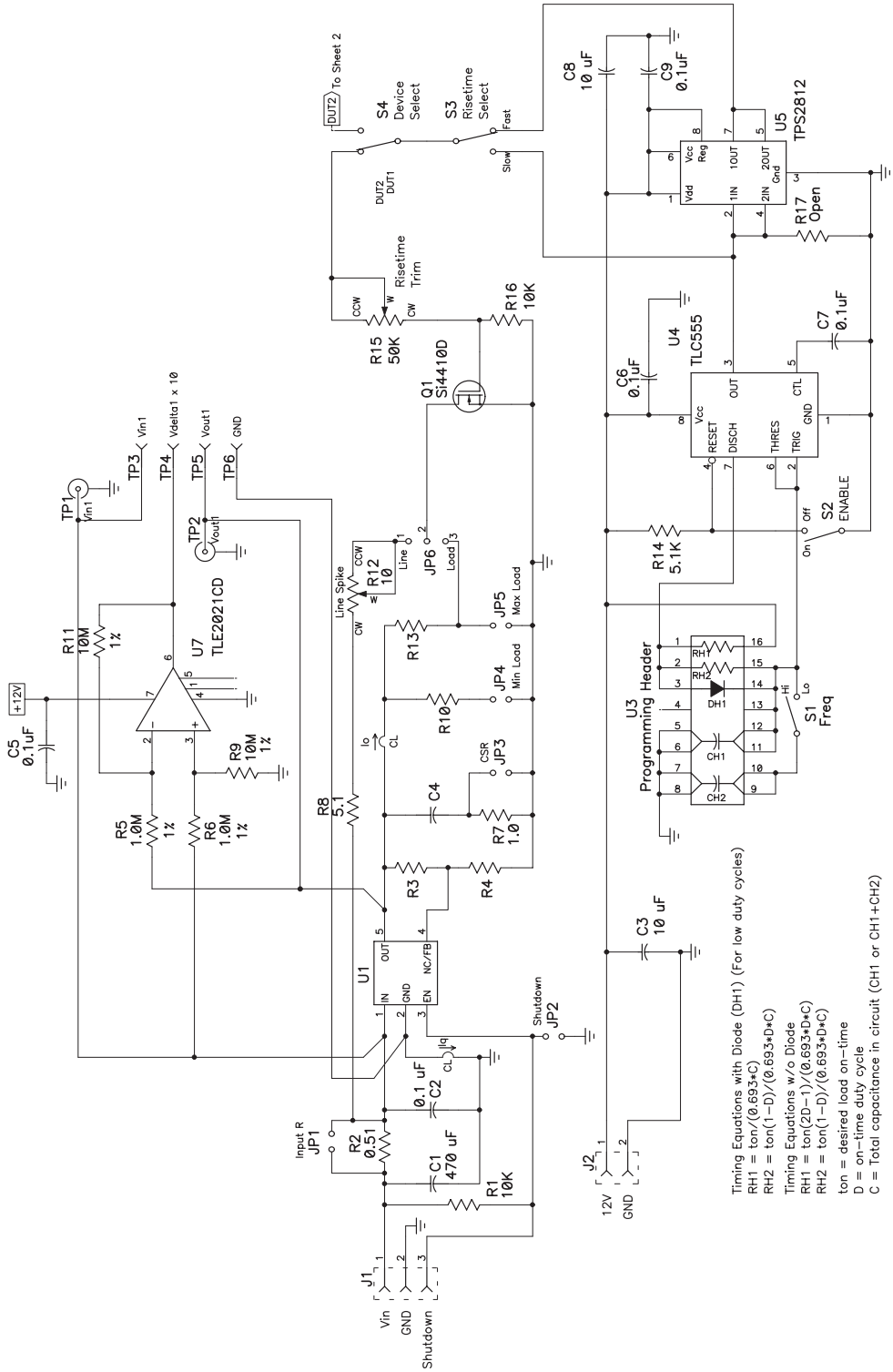
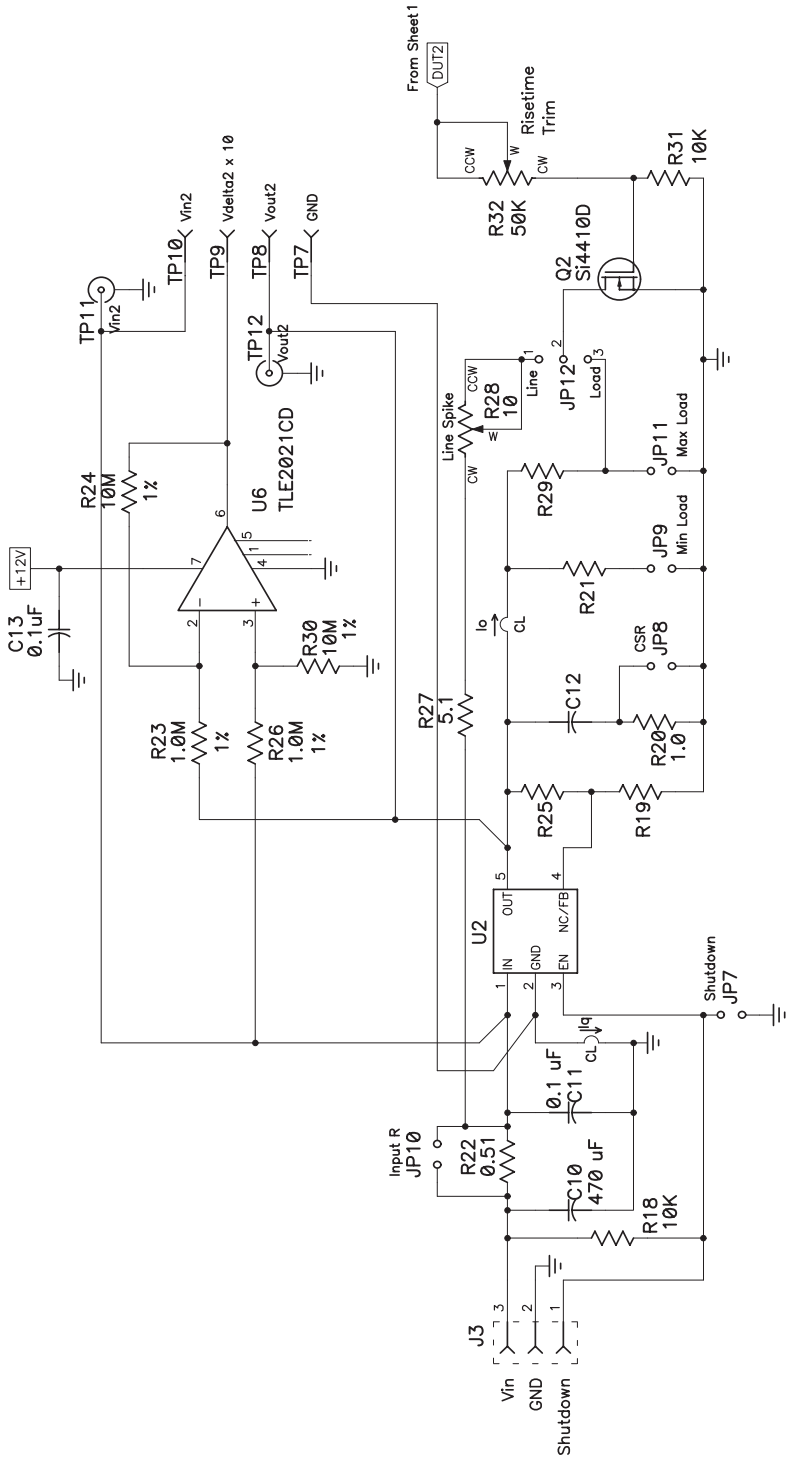


Figure 1–2. SLVP125 EVM Universal LDO Tester Schematic Diagram (Continued)



1.4 Bill of Materials

Table 1–2 lists materials required for the SLVP125 EVM.

Table 1–2. SLVP125 EVM Bill of Materials

Ref	PN	Description	Mfg	Size
C1	16SA470M	Capacitor, OS-Con, 470 µF, 16 V, 20-mΩ, 20%	Sanyo	G
C1 (Alt)	16SP470M	Capacitor, OS-Con, 470 µF, 16 V, 10-mΩ, 20%	Sanyo	G
C2	ECU-V1H104KBW	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%	Panasonic	1206
C3	GRM235Y5V106Z016A	Capacitor, ceramic, 10 µF, 16 V, Y5V, -20% +80%	muRata	1210
C4		Capacitor, user option		1210/1206
C5	ECU-V1H104KBW	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%	Panasonic	1206
C6	ECU-V1H104KBW	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%	Panasonic	1206
C7	ECU-V1H104KBW	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%	Panasonic	1206
C8	GRM235Y5V106Z016A	Capacitor, ceramic, 10 µF, 16 V, Y5V, –20% +80%	muRata	1210
C9	ECU-V1H104KBW	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%	Panasonic	1206
C10	16SA470M	Capacitor, OS-Con, 470 µF, 16 V, 20-mΩ, 20%	Sanyo	G
C10 (Alt)	16SP470M	Capacitor, OS-Con, 470 µF, 16 V, 10-mΩ, 20%	Sanyo	G
C11	ECU-V1H104KBW	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%	Panasonic	1206
C12		Capacitor, user option		1210/1206
C13	ECU-V1H104KBW	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%	Panasonic	1206
J1	ED1515-ND	Terminal block, 3-pin, 6 A, 3.5 mm	OST	3.5mm
J2	ED1514-ND	Terminal block, 2-pin, 6 A, 3.5 mm	OST	3.5mm
J3	ED1515-ND	Terminal block, 3-pin, 6 A, 3.5 mm	OST	3.5mm
JP1	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP2	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP3	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP4	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP5	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP6	PTC36SAAN	Header, single-row, straight, 3-pin, 0.100” x 25 mil	Sullins	0.1”
JP7	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP8	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP9	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP10	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP11	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
JP12	PTC36SAAN	Header, single-row, straight, 3-pin, 0.100” x 25 mil	Sullins	0.1”
Q1	Si4410DY	MOSFET, N-ch, 30-V, 10-A, 13-milliohm	Silconix	SO-8
Q2	Si4410DY	MOSFET, N-ch, 30-V, 10-A, 13-milliohm	Silconix	SO-8
R1	Std	Resistor, Chip, 10 kΩ, 1/8 W, 5%		1206
R2	Std	Resistor, Chip, 0.51 Ω, 1/8 W, 5%		1206
R3	Std	Resistor, Chip, user option, 1/8 W, 1%		1206
R4	Std	Resistor, Chip, user option, 1/8 W, 1%		1206
R5	Std	Resistor, Chip, 1.00 MΩ, 1/8 W, 1%		1206
R6	Std	Resistor, Chip, 1.00 MΩ, 1/8 W, 1%		1206
R7	Std	Resistor, Chip, 1.0 Ω, 1/8 W, 5%		1206
R8	Std	Resistor, Chip, 5.1 Ω, 1/8 W, 5%		1206
R9	Std	Resistor, Chip, 10.0 MΩ, 1/8 W, 1%		1206

Table 1–2. SLVP125 EVM Bill of Materials (Continued)

Ref	PN	Description	Mfg	Size
R10	Std	Resistor, Chip, user option, 1/8 W, 1%		1206
R11	Std	Resistor, chip, 10.0 MΩ, 1/8 W, 1%		1206
R12	72-T93YA-10	Trim Pot, cermet, 10 Ω vertical, top adjust, 1/2 W, 10%	Vishay	3x 0.1”
R13	Std	Resistor, chip, user option, 1/8-1 W, 1%		1206/2512
R14	Std	Resistor, CF, 5.1 KΩ, 1/8 W, 5%		1206
R15	72-T93YA-50K	Trim pot, cermet, 50 KΩ, vertical, top adjust, 1/2 W, 10%	Vishay	3x 0.1”
R16	Std	Resistor, chip, 10 kΩ, 1/8 W, 5%		1206
R17	Std	Resistor, chip, user option, 1/8 W, 5%		1206
R18	Std	Resistor, chip, 10 kΩ, 1/8 W, 5%		1206
R19	Std	Resistor, chip, user option, 1/8 W, 1%		1206
R20	Std	Resistor, chip, 1.0 Ω, 1/8 W, 5%		1206
R21	Std	Resistor, chip, user option, 1/8 W, 1%		1206
R22	Std	Resistor, chip, 0.51 Ω, 1/8 W, 5%		1206
R23	Std	Resistor, chip, 1.00 MΩ, 1/8 W, 1%		1206
R24	Std	Resistor, chip, 10.0 MΩ, 1/8 W, 1%		1206
R25	Std	Resistor, chip, user option, 1/8 W, 1%		1206
R26	Std	Resistor, chip, 1.00 MΩ, 1/8 W, 1%		1206
R27	Std	Resistor, chip, 5.1 Ω, 1/8 W, 5%		1206
R28	72-T93YA-10	Trim pot, cermet, 10 Ω, vertical, top adjust, 1/2 W, 10%	Vishay	3x 0.1”
R29	Std	Resistor, chip, user option, 1/8-1 W, 1%		1206/2512
R30	Std	Resistor, chip, 10.0 MΩ, 1/8 W, 1%		1206
R31	Std	Resistor, chip, 10 KΩ, 1/8 W, 5%		1206
R32	72-T93YA-50K	Trim pot, cermet, 50 KΩ, vertical, top adjust, 1/2 W, 10%	Vishay	3x 0.1”
S1	EG1218	Switch, 1P2T, slide, PC-mount	E-Switch	0.1”
S2	EG1218	Switch, 1P2T, slide, PC-mount	E-Switch	0.1”
S3	EG1218	Switch, 1P2T, slide, PC-mount	E-Switch	0.1”
S4	EG1218	Switch, 1P2T, slide, PC-mount	E-Switch	0.1”
TP1	131-4244-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	Tektronix	
TP2	131-4244-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	Tektronix	
TP3	240-345	Test point, red	Farnell	1 mm
TP4	240-345	Test point, red	Farnell	1 mm
TP5	240-345	Test point, red	Farnell	1 mm
TP6	240-333	Test point, black	Farnell	1 mm
TP7	240-333	Test point, black	Farnell	1 mm
TP8	240-345	Test point, red	Farnell	1 mm
TP9	240-345	Test point, red	Farnell	1 mm
TP10	240-345	Test point, red	Farnell	1 mm
TP11	131-4244-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	Tektronix	
TP12	131-4244-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	Tektronix	
U1		IC, LDO, DUT	TI	Various
U2		IC, LDO, DUT	TI	Various
U3	110-99-316-41-001	Socket, 16-pin, frequency programming	Mill-Max	DIP-16
U4	TLC555CD	IC, CMOS timer	TI	SO-8
U5	TPS2812D	IC, MOSFET driver, 2-Ch, Noninverting	TI	SO-8
U6	TLE2021CD	IC, Op Amp, single-supply, low offset	TI	SO-8
U7	TLE2021CD	IC, Op Amp, single-supply, low offset	TI	SO-8

1.5 Board Layout

Figures 1–3 through 1-6 show the board layout for the SLVP125 EVM.

Figure 1–3. Top Layer

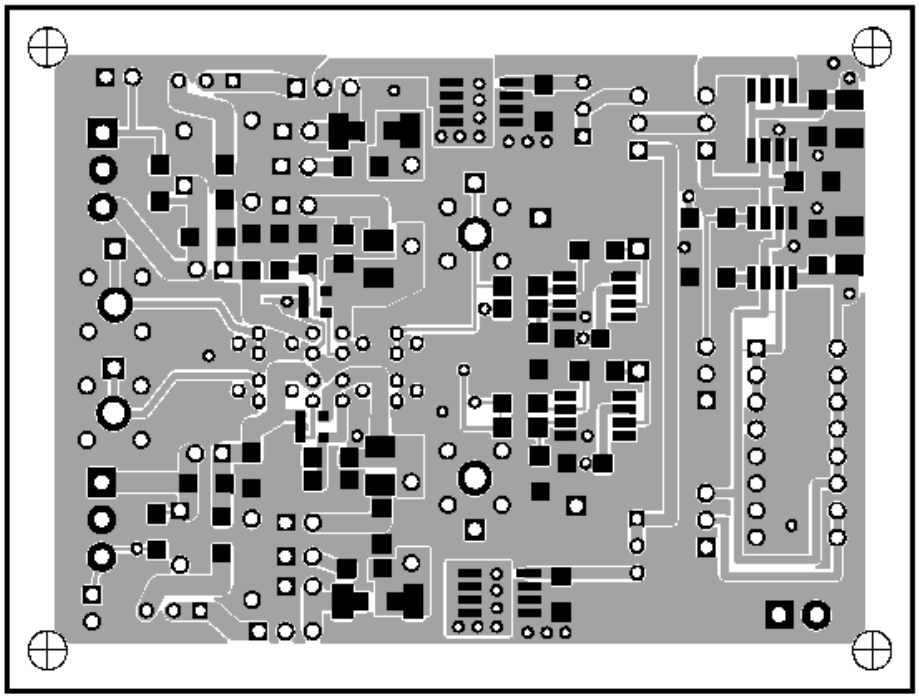


Figure 1–4. Bottom Layer (top view)

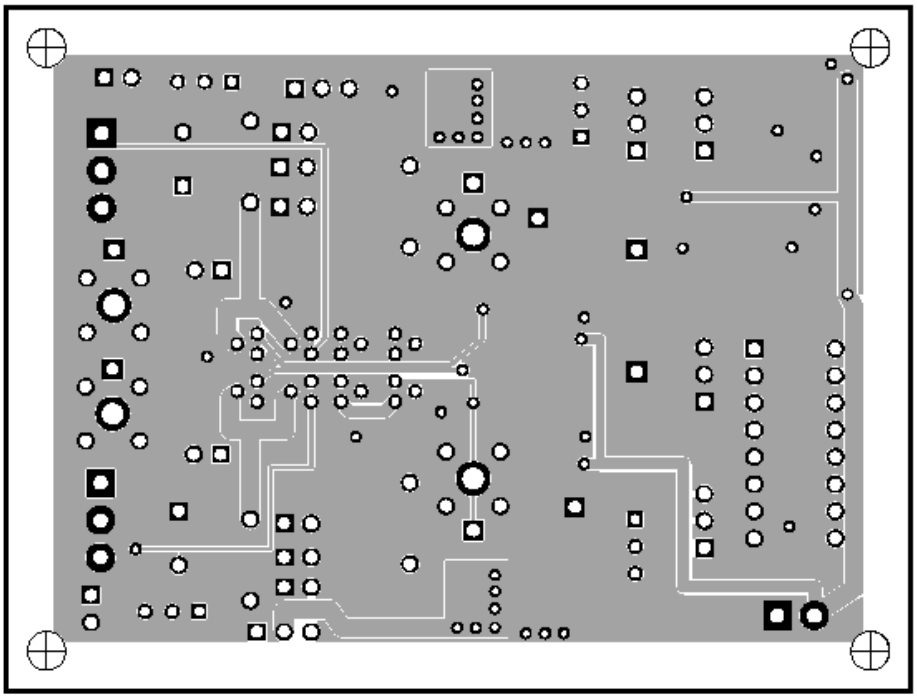
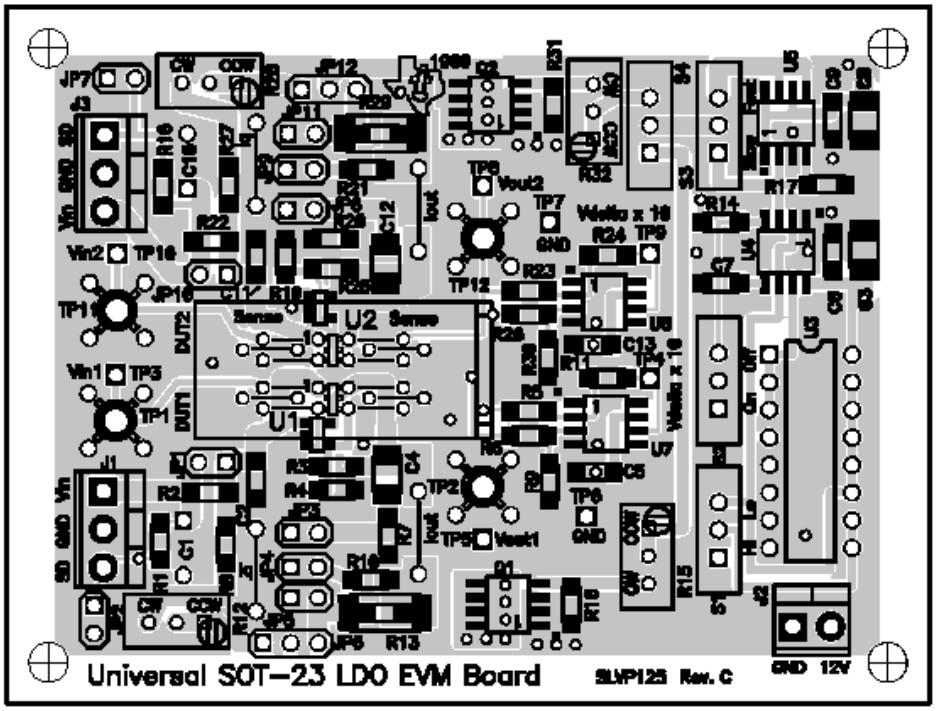


Figure 1–5. Assembly Drawing (top assembly)



Chapter 2

EVM Adjustments and Test Points

This chapter explains the following four EVM adjustment modes:

- Adjustment by switch
- Adjustment by jumper
- Adjustment by trimmer
- Adjustment by programming header

Figure 2–1 shows the locations of the adjustment points on the board.

Topic **Page**

2.1 Adjustment by Switch

- ❑ S1 toggles between high (direction labelling) or low transient generator frequency.
- ❑ S2 switches the transient generator on (direction labelling) and off.
- ❑ S3 toggles between slower (direction labelling) and faster transients.
- ❑ S4 directs transients either to DUT1 (direction labelling) or DUT2.

2.2 Adjustment by Jumper

Table 2–1 lists adjustments that can be made by jumpers.

Table 2–1. Jumper Functions

Function/Device	DUT1	DUT2
Bypasses input resistor	JP1	JP10
Enables DUT	JP2	JP7
Bypasses ESR emulation	JP3	JP8
Set minimum load	JP4	JP9
Set maximum load	JP5	JP11
Toggles between input voltage (direction trimmer) and load transient	JP6	JP12

2.3 Adjustment by Trimmer

Table 2–2 lists the adjustments that can be made by trimmer.

Table 2–2. Trimmer Adjustments

Function/Device	DUT1	DUT2
Risetime of transient	R15	R32
Input voltage spike transient impact	R12	R28

2.4 Adjustment by Programming Header

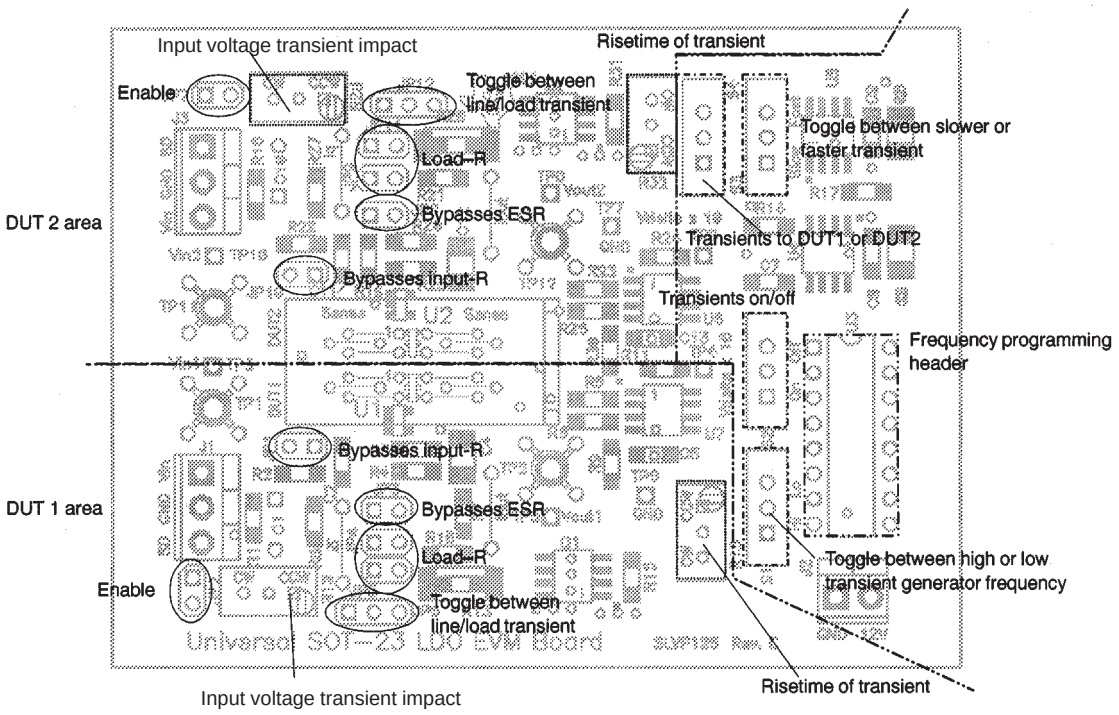
The programming header can be used to program the frequency and the duty cycle of the transient generator. Table 2–3 lists the timing equations.

Table 2–3. Timing Equations

Timing Equations With Diode DH1 for Low Duty Cycles	Timing Equations Without Diode
$RH1 = \frac{t_{on}}{0.693 \times C}$	$RH1 = \frac{t_{on} \times (2D–1)}{0.693 \times D \times C}$
$RH2 = \frac{t_{on} \times (1–D)}{0.693 \times D \times C}$	$RH2 = \frac{t_{on} \times (1–D)}{0.693 \times D \times C}$

Note: t_{on} = desired load on-time [s]
D = on-time duty cycle
C = total capacitance in circuit (CH1 or CH1 + CH2) [F]
RH1, RH2 = Timer resistors value (refer to schematics) [Ω]

Figure 2–1. Location of Adjustment Parts



Top Assembly

2.5 Test Setup

Figure 2–2 shows the test setup. Follow these steps for initial power up of the SLVP125

1) Populate the test devices on the board (U1 and U2) and adjust the settings of jumpers, switches, and trimmers to fit test requirements. Also make sure that the minimum/maximum load resistors are populated and matched to the output current of the LDO you want to test, and that they can handle the power dissipation.

2) Connect a 12-V lab power supply to the 12-V input J2. The polarity is printed on the board. A current limit of 200 mA should be adequate for the test and measure circuit.

3) Connect a 2nd lab power supply (at least capable to supply 2 A) to the J1 and J3 connector at Vin and GND. The polarity is printed on the board. Verify that the output voltage limit is set to 13.5 V and that the output is set to 0 V.

4) Turn on the 12-V lab supply. Turn on the second power supply and ramp the input voltage up to the desired maximum but not further than 13.5 V.

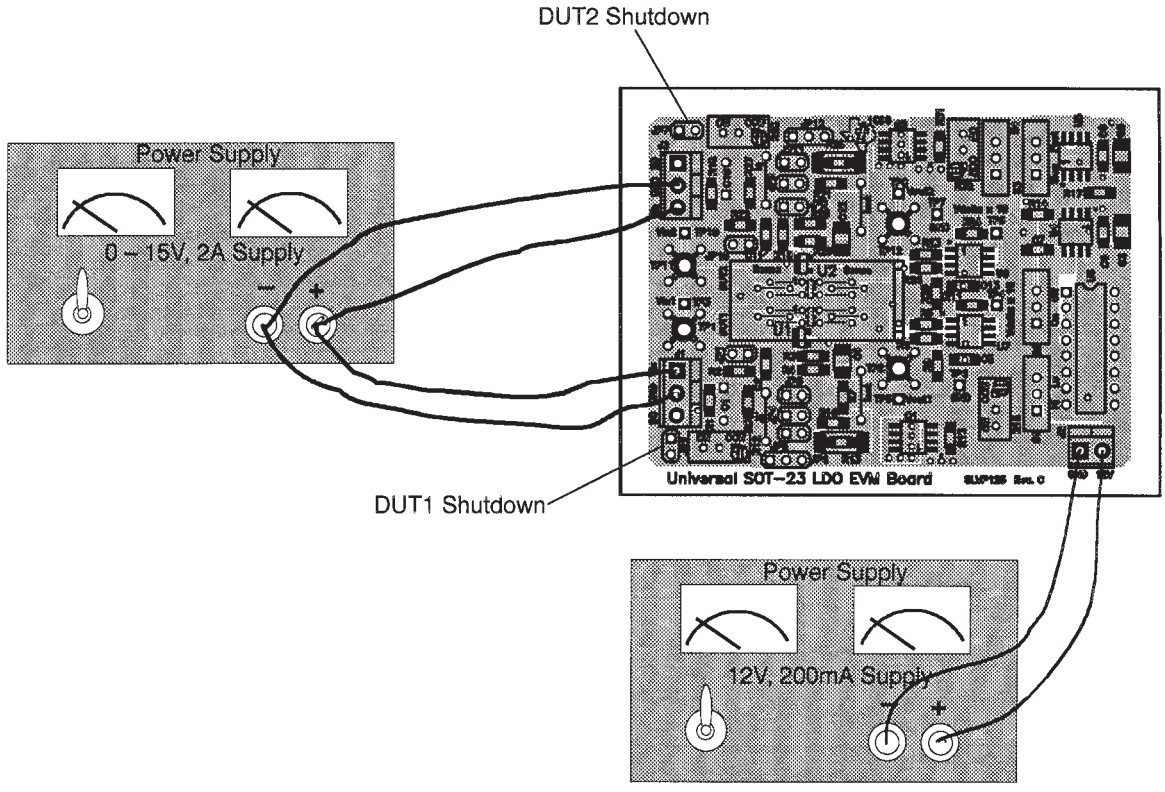
5) Verify that the output voltage (measured at the V_{out1} and V_{out2} pins respectively) has the desired value.

Note:

1) With very small loads (<100 μA) you will measure a small output voltage even with the device in shutdown. This is due to offset voltages of the opamps U6 and U7.

2) If you plan to insert a socket for DUT, you will have to remove the jumper wires from the socket area. The socket has internal connections.

Figure 2–2. Test Setup



NOTE: All wire pairs should be twisted.

Chapter 3

Circuit Design

This chapter describes the LDO circuit design procedure.

Topic **Page**

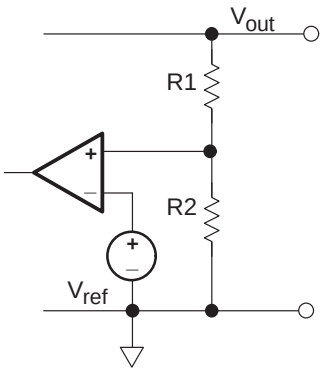
3.1 Adjusting the TPS76x01/TPS77001 Output Voltage

All voltage regulators of the TPS76x01/TPS77001 families use the same internal bandgap voltage, see also Figure 1–1. In the adjustable version, the resistors R1 and R2 are external resistors. Due to the virtual short circuit between the input pins of an op amp, the voltage V_{ref} applies to both the +input pin and the –input pin.

Note:

All TPS76x01/TPS77001 devices except the TPS764xx use pin 4 as a feedback pin for the adjustable version. At the TPS764xx pin 4 acts as a bypass pin for an external bypass capacitor. This capacitor is used to further reduce output voltage noise. See the TPS764xx data sheet for details.

Figure 3–1. Programming the TPS76x01/TPS77001



The equation for the output voltage is:

$$\frac{V_{ref}}{V_{out}} = \frac{R2}{R1 + R2} \Rightarrow \underline{\underline{V_{out}}} = V_{ref} \times \frac{R1 + R2}{R2} = \underline{\underline{V_{ref} \times \left(1 + \frac{R1}{R2}\right)}}$$

The resistor ratio is a function of

$$\frac{V_{out}}{V_{ref}} - 1 = \frac{R1}{R2}$$

Using Figure 3–2, it is possible to get a quick ratio for R1/R2 and their maximum value.

Figure 3–2. Resistor Values

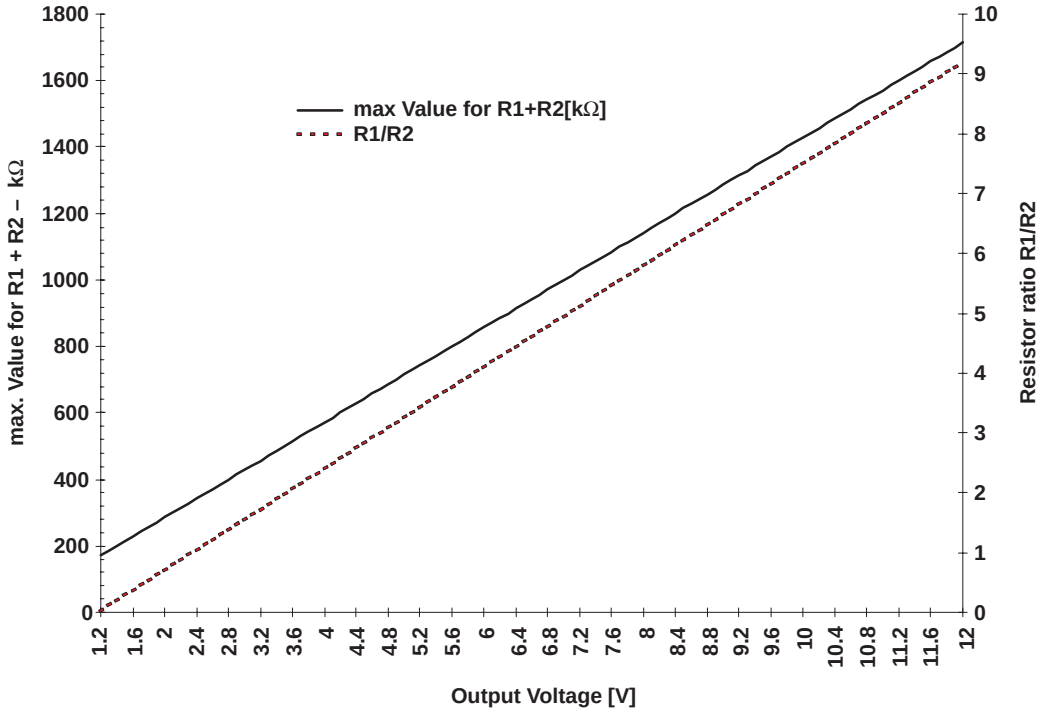


Table 3–1. Exact Resistor Values

V_{out}	R1/R2	Maximum Value for R1+R2[kΩ]
1.2	**0.018676**	**171.429**
1.3	0.103565	185.714
1.4	0.188455	200.000
1.5	0.273345	214.286
1.6	0.358234	228.571
1.7	0.443124	242.857
1.8	0.528014	257.143
1.9	0.612903	271.429
2	**0.697793**	**285.714**
2.1	0.782683	300.000
2.2	0.867572	314.286
2.3	0.952462	328.571
2.4	1.037351	342.857
2.5	1.122241	357.143
2.6	1.207131	371.429
2.7	1.29202	385.714
2.8	1.37691	400.000
2.9	1.4618	414.286
3	**1.546689**	**428.571**
3.1	1.631579	442.857
3.2	1.716469	457.143
3.3	1.801358	471.429

Table 3–1. Exact Resistor Values(Continued)

V_{out}	R1/R2	Maximum Value for R1+R2[kΩ]
3.4	1.886248	485.714
3.5	1.971138	500.000
3.6	2.056027	514.286
3.7	2.140917	528.571
3.8	2.225806	542.857
3.9	2.310696	557.143
4	**2.395586**	**571.429**
4.1	2.480475	585.714
4.2	2.565365	600.000
4.3	2.650255	614.286
4.4	2.735144	628.571
4.5	2.820034	642.857
4.6	2.904924	657.143
4.7	2.989813	671.429
4.8	3.074703	685.714
4.9	3.159593	700.000
5	**3.244482**	**714.286**
5.5	3.66893	785.714
6	**4.093379**	**857.143**
6.5	4.517827	928.571
7	**4.942275**	**1000.000**
7.5	5.366723	1071.429
8	**5.791171**	**1142.857**
8.5	6.21562	1214.286
9	**6.640068**	**1285.714**
9.5	7.064516	1357.143
10	**7.488964**	**1428.571**
10.5	7.913413	1500.000
11	**8.337861**	**1571.429**
11.5	8.762309	1642.857
12	**9.186757**	**1714.286**

To ensure proper regulation, the divider current should be 7 μA. The maximum resistor value for R1+R2 can be seen in Figure 3–2 and Table 3–1.

To get the actual values for R1 and R2, get the resistor ratio and the maximum resistor value for the desired output voltage out of Figure 3–2 or Table 3–1 and do the following calculations:

For 3 V, one gets:

$$\text{I)}\quad \frac{R1}{R2} = 1.546689 \qquad \text{II)}\quad R1 + R2 = 428.571\ \text{k}\Omega$$

$$\Rightarrow \text{I}')\quad R1 = 1.546689 \times R2$$

$$\text{I}')\ \text{in}\ \text{II)}: \qquad \Rightarrow 1.546689 \times R2 + R2 = 428.571\ \text{k}\Omega$$

$$\Rightarrow \underline{\underline{R2}} = \frac{428.571\ \text{k}\Omega}{2.546689} \underline{\underline{= 168.286\ \text{k}\Omega}}$$

Make R2 = 169 kΩ and calculate R1:

Derived from equation I), one gets for R1:

$$\underline{\underline{R1}} = 1.546689 \times 169\ \text{k}\Omega \underline{\underline{= 261.39\ \text{k}\Omega}}$$

The next value in the E96 series shown in Table 3–2 is 261 kΩ.

The error for using these resistors is:

$$\frac{261\ \text{k}\Omega}{169\ \text{k}\Omega} = 1.544379 \Rightarrow \textit{Error} = \left(1 - \frac{1.544379}{1.546689}\right) \times 100\% = 0.149371\%$$

A free-ware program called *WinResis* available on the Internet can help you find the correct resistor values.

Table 3–2. E96 Resistor Series

E96 series					
100	147	215	316	464	681
102	150	221	324	475	698
105	154	226	332	487	715
107	158	232	340	499	732
110	162	237	348	511	750
113	165	243	357	523	768
115	169	249	365	536	787
118	174	255	374	549	806
121	178	261	383	562	825
124	182	267	392	576	845
127	187	274	402	590	866
130	191	280	412	604	887
133	196	287	422	619	909
137	200	294	432	634	931
140	205	301	442	649	953
143	210	309	453	665	976

3.2 Temperature Considerations

To protect the device and assure the specifications, the maximum junction temperature should not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$. The maximum power dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{J,max} - T_A}{R_{\theta JA}}$$

Where

$T_{J,max}$ is the maximum allowed junction temperature [°C], i.e., 125°C for the TPS76xxx/TPS77xxx families

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 285°C/W for the 5-terminal SOT23

T_A is the ambient temperature

The regulator dissipation is calculated using:

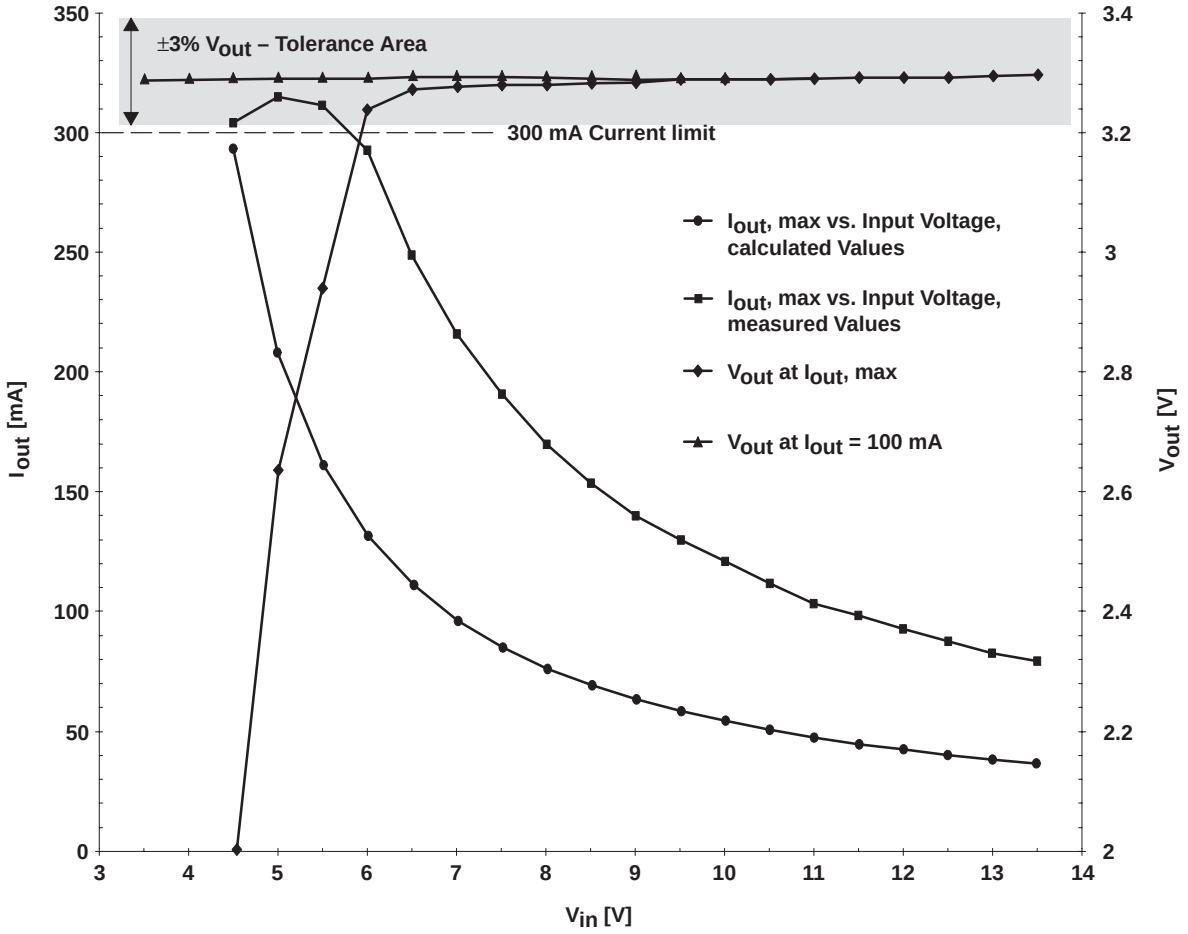
$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT}$$

The maximum output current at a given temperature can be calculated as:

$$I_{out,max}[mA] = \frac{125°C - T_A}{\left(V_{in} - V_{out}\right) \times 285°C/W} \times 1000\ mA$$

Figure 3–3 shows the test results on a TPS76933 device. Also displayed are the calculated results.

Figure 3–3. Calculated and Measured Maximum Output Current vs Input Voltage Without Cooling for TPS76933 in Test Setup



3.3 External Capacitor Requirements – ESR

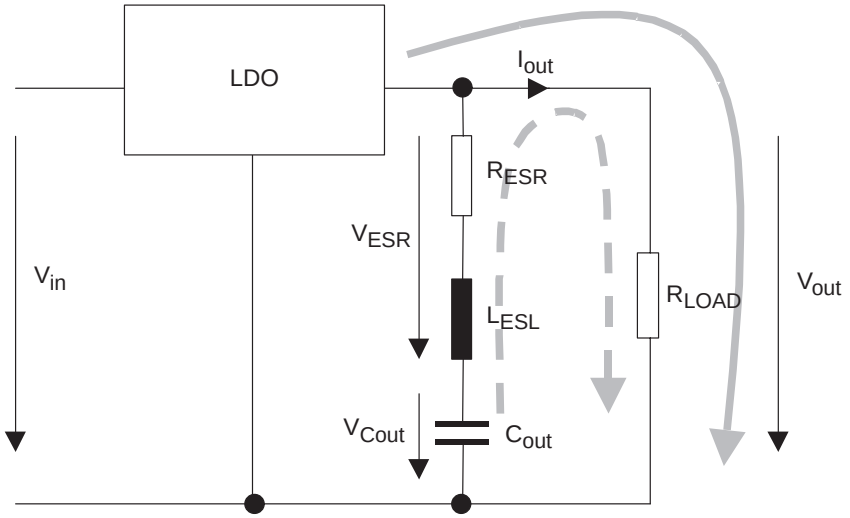
Besides its capacitance, every capacitor also contains parasatic resistances. These parasatic resistances are ohmic resistances as well as inductive impedances. The ohmic resistances are called equivalent series resistance (ESR), and the inductive impedances are called equivalent series inductance (ESL). L is the designator for inductors. The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 3–4.

Figure 3–4. ESR and ESL

In most cases one can neglect the very small inductive impedance ESL. Therefore the following description focuses mainly on the parasitic resistance ESR.

Figure 3–5 shows the output capacitor and its parasitic resistances in a typical LDO output stage.

Figure 3–5. LDO Output Stage With Parasitic Resistances ESR and ESL



In steady state (dc state condition) the load is supplied by the LDO (solid arrow) and $V_{Cout} = V_{out}$. This means no current is flowing into the C_{out} branch. If now I_{out} suddenly increases, the following occurs (see Figure 3–6 and the screen shot in Chapter 4, Figure 4–7):

The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 3–6). Therefore capacitor C_{out} has to provide the current for the new load condition (dashed arrow). C_{out} acts like a battery now with an internal resistance, ESR. Therefore, depending on the current demand at the output, voltage drop will occur at R_{ESR} and L_{ESL}. This voltage is shown as V_{ESR} in Figure 3–5. The internal inductance also causes an additional delay (shown as t_L in Figure 3–6), so C_{out} could not immediately supply current to the load. When C_{out} is finally conducting current to the load, the initial voltage at the load will be $V_{out} = V_{Cout} - V_{ESR}$. Due to the discharge of C_{out}, the output voltage V_{out} will drop continuously until the response time t_1 of the LDO is reached and the LDO will resume supplying the load. From this point the output voltage starts rising again until it reaches the level directed by the LDO. This period is shown as t_2 in Figure 3–6. The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

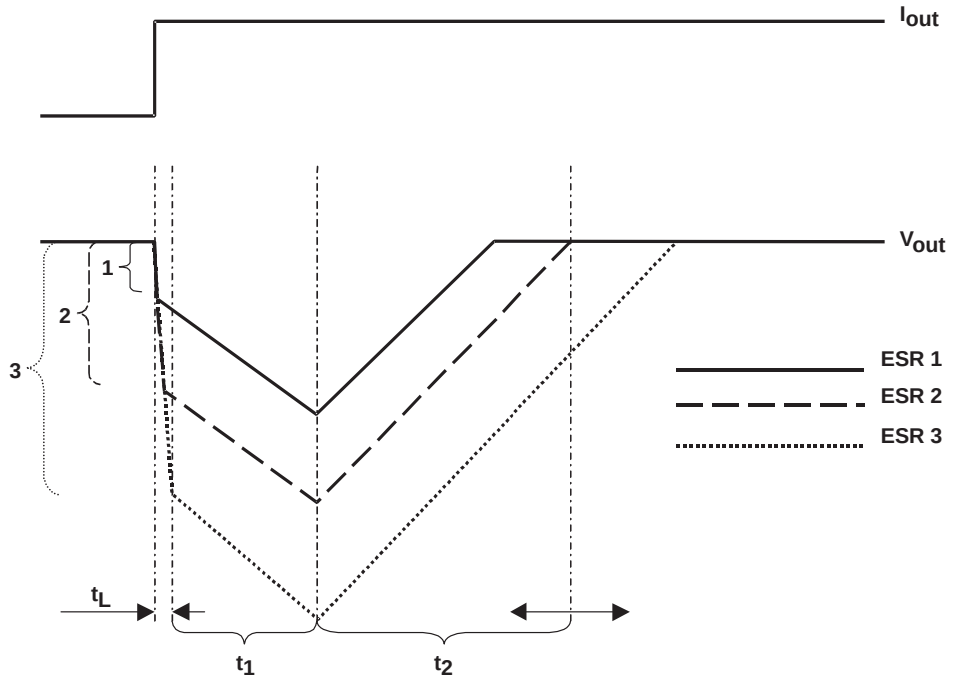
Understanding the above, one can draw the following conclusions:

- The higher the ESR, the bigger the spike at the beginning of a load transient and the longer the time to return to a steady state.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage loss during the LDO response period (shown as t_1 in Figure 3–6).

Conclusion:

The higher the output current and the load step differentials, the higher the requirements for a C_{out} with low ESR.

Figure 3–6. Correlation of Different ESRs and Their Influence to the Regulation of V_{out} at a Load Step From Low to High Output Current



In order to get a good performing system, an LDO with short response time and an output capacitor with low ESR are required.

For any regulator of the TPS76xxx/TPS770xx series, an output capacitor of at least 4.7 μF is required. The ESR of the capacitor should be between 0.5 Ω and 3 Ω to ensure stability.

Chapter 4

Test Results

This chapter presents laboratory test results for the LDO design.

Topic **Page**

4.1 Test Results

Figures 4–1 through 4–7 show the results of various tests and test conditions for the circuit using the TPS76933 device.

Figure 4–1. Rise Time of Function Generator at Gate of MOSFET Q1 (high speed)

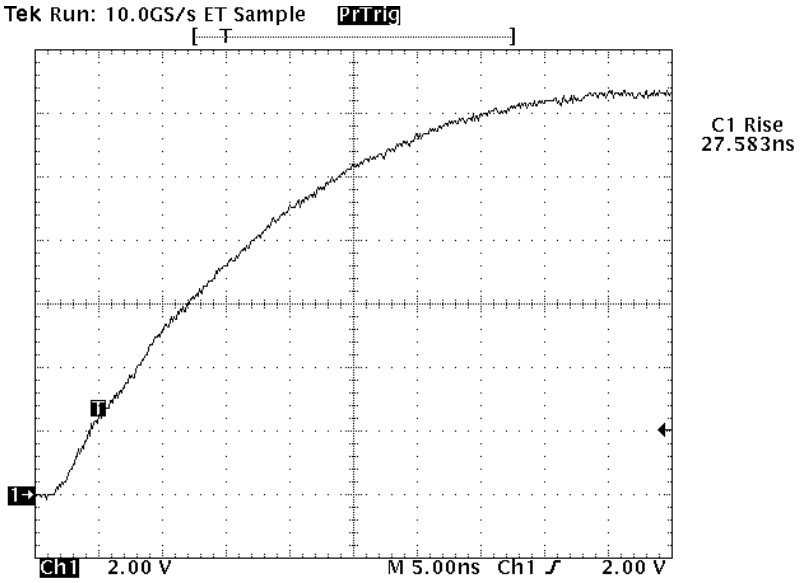


Figure 4–2. Rise Time of Function Generator at Gate of MOSFET Q1 (low speed)

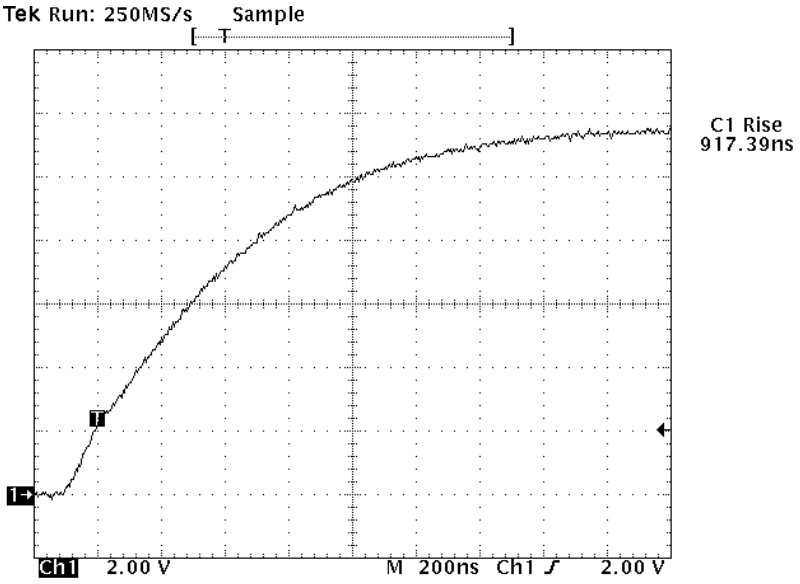


Figure 4–3. Transient at Input (Ch1); 4.3 V Input, 3.3 V Output (Ch2) at 100 mA Load, C_{out} = 10 µF

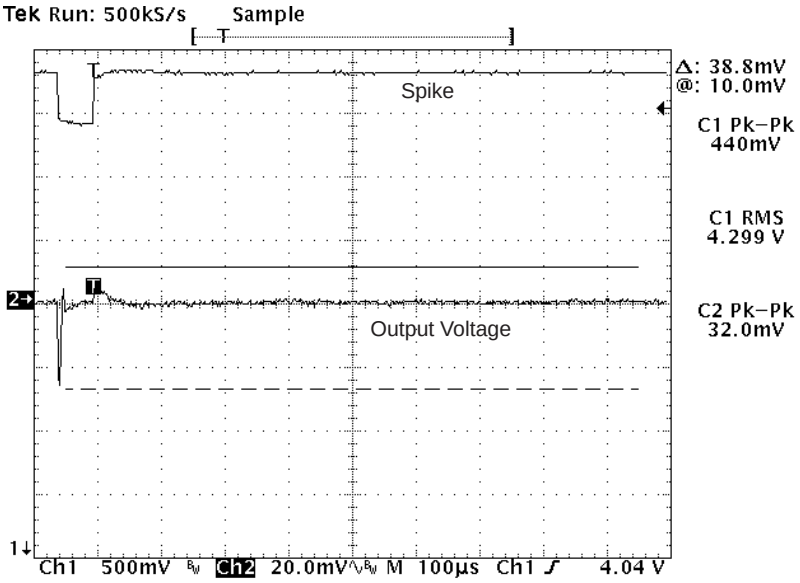


Figure 4–4. Delay Time EN → Output High

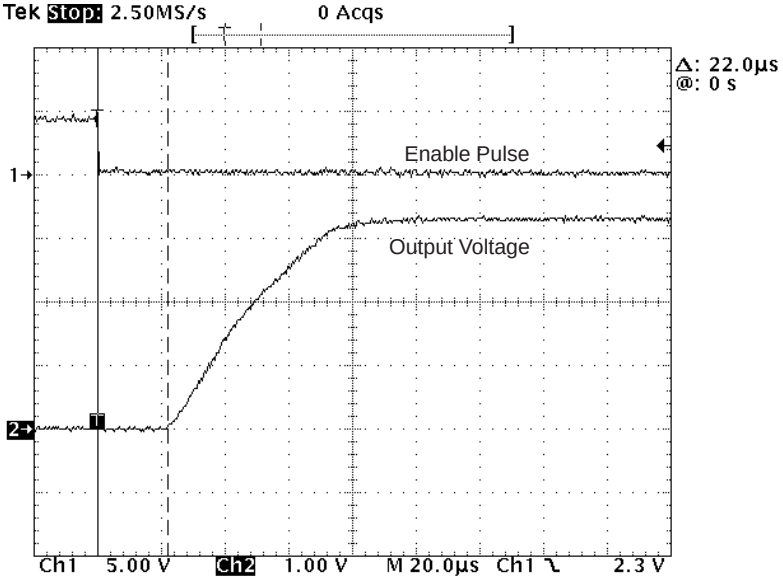


Figure 4–5. Full Load (100 mA) – No Load Transition, ΔV_{out}, Whole Period

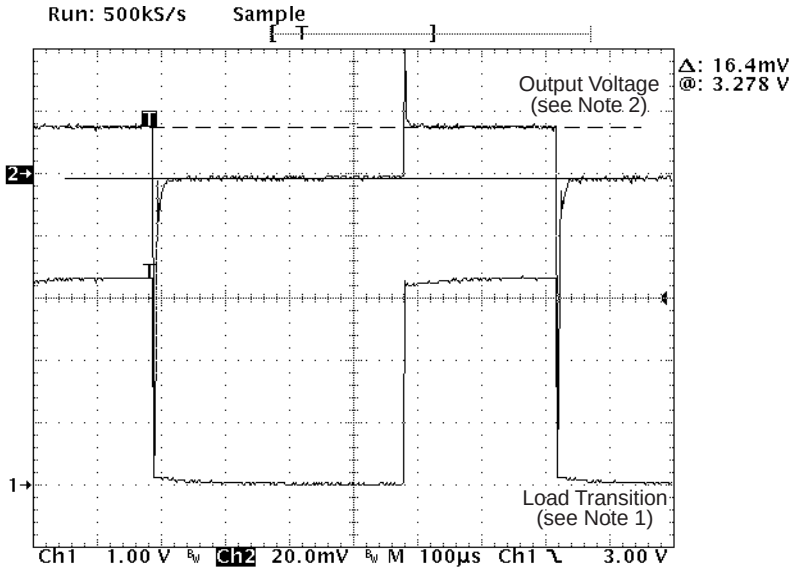


Figure 4–6. Full Load (100 mA) – No Load Transition With C_{out} = 10 µF Electrolytic

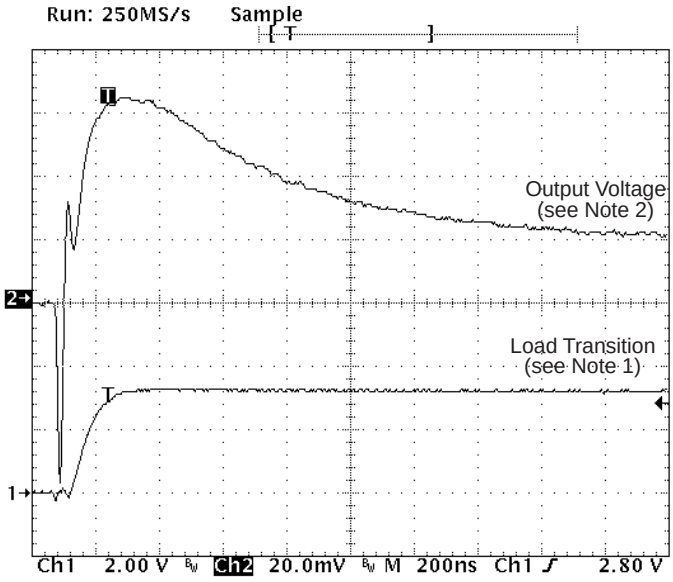
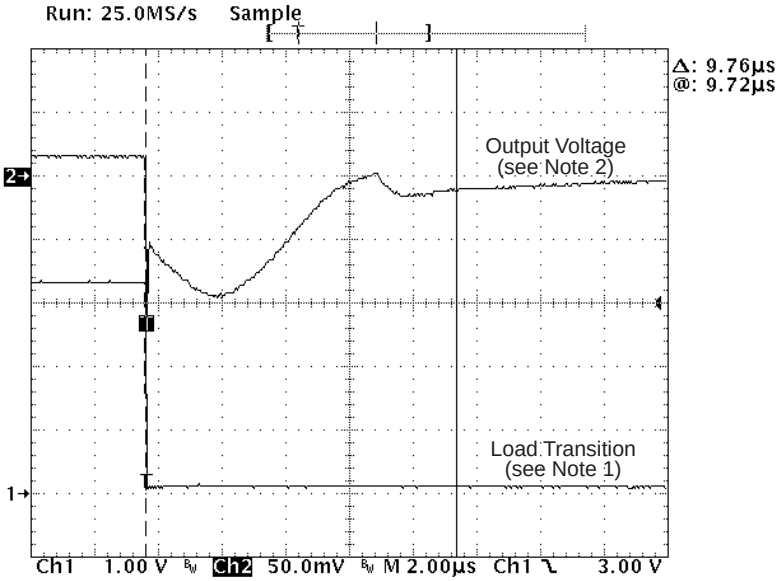


Figure 4–7. No Load – Full Load (100 mA) Transition With C_{out} = 10 μF Electrolytic



Notes:
1) The load transition was measured as the voltage drop at the drain of Q1 (see Figure 1–2). Therefore load on is displayed as 0 V and load off is displayed as 3.3 V.
2) In order to display the output voltage transient with high resolution, a dc offset of 3.3 V was introduced. The actual dc values can be seen with the cursor lines in Figure 4–5.
output voltage without full load: 3.296 V
output voltage with full load: 3.278 V