Synchronous Buck Converter Design Using TPS56xx Controllers in SLVP10x EVMs User's Guide

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Preface

Read This First

About This Manual

This user's guide describes techniques for designing synchronous buck converters using TI's SLVP10x evaluation modules (EVM) and TPS56xx ripple regulator controllers.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 Introduction
- Chapter 2 Design Procedure
- Chapter 3 Test Results

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

- ❑ TPS56xx data sheet (literature number SLVS177)
- ❑ Designer's Notebook *The TPS56xx Family of Power Supply Controllers* (literature number SLVT140A)

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Chapter 1

Introduction

Design simplicity, low component count, and lower cost make buck converters popular solutions where low input voltages are available for the converter and where isolation is not a requirement.

This user's guide describes techniques for designing synchronous buck converters using TI's SLVP10x evaluation modules (EVM) and TPS56xx ripple regulator controllers. Synchronous buck converters provide an elegant power supply solution for rapidly transitioning DSP loads such as the Texas Instruments TMS320C6201, fast memory, and similar processors. An order of magnitude improvement in dynamic response of this converter over standard control methods reduces hold-up capacitance needs near the transitioning loads, thus saving cost and board space.

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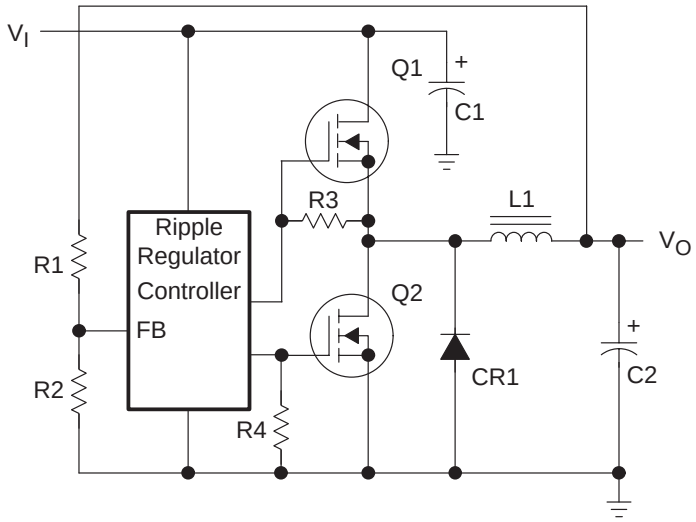
1.1 Synchronous Buck Converter Circuit Operation

In the synchronous buck converter topology, a power MOSFET replaces the traditional buck converter output-stage commutating diode. This improvement reduces the typical 0.5-V-to-1-V diode drop to about 0.3 V or less, resulting in typical circuit efficiency improvements of around 5% and higher.

The basic synchronous buck converter circuit includes a pair of MOSFETs, an output filter, and a controller that provides the synchronous switching function. Figure 1–1 shows the simplified schematic diagram of a typical synchronous buck converter.

Figure 1–1. Typical Synchronous Buck Converter



In the synchronous buck converter shown in Figure 1–1, the ripple regulator controller controls the output voltage.

If the output voltage falls below the regulation level, the controller turns on MOSFET Q1 and turns off Q2; this simultaneously charges inductor L1 and feeds the output load. When the output voltage exceeds the regulation level, the controller turns off Q1 and turns on Q2, thereby providing an alternate path through Q2 to deliver the current in inductor L1 into the load; this maintains continuous power delivery during the on and off states of Q1. The controller ensures that power MOSFETs Q1 and Q2 are never on simultaneously, a condition which would place a momentary short across the input power bus, resulting in much lower efficiencies and potential destruction of the switching devices.

1.2 Design Strategy

The TI SLVP10x evaluation modules (EVM) provide synchronous buck converter circuits for evaluating the capabilities of the TPS56xx family of ripple regulator controllers. The EVM converters can provide proven, demonstrated reference designs to aid in the rapid development of application-specific synchronous buck converters. Output capacities of the EVM converters are optimized for the Siliconix Si4410 power MOSFET device. These devices are rated for 10 amperes of continuous operation, so an 8–ampere converter load rating is well within the rated power capacity.

The 8-ampere output power level is a reasonable selection criteria for powering circuit cards with multiple DSPs, and for providing the regulated voltage to other hardware on the circuit card. Component size can be reduced for designs requiring lower power levels.

The TPS56xx controllers each provide one of four popular output voltage levels. The last two digits of the part number correlate to the set-point voltage level: TPS5633 is the 3.3-V controller, TPS5625 is the 2.5-V controller, TPS5618 is the 1.8-V controller, and TPS5615 is the 1.5-V controller. Many digital devices, memories, and DSP I/O circuits use the 3.3-V level. The core of the TMS320C6201 DSP revision 2.2 silicon requires 2.5-V. Revision 3.0 of this DSP will need 1.8-V. The GTL bus, as well as various processors and future DSPs, may require the 1.5-V controller. An external resistor divider can be used to fine tune the output voltages of these controllers for other applications.

Table 1–1 summarizes the four EVM converter modules.

Table 1–1. Summary of EVM Converter Modules

EVM Part Number	EVM Board Number	Controller	Output Voltage	Max. Output Current
TPS5633EVM–104	SLVP104	TPS5633	3.3 V	8 A†
TPS5625EVM–105	SLVP105	TPS5625	2.5 V	8 A†
TPS5618EVM–106	SLVP106	TPS5618	1.8 V	8 A†
TPS5615EVM–115	SLVP115	TPS5615	1.5 V	8 A†

† Output current is limited by the temperature rise of the power MOSFETs chosen. Higher or lower current designs are possible.

1.3 Design Specification Summary

This section summarizes the design requirements of the EVM converters. Although every attempt was made to accurately describe the performance of the EVM converters and the TPS56xx controllers, in case of conflicts, the TPS56xx data sheet takes precedence over this document.

The TPS56xx family of controllers provides the necessary regulation functions. In addition to a reference voltage accuracy of ±1% over the full operating temperature range, the controller has remote sense inputs to provide a precisely regulated output voltage. The controller also provides undervoltage lock-out, overload protection, overvoltage protection, and overtemperature protection. The controller has a logic level INHIBIT input to control the converter turn-on and turn-off and a power good output to indicate output voltage status. Undervoltage lock-out prevents operation of the power supply when the 12 Vdc input voltage is not sufficient for proper operation. Overload protection protects the power supply from accidental overloads or short circuits. Overvoltage protection prevents damage to the load in the event of an internal power supply failure or presence of high voltages on the output from an external condition. Both overvoltage and overcurrent cause a latched shutdown. Both power MOSFETs are driven to an OFF state. Recovery from shutdown requires removal of the 12 V control input supply for reset. Table 1–2 lists the operating specifications of the EVM converters.

Table 1–2. EVM Converter Operating Specifications

Specification	Min	Typ	Max	Units
Power Input Voltage Range	3		13.2	V
Control Input Voltage Range	10.8		13.2	V
Static Voltage Tolerance†				
SLVP104 (3.3 V)	3.27	3.30	3.33	V
SLVP105 (2.5 V)	2.47	2.50	2.53	V
SLVP106 (1.8 V)	1.78	1.80	1.82	V
SLVP115 (1.5 V)	1.48	1.50	1.52	
Line Regulation‡		± 0.05%	± 0.1%	
Load Regulation§		± 0.2%	± 0.4%	
Transient Response¶		± 50		mV pk
		50		µsec
Output Current Range#	0		8	A
Current Limit#	8.0		9.5	A
Operating Frequency☆		125		kHz
Output Ripple‖				
SLVP104 (3.3 V)		66		mV p–p
SLVP105 (2.5 V)		50		mV p–p
SLVP106 (1.8 V)		50		mV p–p
SLVP115 (1.5 V)		50		mV p–p

Table 1–2. EVM Converter Operating Specifications (Continued)

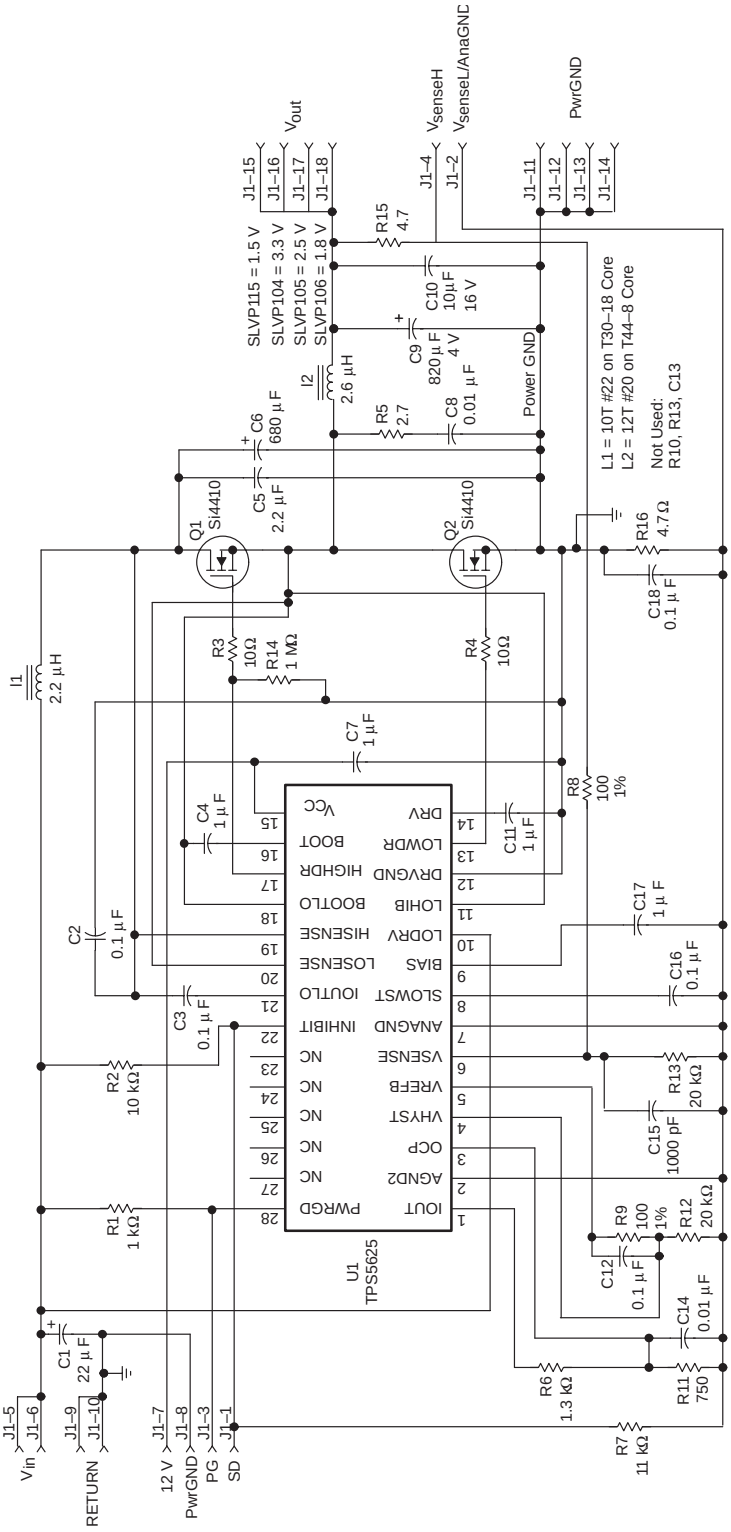
Specification	Min	Typ	Max	Units
Efficiency, 8 A Load				
SLVP104 (3.3 V)		90%		
SLVP105 (2.5 V)		88%		
SLVP106 (1.8 V)		83%		
SLVP115 (1.5 V)		86%		
Efficiency, 4 A Load				
SLVP104 (3.3 V)		93%		
SLVP105 (2.5 V)		92%		
SLVP106 (1.8 V)		89%		
SLVP115 (1.5 V)		80%		

† Vi = 5 V, Io = 8 A
‡ Io = 8 A, Vi = 5 V ±10%
§ Vi = 5 V
¶ Vi = 5 V, Io stepped repetitively from 4 A to 8 A
# Output current rating is limited by thermal considerations. Load currents above this rating may cause damage to the power supply.
‖ Unless otherwise specified, all test conditions are T_A = 25°C, Vi = 5 V, Io = 8 A, Vo = nominal.
☆ Vi = 5 V, Io = 8 A, Vo = 2.5 V

1.4 Schematic

Figure 1–2 shows the SLVP105 EVM converter (2.5 V output) schematic diagram. The schematic diagrams for the other EVM converters are identical except for the controller IC used.

Figure 1–2. SLVP105 EVM Converter Schematic Diagram



1.5 Bill of Materials

Table 1–3 lists materials required for the SLVP105 EVM.

Table 1–3. SLVP105 EVM Bill of Materials

Ref Des	Qty	Part Number	Description	MFG
C1	1	10SS22M	Capacitor, Os-Con, 22 μF, 10 V, 20%	Sanyo
C2	4	GRM39X7R104K016A	Capacitor, Ceramic, 0.1 μF, 16 V, 10%, X7R	muRata
C3		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 μF, 16 V, 10%, X7R	muRata
C4	4	GRM42–6Y5V105Z016A	Capacitor, Ceramic, 1.0 μF, 16 V, +80%–20%	muRata
C5	1	GRM42–6Y5V225Z016A	Capacitor, Ceramic, 2.2 μF, 16 V, Y5V	muRata
C6	1	6SP680M	Capacitor, Os-Con, 680 μF, 6.3 V, 20%	Sanyo
C7		GRM42–6Y5V105Z016A	Capacitor, Ceramic, 1.0 μF, 16 V, +80%–20%	muRata
C8	2	GRM39X7R103K025A	Capacitor, Ceramic, 0.01 μF, 25 V, 10%, X7R	muRata
C9	1	4SP820M	Capacitor, Os-Con, 820 μF, 4 V, 20%	Sanyo
C10	1	GRM235Y5V106Z016A	Capacitor, Ceramic, 10 μF, 16 V, Y5V	muRata
C11		GRM42–6Y5V105Z016A	Capacitor, Ceramic, 1 μF, 16 V, +80%–20%	muRata
C12		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 μF, 16 V, 10%, X7R	muRata
C14		GRM39X7R103K025A	Capacitor, Ceramic, 0.01 μF, 25 V, 10%, X7R	muRata
C15	1	GRM39X7R102K050A	Capacitor, Ceramic, 1000 pF, 50 V, 10%, X7R	muRata
C16	1	GRM39X7R104K016A	Capacitor, Ceramic, 0.1 μF, 16 V, 10%, X7R	muRata
C17		GRM42–6Y5V105Z016A	Capacitor, Ceramic, 1.0 μF, 16 V, +80%–20%	muRata
C18		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 μF, 16 V, 10%, X7R	muRata
J1	1	S1122–18–ND	Header, RA, 18-pin, 0.23 Posts x 0.20 Tails	Sullins
L1	1		Inductor, Filter, 2.2 μH, 10 A (10T #22/T30–18 Core)	
L2	1		Inductor, Filter, 2.6 μH, 10 A (12T #20/T44–8 Core)	
Q1	2	Si4410DY	FET, N-ch, 30-V, 10-A, 13.5-mΩ	Siliconix
Q2		Si4410DY	FET, N-ch, 30-V, 10-A, 13.5-mΩ	Siliconix
R1	1	Std	Resistor, Chip, 1 kΩ, 1/16 W, 5%	
R2	1	Std	Resistor, Chip, 10 kΩ, 1/16 W, 5%	
R3	1	Std	Resistor, Chip, 10 Ω, 1/10 W, 5%	
R4	1	Std	Resistor, Chip, 10 Ω, 1/10 W, 5%	
R5	1	Std	Resistor, Chip, 2.7 Ω, 1/4 W, 5%	
R6	1	Std	Resistor, Chip, 1.3 kΩ, 1/16 W, 5%	
R7	1	Std	Resistor, Chip, 11 Ω, 1/16 W, 5%	
R8	2	Std	Resistor, Chip, 100 Ω, 1/16 W, 5%	
R9		Std	Resistor, Chip, 100 Ω, 1/16 W, 1%	
R11	1	Std	Resistor, Chip, 750 Ω, 1/16 W, 1%	
R12 – R13	1	Std	Resistor, Chip, 20 kΩ, 1/16 W, 1%	
R14	1	Std	Resistor, Chip, 1 MΩ, 1/16 W, 5%	
R15 – R16	1	Std	Resistor, Chip, 4.7 Ω, 1/16 W, 1%	
U1	1	TPS5625PWP	IC, PWM Ripple Controller, Fixed 2.5-V	TI

1.6 Board Layout

Figures 1–3 through 1–5 show the board layout for the SLVP104 through SLVP106 and SLVP115 evaluation modules.

Figure 1–3. Silkscreen

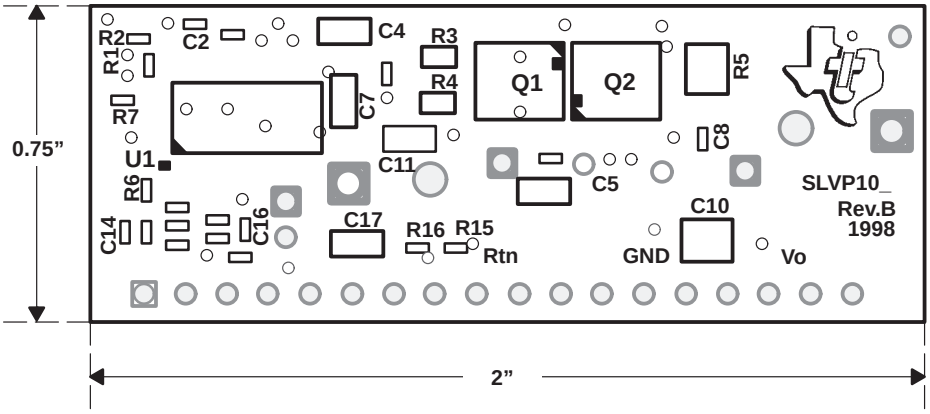


Figure 1–4. Top Side Copper

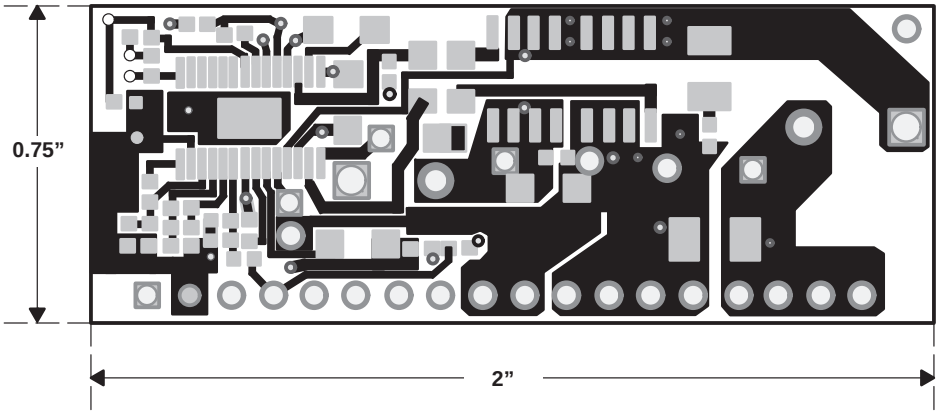
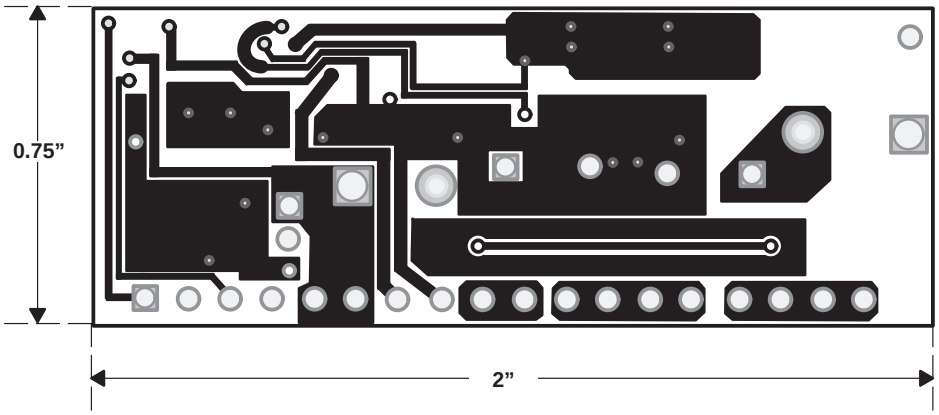


Figure 1–5. Bottom Side Copper



1.7 Mounting Arrangement

Figures 1–6 and 1–7 show two popular mounting arrangements.

Figure 1–6. SIP-Mounted Board Arrangement

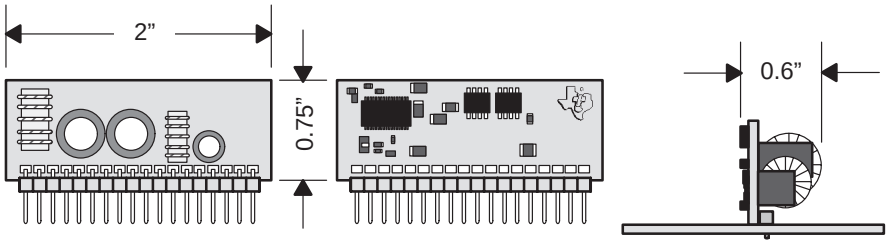
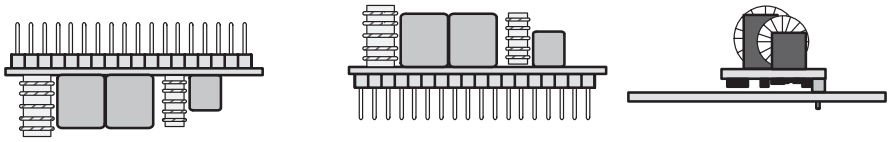


Figure 1–7. Flat-Mounted Board Arrangement



Chapter 2

Design Procedure

The SLVP104, SLVP105, SLVP106, and SLVP115 are dc-dc synchronous buck converter evaluation modules (EVMs) that provide a regulated output voltage at up to 8 A with a power input voltage range of 3 V to 13.2 V. A low power 12 V, 20 mA source is also required to power the TPS56xx controller. The controller operates at a nominal frequency of 125 kHz for 5 V input and 2.5 V output. To provide the highest level of performance, the EVM converters use *hysteretic*, or ripple, control. Hysteretic-controlled synchronous buck converters have several advantages over conventional PWM-controlled power supplies:

- Correction of output voltage variations caused by output-load or input-voltage transients is extremely fast.
- The user controls output ripple by adjusting the operational parameters of the converter, instead of relying on brute force methods requiring the choice of an output filter.
- Hysteretic control sets the operational frequency of the converter. For a given set of external components, the lower the permissible ripple setting, the higher the operational frequency.
- There is no control loop to design.

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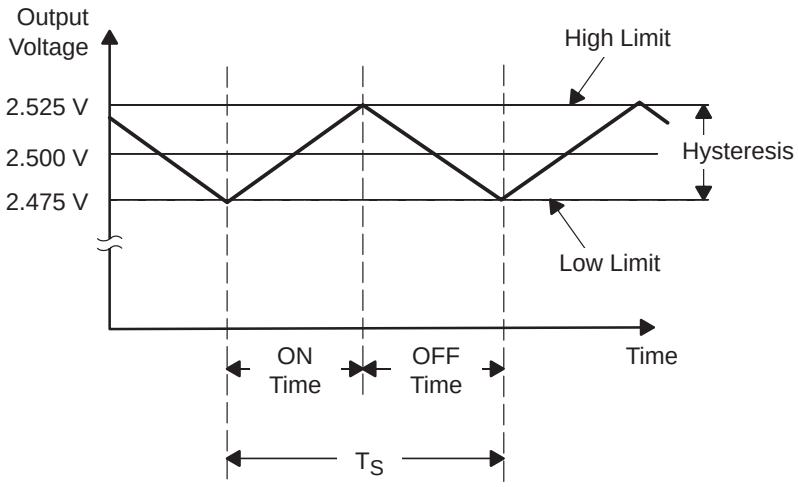
2.1 Detailed Circuit Description

Hysteretic converter control maintains the output voltage within the hysteresis band centered about the internal reference voltage. Figure 2–1 shows a simplified representation of hysteretic control. If the output voltage is at or below the level of the reference minus one-half of the hysteresis (low limit), the controller turns on the top MOSFET (Q1 in Figure 1–1) and turns off the bottom MOSFET (Q2 in Figure 1–1) of the synchronous buck converter power stage. This is the power stage on state, and it causes the output voltage to increase. When the output voltage reaches or exceeds the reference plus one-half of the hysteresis (high limit), the controller turns off the top MOSFET and turns on the bottom MOSFET. This is the power stage off state, and it causes the output voltage to decrease. This hysteretic method of converter control keeps the output voltage within the hysteresis band around the reference voltage. If output-load current steps or input-voltage transients force the output voltage out of the hysteresis band, the controller sets the power-stage MOSFETs in the continuous on or off state, as required, to return the output voltage to the hysteresis band. Thus, the output voltage is corrected as quickly as the output filter allows. There are no error amplifier sensing and adjusting delays, as is the case with either voltage- or current-mode controllers. Hysteretic control is quite robust, since large changes in power stage component values do not affect the output voltage static or dynamic characteristics.

Figure 2–1. Ripple Regulator Output Voltage Waveform



Although some may see the variable switching frequency of hysteretic control as a drawback, it is usually not a problem. Input voltage, output capacitor ESR, capacitor ESL, and output inductance have the most influence on switching frequency. If the input voltage is regulated within a relatively narrow range, and stable filter components are used, the frequency variation is small. Also, since the output voltage ripple is well controlled, this variation is rarely a problem for overall system operation.

In addition to excellent output-voltage regulation and user-adjustable output-voltage ripple, the controller also provides user-adjustable soft-start and overload protection, fixed overvoltage protection, and a logic level enable input.

2.2 Detailed Circuit Design

This section describes design procedures for continuous-mode synchronous buck converter EVMs SLVP104 through SLVP107 and SLVP115 for the TPS56xx family of controllers. Many ways exist to design power supplies, and some iteration may be necessary when performance differs from design predictions. In many instances example calculations accompany the design equations. This user's guide covers four output voltage versions. Unless otherwise specified all example calculations apply to the SLVP105 (5 V_I to 2.5 V_O) version, and reference designators refer to the schematic, Figure 1–2. Statements about the TPS5625 controller also apply to the other controller versions, except for differences in the reference voltage.

2.2.1 Controller Functions

The following section describes controller functions and gives procedures to determine the correct component values to implement them.

2.2.1.1 Slowstart Design

Slowstart, or soft-start, reduces power-up transients. Without slowstart, the following events occur when input power is applied:

- The output voltage is initially zero volts.
- The controller turns on the top MOSFET to raise the output voltage to approximately V_{ref}.
- High transient currents may flow in the output inductor and capacitor.

Although this form of start-up usually does not cause component failures, it does apply stresses greater than those typically encountered in normal operation. Good design practice includes slowstart circuitry to avoid these unnecessary stress levels.

The slowstart circuit in the TPS5625 controls the output voltage power-up rate. An internal current source charges a capacitor connected between SLOWST (pin 8) and ANAGND (pin 7). The output voltage follows the voltage on the slowstart capacitor during start-up. The following equation determines slowstart charging current:

$$I_{SLOWSTART} = \frac{I(VREFB)}{5}$$

Where I(VREFB) = the current out of VREFB (pin 5).

Choice of slowstart time and capacitor value is largely arbitrary as long as system start-up time requirements are met. For this design, a slowstart time of 10 ms is chosen, and the slowstart capacitor is chosen to be 0.1 µF. Therefore, to charge 0.1 µF from zero volts to 2.5 volts in 10 ms, the following equation holds:

$$I_{SLOWSTART} = C_{SLOWSTART} \times \frac{\Delta V_C}{\Delta t_{SS}} = 0.1\ \mu F \times \frac{2.5\ V}{10\ ms} = 25\ \mu A$$

This gives a value of I(VREFB) = 5 × 25 μA = 125 μA.

So, the resistance required from VREFB (pin 5) is:

$$R = \frac{2.5\ V}{125\ \mu A} = 20\ k\Omega.$$

This value is used in the next section to determine the values of R9 and R12 that set the hysteresis level.

2.2.1.2 Output Voltage Ripple

The next step is to choose the desired output voltage ripple. As a first approximation, the output voltage ripple is the difference between the two levels (low limit and high limit) shown in Figure 2–1. Setting the hysteresis in the hysteresis comparator of the TPS5625 sets these two levels. Two external resistors set the hysteresis so it is centered around VREF (pin 5). Connect the two external resistors to form a resistor divider from VREFB (pin 5) to ANAGND (pin 7) with the center of the divider connected to VHYST (pin 4). The comparator hysteresis is equal to twice the voltage between the VREFB (pin 5) and VHYST (pin 4) pins. Or,

$$V_{Hysteresis} = 2 \times (VREFB – VHYST)$$

For this design, 25 mV of hysteresis was chosen.

$$V_{Hysteresis} = 25\ mV = 2 \times (2.5\ V – VHYST).$$

Solving for VHYST:

$$VHYST = VREFB – \frac{V_{Hysteresis}}{2} = 2.5 – \frac{25\ mV}{2} = 2.4875\ V.$$

Referring to the schematic, Figure 1–2, the two external resistors are R9 and R12. From the previous section, the total resistance required is 20 kΩ. Since R9 is very small compared to R12, we set R12 = 20 kΩ. Now, to calculate the value of R9:

$$VHYST = VREFB \times \frac{R12}{R12 + R9}$$

Solving for R9:

$$R9 = \frac{VREFB \times R12}{VHYST} – R12 = \frac{(2.5\ V)(20\ k\Omega)}{2.4875} – 20\ k\Omega = 100\ \Omega$$

A 0.1-μF capacitor, C12, placed across R9, provides noise immunity.

The propagation delay of the hysteretic comparator also influences output voltage ripple. The TPS5625 hysteretic comparator has a 150-ns typical propagation delay with a 250-ns maximum. This delay must be considered when calculating the power stage on-time and off–time; it is discussed in the *Detailed Output Ripple Analysis* section.

2.2.1.3 Output Voltage Sense

To sense the output voltage, a small amount of noise filtering must be applied to prevent the hysteretic comparator from tripping on noise spikes. Capacitor

C15 provides the noise filtering in conjunction with the voltage divider formed by resistors R8 and R13. Although necessary, this filtering causes additional delay from the output voltage to the VSENSE pin of the TPS5625. For the values used in this design, the delay is approximately 120 ns. This delay is in addition to the hysteretic comparator propagation delay discussed in the previous section.

2.2.1.4 Output Voltage Remote Sense

The EVM design provides remote output-voltage sensing. If remote sensing is not desired, do not connect the remote sense connections, VsenseH and VsenseL/AnaGnd. If remote sensing is not connected, the unit reverts to local sensing of the output voltage through R15 and R16. Capacitor C18, across R16, suppresses noise.

2.2.1.5 Overcurrent Protection

A sample-and-hold circuit measures the power supply output current by sensing the on-state drain-to-source voltage of the top MOSFET (Q1 in Figure 1–2). This arrangement improves efficiency over solutions having a separate current sensing resistor. The drain of Q1 is connected to HISENSE (pin 19). The source of Q1 is connected to LOSENSE (pin 20). When Q1 is on, a TPS5625 internal switch is also on and samples the source voltage of Q1. This sampled voltage is applied to IOUTLO (pin 21) and is held by the external 0.1-µF capacitor, C3, which is connected from IOUTLO (pin 21) to HISENSE (pin 19). The TPS5625 amplifies (gain=2) the sampled-and-held voltage on C3 and sends the output voltage to IOUT (pin 1).

A resistor-divider network (R6 and R11) applies the IOUT output voltage to OCP (pin 3). The resistor-divider network is designed so that the voltage applied to OCP is 100 mV for the desired output current limit point. A 0.01-µF capacitor, C14, connected from OCP to ANAGND, suppresses noise. If the voltage on OCP exceeds 100 mV, a fault latch is set and the output drivers are turned off. The latch remains set until VCC (pin 15) goes below the undervoltage lockout value. A 0.1-µF local-bypass capacitor, C2, is placed from HISENSE (pin 19) to DRVGND (pin 12). The following equations summarize the relationships discussed above.

The on-state drain-to-source voltage of Q1 is:

$$\left(V_{HISENSE} - V_{IOUTLO}\right) = I_O \times R_{DS(on)}$$

The voltage difference, $V_{HISENSE} - V_{IOUTLO}$, is internally amplified by a fixed gain of two to produce the IOUT signal.

$$V_{IOUT} = \left(V_{HISENSE} - V_{IOUTLO}\right) \times 2$$

The V_{IOUT} signal is scaled for the desired current limit level and applied to the OCP pin:

$$V_{OCP} = V_{IOUT} \times \frac{R11}{R6 + R11}$$

Therefore, to set the power supply output current, first calculate the quantity I_O*$R_{DS(on)}$ for the value of I_O desired for current limit. The temperature dependence of $R_{DS(on)}$ must also be considered, since this parameter varies up to 50% at high temperatures for typical MOSFETs. Next, multiply this voltage by two. Finally, set the R6 and R11 voltage divider to produce 100 mV at the desired current limit point.

An alternate current sensing scheme, using a current sense resistor in series with the drain of Q1, provides higher accuracy at the expense of lower efficiency.

2.2.1.6 Power Good

The power-good circuit monitors V_O for an undervoltage condition. If V_O drops below 93% of VREF, open-drain output PWRGD is pulled low. Resistor R1 is a pullup for the open-drain output.

2.2.1.7 Bias

The analog BIAS (pin 9) output from the internal analog bias regulator provides a quiet bias supply for the internal controller circuitry. External loads should not be driven by the bias regulator. A 1-µF capacitor, C17, is connected from BIAS to ANAGND.

2.2.1.8 Low-Side Drive Controls

The TPS56xx contains circuitry to control the low-side MOSFET drive for various applications.

LODRV (pin 13) is an enable input for the low-side MOSFET driver. This pin is connected to the 5 V input supply for normal synchronous operation. Applying a logic low to LODRV causes the driver for the low-side MOSFET to go to a high state, causing the low-side MOSFET to turn on and act as a crowbar for the output. This input has precedence over any input present at LOHIB (pin 11); that is, a low input to LODRV overrides the inhibit function.

LOHIB is an inhibit input for the low-side MOSFET driver. This input must be logic low before the low-side MOSFET can be turned on; that is, a logic high on LOHIB prevents the low-side MOSFET driver from turning on the low-side MOSFET. For normal synchronous operation, this pin is connected to the junction of the high- and low-side MOSFETs. This prevents cross-conduction of the two MOSFETs by constraining the low-side MOSFET to off unless its drain-to-source voltage is at a low level. Shoot-through current caused by both MOSFETs being on simultaneously is actively prevented.

Note: If LODRV is low, the low-side MOSFET is turned on regardless of the LOHIB input.

2.2.1.9 High Side Driver

The high-side driver, designed to drive low Rds(on) n-channel MOSFETs, has a peak current rating of 2 A, source and sink. The driver for the high-side MOSFET can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The maximum voltage that can be applied between BOOT and DRVGND is 32 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting V_{CC} to BOOT. A 1-μF bypass capacitor, C4, is connected from BOOT (pin 16) to BOOTLO (pin 18).

2.2.1.10 Grounding

There are three separate ground connections enabling the user to isolate high-current grounds from low current logic grounds. The low-current logic ground is called analog ground. ANAGND (pin 7) and AGND2 (pin2) are the connections for analog ground. The high-current ground is called power ground and must be connected to DRVGND (pin 12). The maximum voltage difference between ANAGND and DRVGND must be limited to less than ±0.2 V.

Refer to the Layout Guidelines section of the TPS56xx data sheet for further information on grounding.

2.2.2 External Component Selection

This section shows the procedure used in designing and selecting the power stage components of the SLVP104 through SLVP106 and SLVP115 EVMs.

2.2.2.1 Duty Cycle Estimate

The duty cycle, D, is the ratio of the high-side power-switch conduction time to the period of one switching cycle. An estimate of the duty cycle is used frequently in the following sections. The duty cycle for a continuous mode synchronous step-down converter is given by:

$$D = \frac{V_O + I_O \times R_{DS(on)} + I_O \times R_{IND}}{V_I}$$

Where

$R_{DS(on)}$ = On resistance of the power MOSFETs and
R_{IND} = DC resistance of the output inductor.

From the manufacturer's data sheet for the Si4410 power MOSFET, the on-state drain resistance, $R_{DS(on)}$ = 13.5 mΩ. Assuming a junction temperature of 120°C, $R_{DS(on)}$ is multiplied by 1.4 to account for the increase in resistance at elevated temperature. Therefore, the value for $R_{DS(on)}$ is 13.5 mΩ × 1.4 = 19 mΩ. The dc resistance of the output inductor is approximately 8 mΩ. So, for an output of 2.5 V at 8 A and 5 V in, the duty cycle is:

$$D = \frac{2.5\ V + 8\ A \times 0.019\ \Omega + 8\ A \times 0.008\ \Omega}{5\ V} = 0.54$$

2.2.2.2 Input Capacitance

The input capacitor is selected to provide a low-impedance input voltage source for the power stage. The input capacitor's ESR, ESL, RMS current rating, and capacitance are important parameters during the selection process. The most stringent requirement is often the RMS current that the capacitor must handle. An equation for the RMS current seen by the input capacitor for a buck converter is given by:

$$I_{C6(RMS)} = \sqrt{D \times (1-D) \times I_L^2 + D \times \frac{\Delta I_L^2}{12}}$$

The above equation assumes that there is also an input inductor and its current is constant. For V_I = 5 V and I_O = 8 A, we get:

$$I_{C6(RMS)} = \sqrt{0.54 \times (1-0.54) \times 8^2 + 0.54 \times \frac{2.6^2}{12}} = 4.03\ A$$

The current rating for C6 is 4.84 A.

2.2.2.3 Output Capacitance

Normally, the output capacitor is selected to limit ripple voltage to the level required by the specification, but in a ripple regulator such as this, the control circuit determines the output voltage ripple. The output ripple, previously chosen to be 25 mV, is relatively independent of the output capacitor characteristics. Since output voltage ripple is set, the output capacitor is chosen to provide satisfactory response to fast load transients.

To understand the importance of the output capacitor characteristics, consider the following: This power supply is designed for a worst-case load step of no load (0 Amps) to full load (8 Amps) with a slew rate of 30 A/µs. This implies that the load transient occurs in less than 267 ns .

$$\left(\frac{8\ A}{30\ A/\mu s} = 267\ ns\right)$$

Since the duration of this load transient is less than one switching cycle of the power supply, the output filter alone controls the output voltage deviation. Therefore, for fast load transients, the output capacitor characteristics dominate the output filter performance. In this design, the output capacitor's ESR (equivalent series resistance) and ESL (equivalent series inductance) are the most significant parameters.

To calculate the ESR requirement, assume that the output capacitor supplies all the load-step current. Also assume that the output voltage change due to the capacitor's capacitance is much smaller than the voltage change due to the ESR, and that the capacitor's equivalent series inductance is negligible. In most practical applications, this assumption is reasonable and greatly simplifies calculations. So, the ESR required to limit output voltage changes to 200 mV due to an 8 amp load step is:

$$ESR \le \frac{\Delta V_O}{\Delta I_O} = \frac{200\ mV}{8\ A} = 25\ m\Omega.$$

The required level of ESR needs a large amount of capacitance also. This design uses a Sanyo OS–Con type, electrolytic, 820-μF, 4-V capacitor with a specified maximum ESR of 12 mΩ. This is C9 in Figure 1–2.This capacitor is a good compromise between performance, cost, and board area requirements. Cheaper capacitors require multiple capacitors to achieve equivalent ESR levels. The cost of the Sanyo parts is offset by savings in board area and number of parts required. For good design practice, C10, a 10-μF ceramic capacitor, is placed in parallel with C9. Ceramic capacitors are very effective for suppressing high frequency switching spikes. Using ceramic capacitors in parallel with the main output capacitors also reduces the effects of ESL. Limiting PCB and capacitor lead lengths also controls ESL.

To summarize, the output capacitor(s):

- Must be selected to provide a sufficiently low ESR
- Must have an adequate voltage rating for the application
- Must have an ample ripple current rating to handle the applied ripple current

This ripple current is dependent on the output inductance that is calculated in the next section. The RMS current in the output capacitance is calculated as follows:

$$I_{C\,RMS} = \Delta I_L \times \frac{\sqrt{3}}{6} = \Delta I_L \times 0.289 = 2.6\ A \times 0.289 = 0.75\ A_{RMS}.$$

The capacitor used in this design has a ripple current rating of 5.04 A_{RMS}.

2.2.2.4 Detailed Output Ripple Analysis

To predict the power supply switching frequency, the output voltage ripple must be investigated, since the power supply switching instants are based upon the state of the output voltage.

To begin the analysis, recall that the three elements of the capacitor that contribute to ripple are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance. Assume that all three elements are in series and there are no other parasitic components to consider.

Figure 2–2 shows ideal waveforms to help illustrate the analysis.

The analysis is based on the ac component of the output inductor ripple current flowing through the output capacitor and causing voltage drops across each of the capacitor elements.

Figure 2–2 (a) shows the output-inductor current waveform.

Figure 2–2 (b) shows the current assumed to be flowing in the output capacitor. Notice that the peak-peak amplitude is identical to the inductor current (Figure 2–2 (a)) but with the dc component (= I_O) removed because no dc current can flow in a capacitor.

Figure 2–2 (c) shows the voltage across the capacitor ESR. This voltage is given by:

$$V_{ESR} = I_C \cdot R_{ESR}$$

This approximates switching power supply output voltage ripple.

Figure 2–2 (d) shows the voltage across the capacitor ESL. Since an inductance is assumed, the voltage across the ESL is given by:

$$V_{ESL} = L_{ESL} \cdot \frac{dI_C}{dt}$$

Where L_{ESL} is the equivalent series inductance of the capacitor.

Note that dI_c/dt is just the slope of the inductor current, is constant (and positive) during the on time, and is constant (and negative) during the off time.

Figure 2–2 (e) shows the voltage across the ideal capacitor. This voltage is given by:

$$v_C = \frac{1}{C} \int I_C \cdot dt$$

Where I_C is the current shown in Figure 2–2 (b).

The total output voltage ripple is the sum of the voltages across all three elements. The above three relationships are clearly functions of the inductor current, I_L. They also include what can be called proportionality constants, i.e., R_{ESR}, L, and $1/C$, so that many different shapes of output voltage ripple can be produced depending on the relative values of the proportionality constants. Operating frequency is also a major factor in determining the output voltage shape.

Figure 2–2 (f) shows the sum of one combination of voltages across the three capacitor elements. It represents a simulation of the output voltage ripple when using the circuit elements described in this user's guide.

Figure 2–2. Ripple Regulator Detailed Output Voltage

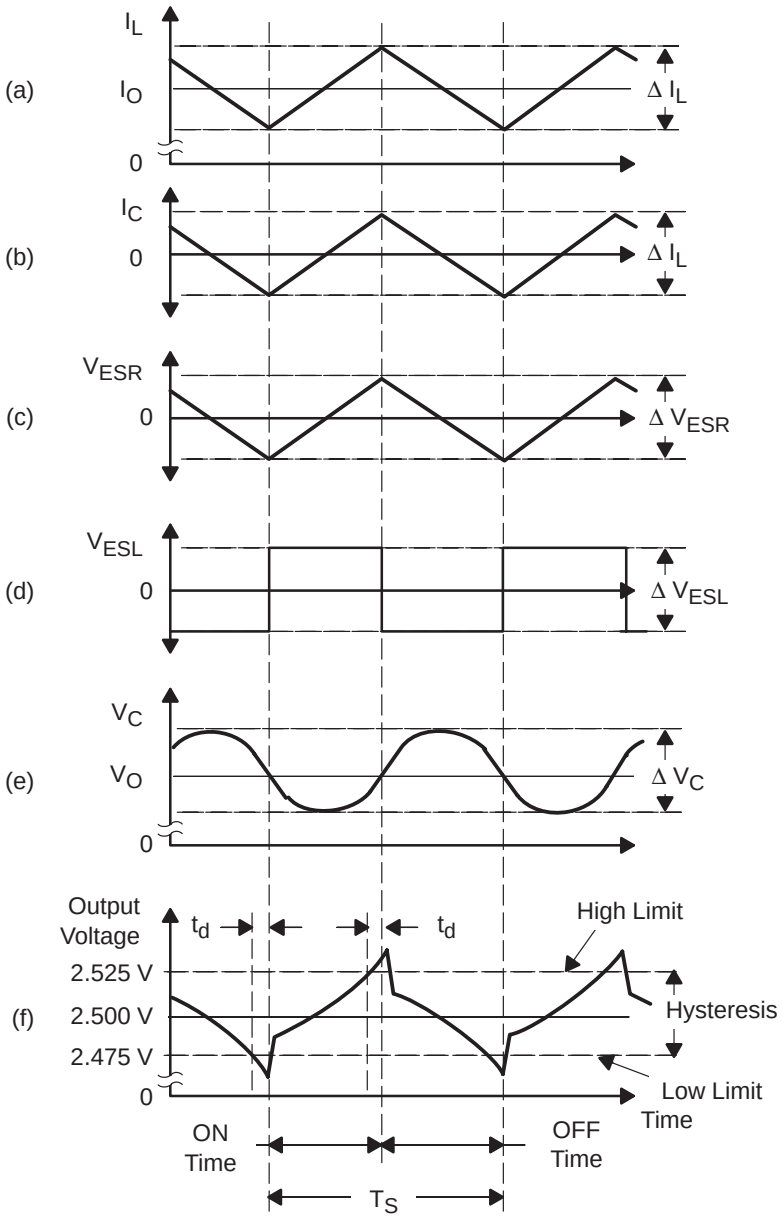


Figure 2–2 also shows the small but significant delay time, t_d, that is not the result of output capacitor characteristics. This delay covers the interval between the sensed output voltage reaching the internal hysteretic comparator trip point, and the output inductor current changing slope. Time delay, t_d, is due to internal comparator propagation delay, internal logic and drive circuit delays, and delays intrinsic to switching power MOSFETs from on to off or vice versa. For the purposes of this analysis, the delay is considered constant.

The delay causes the output voltage ripple to be slightly higher than what is set by the controller. It also causes the switching frequency to be slightly lower than it would be with no delay. The delay however, can be taken into account during design and should present no surprises to the designer.

2.2.2.5 Converter Switching Frequency

Following the analytic approach of the previous section, the expression for the converter switching frequency is given by:

$$f_{sw} = \frac{\left(V_I - V_O\right) \cdot V_O \cdot \left(R_{ESR} \cdot C_O - t_d\right)}{\left(V_I \cdot R_{ESR} \cdot t_d + V_{Hysteresis} \cdot L_O - L_{ESL} \cdot V_I\right) \cdot V_I \cdot C_o} \qquad \text{EQ 2–1}$$

Although the equation looks formidable, it is easily implemented in an Excel spreadsheet, MathCad file, or any of several other analysis tools.

To verify the accuracy of the equation, measurements were made on the output capacitor and output inductor to determine the actual component and parasitic values. Also measured were t_d, total delays, and hysteresis of the internal comparator, $V_{Hysteresis}$. The variables and measured values are:

V_I = Input voltage – *3.5 V – 6.5 V*

V_O = Output voltage – *2.5 V*

R_{ESR} = Output capacitor ESR – *6.1 mΩ*

$V_{Hysteresis}$ = Output ripple setting – *30 mV*

L_{ESL} = Output capacitor ESL – *5.9 nH*

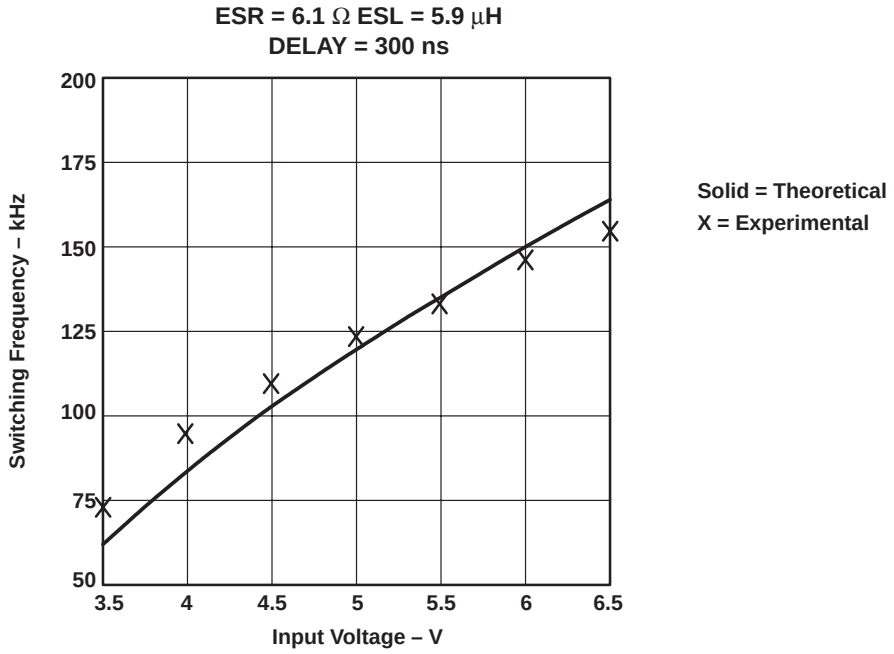
L_O = Output inductance – *2.67 µH*

C_O = Output capacitance – *820 µF*

The effect of parasitic resistances, such as MOSFET $R_{DS(on)}$ or output inductor dc resistance, is not included in the above equation. In an efficient converter, these parasitics are negligible.

Figure 2–3 shows a graph of the equation using actual component values and parasitics used in the SLVP105 (2.5 V) EVM. The graph also includes experimental data taken to verify the accuracy of the equation. The experimental data points are shown as *X*s in the graph.

Figure 2–3. Converter Switching Frequency vs. Input Voltage



2.2.2.6 Output Inductance

In any buck converter, for a given operating point, the output inductance governs the peak-to-peak amplitude and the slope (di/dt) of the inductor ripple current. Once the output ripple voltage is set (by setting VHYST), the output inductance (plus component parasitics) governs the converter switching frequency. The inductor value also affects the response time to output load transients. A higher inductance allows the output voltage to sag more before recovering. On the other hand, too low a value produces excessive ripple current in the output capacitors. Therefore, the inductor value is fairly critical and should be stable over the expected load and temperature range.

The important factors to be considered when designing or selecting the inductor are its inductance, current capability, and dc resistance.

Given a desired switching frequency, an expression for the needed inductance can be obtained by solving the switching frequency equations for L_O to obtain:

$$L_O = \frac{\left(V_I - V_O\right) V_O \left(R_{ESR} \cdot C_O - t_d\right)}{V_I \cdot C_o \cdot f_{sw} \cdot V_{Hysteresis}} + \frac{V_I \cdot L_{ESL}}{V_{Hysteresis}} - \frac{V_I \cdot R_{ESR} \cdot t_d}{V_{Hysteresis}}$$

2.2.2.7 Power Switches

The TPS5625 controller can drive two N-channel power MOSFETs in a synchronous rectifier configuration. This design uses the Siliconix Si4410DY MOSFET, a device chosen for its low $R_{DS(on)}$ of 13.5 mΩ and drain-to-source breakdown voltage rating of 30 V.

Power dissipation for the switching MOSFETs, Q1 and Q2, which includes both conduction and switching losses, is given by:

$$P_{DQ1} = \left(I_O^2 \times R_{DS(on)} \times D\right) + \left(0.5 \times V_i \times I_O \times t_{r+f} \times f_{sw}\right)$$

$$P_{DQ2} = \left(I_O^2 \times R_{DS(on)} \times (1-D)\right) + \left(0.5 \times V_i \times I_O \times t_{r+f} \times f_{sw}\right)$$

An example MOSFET power dissipation calculation for Q1 and Q2 is shown below with the following assumptions:

The total switching time, t_{r+f} = 100 ns,

An $R_{DS\ (on)}$ high temperature adjustment factor = 1.4,

A 40°C maximum ambient temperature,

V_I = 5 V, V_O = 2.5 V, and I_O = 8 A then :

$$P_{DQ1} = 8^2 \times (0.0135 \times 1.4) \times 0.54 + 0.5 \times 5 \times 8 \times 100 \times 10^{-9} \times 125\ kHz = 0.65 + 0.25 = 0.90\ W$$

$$P_{DQ2} = 8^2 \times (0.0135 \times 1.4) \times 0.46 + 0.5 \times 5 \times 8 \times 100 \times 10^{-9} \times 125\ kHz = 0.56 + 0.25 = 0.81\ W$$

The thermal impedance of these devices, $R_{\theta JA}$ = 90°C/W for FR-4 with 2-oz. copper and a one-inch-square pattern, thus:

$$T_{JQ1} = T_A + \left(R_{\theta JA} \times P_D\right) = 40 + (90 \times 0.90) = 121°C$$

$$T_{JQ2} = T_A + \left(R_{\theta JA} \times P_D\right) = 40 + (90 \times 0.81) = 113°C$$

Conduction losses are comparable to switching losses in this application, but may not be in others. It is good design practice to check power dissipation at the extreme limits of input voltage to find the worst case.

2.2.2.8 Snubber Network

A snubber network is usually needed to suppress the ringing at the node where the power switches and output inductor connect. This is especially important in this design because this signal is used as the input to the LOHIB pin. The snubber design is very dependent on PWB layout and component parasitics, but as a starting point, select a snubber capacitor with a value that is 4 to 10 times larger than the estimated capacitance at this node. The power dissipated in the snubber resistor is directly proportional to this capacitor value, so this value should be chosen with care. After experimental evaluation, a capacitor value of 0.01 µF was selected with a resistor value of 2.7 Ω. One important design constraint is that the resistor value should be chosen so that the snubber RC time constant times 3 is less than the minimum on time or minimum off time of the power switches. This allows the snubber capacitor to fully charge and discharge during each portion of the switching period.

Chapter 3

Test Results

This chapter shows the test setups used, and the test results obtained, in designing the SLVP10x EVMS.

Topic **Page**

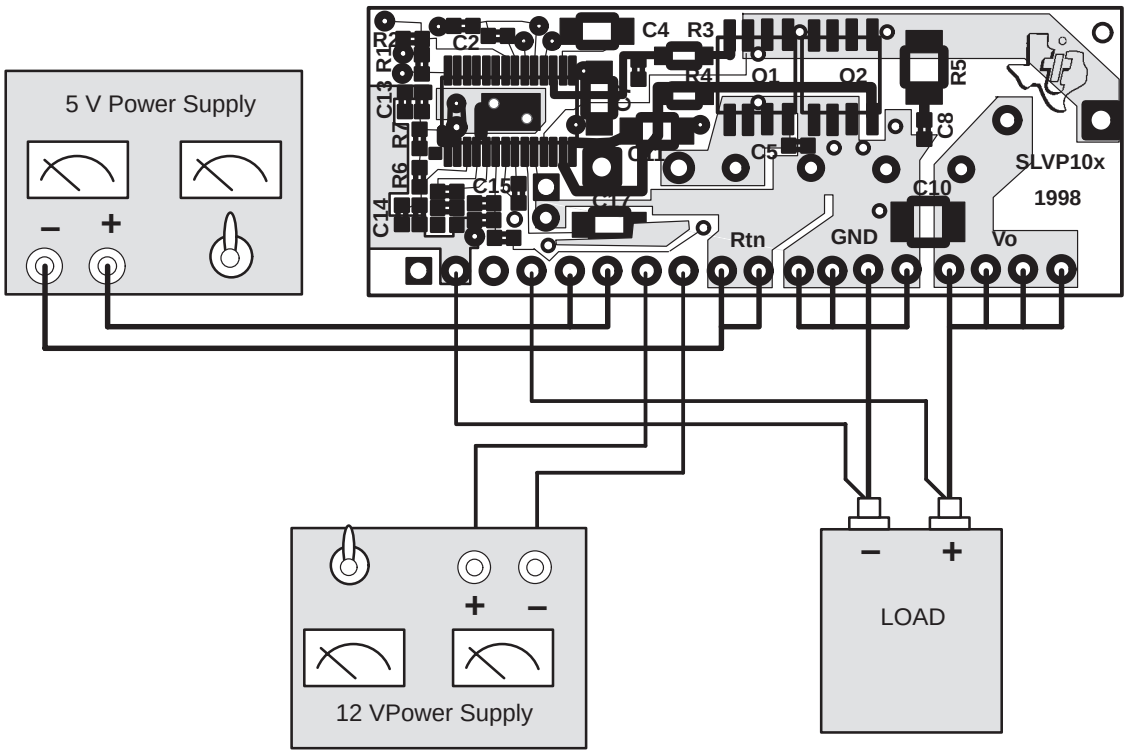
3.1 Test Setup

Follow thes steps for initial power-up of the SLVP105:

1) Connect an electronic load from Vout to PwrGND (J1-15, -16, -17, -18 to J1-11, -12, -13, -14) adjusted to draw approximately 1 A at 2.5 V. The exact current is not critical; any nominal current is sufficient. A fixed resistor can also be used in place of the electronic load. The output current drawn by the resistor is $I_O = \frac{2\ 5\ V}{R}$ Amps where R is the value of the load resistor. The resistor power rating, P_R should be at least $\frac{2.5^2}{R} \times 2$ Watts. Connect the sense lines from the load to VsenseH and VsenseL (J1-4 and J1-2).
2) Connect a 12-V lab power supply to the 12-V input (J1-7 referenced to PwrGND, J1-8) of the SLVP105. A current limit set for 20 mA should be adequate for the controller's power requirements.
3) Connect another lab power supply to the 5 V DC input of the SLVP105 (J1-5, -6 referenced to Return, J1-9, -10). Verify that the current limit is set for at least 2 A and that it is set to 0 V.
4) Turn on the 12-V lab supply. Turn on the 5-V power supply and ramp the input voltage up to 5 V. Once proper operation is verified, this order is not important.
5) Verify that the SLVP105 output voltage (measured at the module output pins) is 2.5 V $\pm$ 0.025 V.
6) For subsequent testing, ensure the lab supply output current capacity and current limit are at least 7 A so that the SLVP105 can be operated at maximum load of 8 A.
7) For initial power-up of the other converters, replace any reference to 2.5 V in the above discussion with a reference to the appropriate output voltage.
8) Refer to Chapter 3 for selected typical waveforms and operating conditions for verification of proper module operation.

Figure 3–1 shows the SLVP105 test setup.

Figure 3–1. Test Setup



3.2 Test Results

Table 3–1 and Figures 3–2 to 3–12 show test results for the SLVP105.

Table 3–1. SLVP105 Efficiency and Load Regulation Data vs. Output Current

Vin [V]	Iin [A]	Vo [V]	Iout [A]	Losses [W]	Efficiency, %
5	0.038	2.4993	0	0.34	0
5	0.553	2.499	1	0.39	86.5
5	1.073	2.4986	2	0.49	91.1
5	1.61	2.4982	3	0.68	91.7
5	2.159	2.4978	4	0.93	91.5
5	2.723	2.4973	5	1.25	90.9
5	3.3.4	2.4966	6	1.66	90.0
5	3.909	2.496	7	2.20	88.8
5	4.53	2.4953	8	2.81	87.7

Note: Losses from 12 V (V_{CC}) input included in efficiency data

Figure 3–2. Test Setup

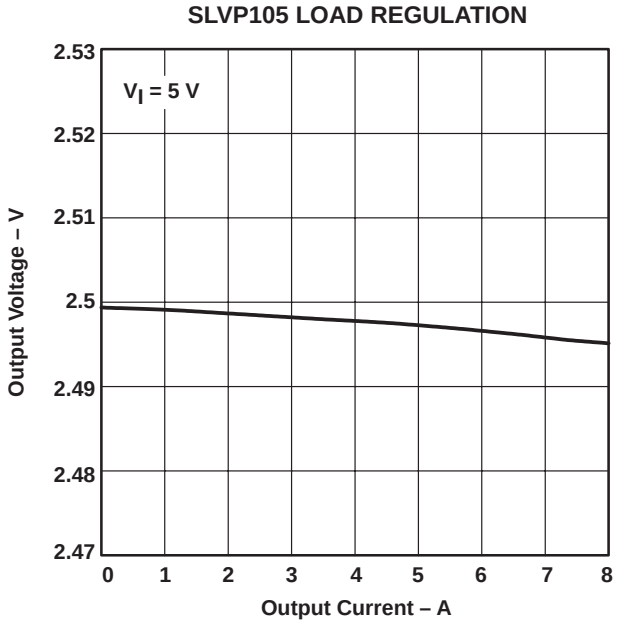


Figure 3–3. SLVP105 Efficiency vs. Load

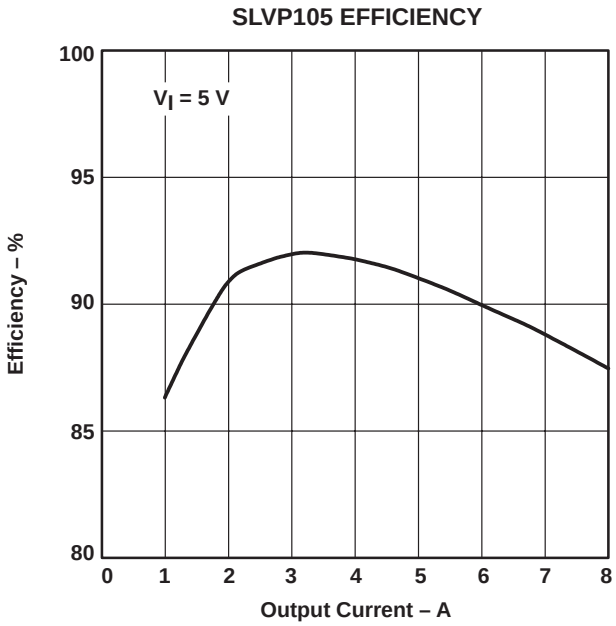


Figure 3–4. SLVP105 No Load (0 A) Output Voltage Ripple

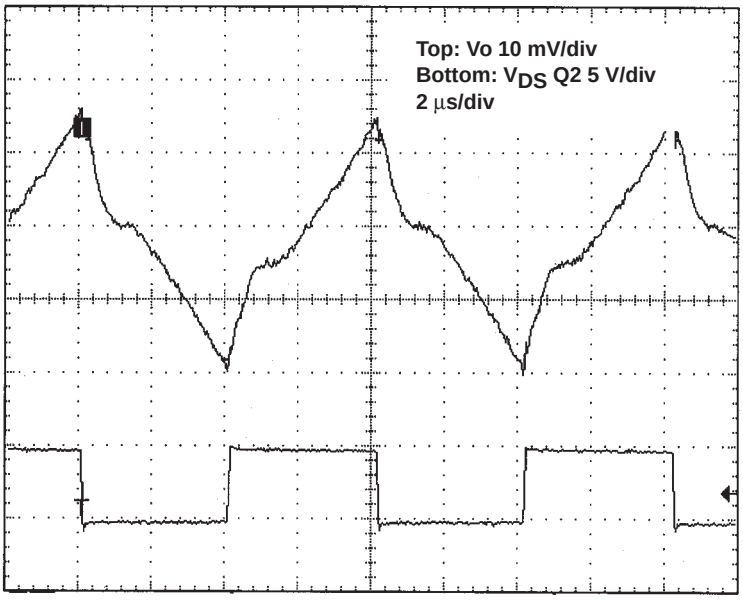


Figure 3–5. SLVP105 Full Load (8 A) Output Voltage Ripple

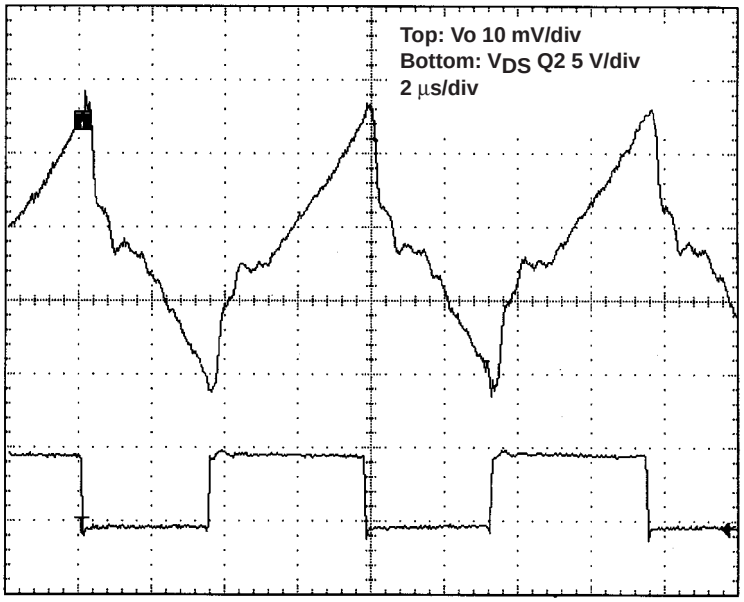


Figure 3–6. SLVP105Full Load (8 A) Startup with 5 V Input Application

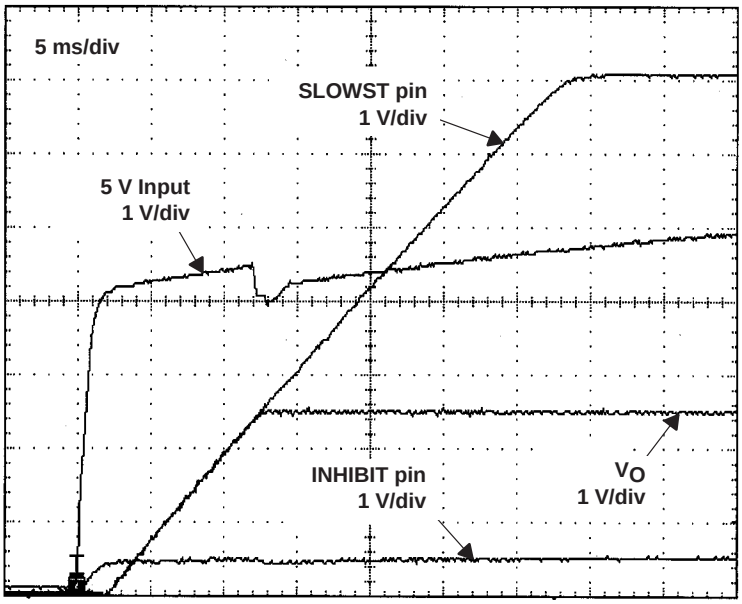


Figure 3–7. SLVP105 Startup with INHIBIT Applicaltion

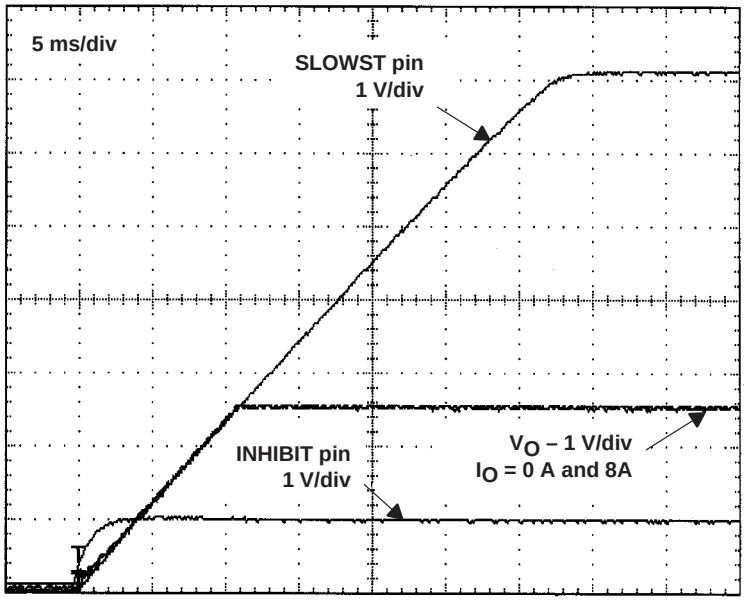


Figure 3–8. SLVP105 Startup with V_{CC} Application

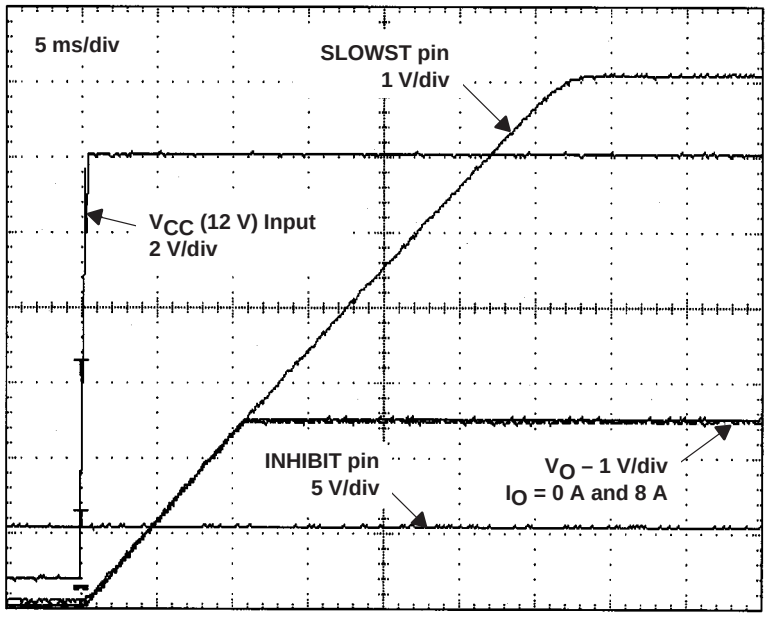


Figure 3–9. SLVP105 Shutdown with INHIBIT Removal

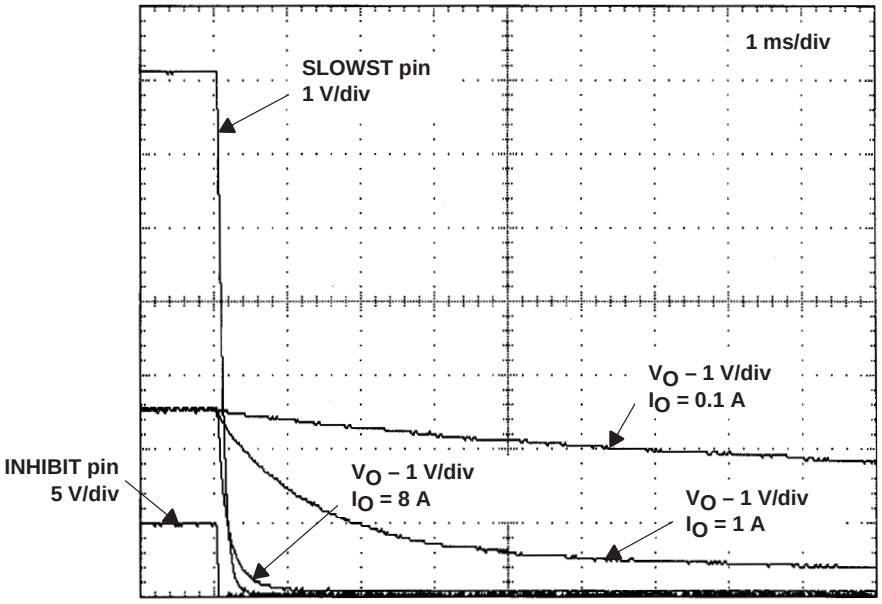


Figure 3–10. SLVP105 Shutdown with V_{CC} Removal

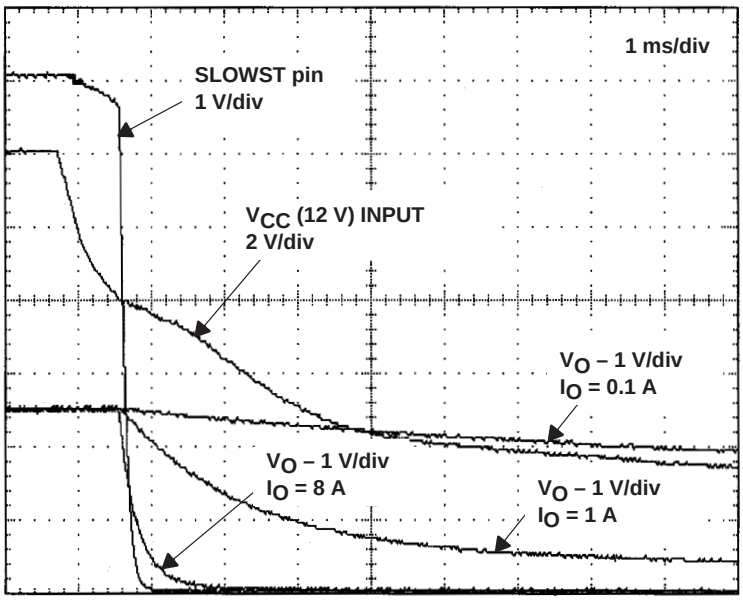


Figure 3–11. SLVP105 Application of Load Transient

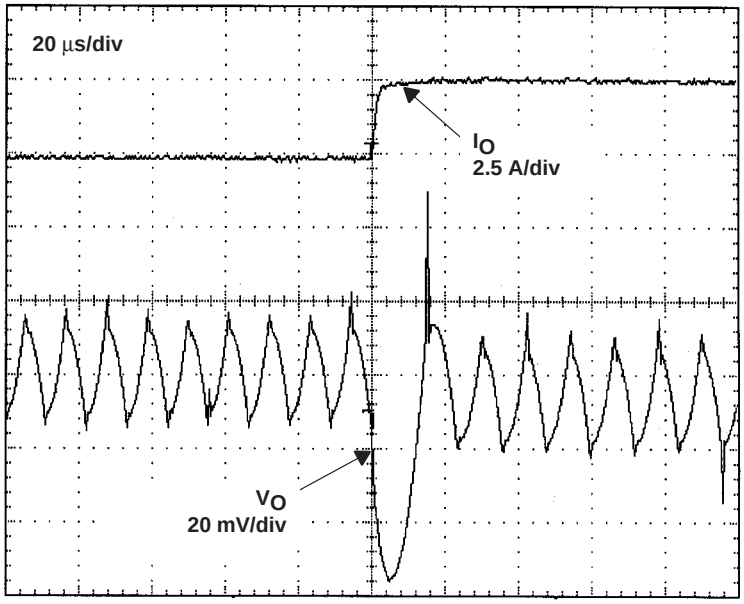


Figure 3–12. Removal of Load Transient