User's Guide

SLVU433–February 2011

TPS53128EVM-620

The TPS53128EVM-620 Evaluation Module presents an easy-to-use reference design for a common dual output power supply using the TPS53128 controller in cost sensitive applications.

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1 Introduction

1.1 Description

The TPS53128EVM-620 evaluation board provides the user with a convenient way to evaluate the TPS53128 Dual D-CAP2™ Mode Control Step-Down Controller in a realistic cost-sensitive application. Providing both a low core-type 1.05-V and I/O type 1.8-V output at up to 4 A from a loosely regulated 12-V (8-V to 22-V) source, the TPS53128EVM-620 includes switches and test points to assist a user in evaluating the performance of the TPS53128 controller in their application.

1.2 Application

- Digital television
- Set-top box
- DSL and cable modems
- Cost-sensitive digital consumer products

1.3 Features

- 8-V to 22-V input
- 1.05-V and 1.8-V output
- Up to 4 A per channel output
- 350-kHz psudeo-fixed frequency D-CAP2™ mode control
- Independent enable switches for power-on/power-off testing

2 Electrical Performance Specifications

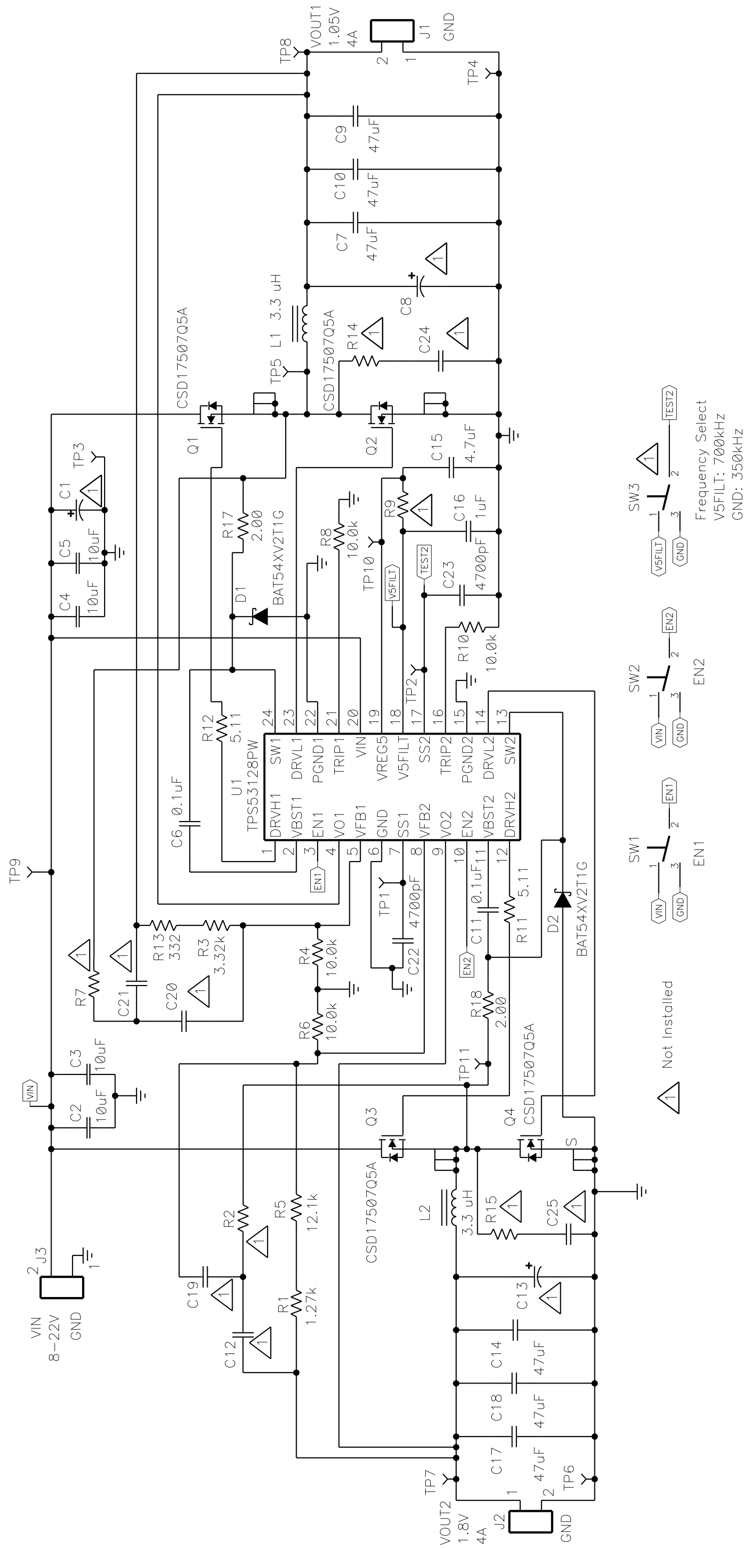
Table 1. TPS53128EVM-620 Electrical and Performance Specifications

Parameter		Notes and Conditions	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input Voltage		8	12	22	V
I_{IN}	Input Current	V_{IN} = 12 V, I_{OUT1} = 4 A, I_{OUT2} = 4 A	–	1.2	1.5	A
	No Load Input Current	V_{IN} = 12 V, I_{OUT} = 0 A	–	20	–	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 4 A	4.0	4.2	4.5	V
OUTPUT CHARACTERISTICS						
V_{OUT1}	Output Voltage 1	V_{IN} = 12 V, I_{OUT1} = 2 A	–	1.05	–	V
	Line Regulation	V_{IN} = 8 V to 22 V	–	–	1%	
	Load Regulation	I_{OUT1} = 0 A to 4 A	–	–	1%	
V_{OUT1_rip}	Output Voltage Ripple	V_{IN} = 12 V, I_{OUT2} = 4 A	–	-	30	mVpp
I_{OUT1}	Output Current 1	V_{IN} = 8 V to 22 V	0		4	A
V_{OUT2}	Output Voltage 2	V_{IN} = 12 V, I_{OUT2} = 2 A	–	1.80	–	V
	Line Regulation	V_{IN} = 8 V to 22 V	–	–	1%	

Table 1. TPS53128EVM-620 Electrical and Performance Specifications (continued)

Parameter		Notes and Conditions	MIN	TYP	MAX	UNIT
	Load Regulation	I_{OUT2} = 0 A to 4 A	–	–	1%	
V_{OUT2_rip}	Output Voltage Ripple	V_{IN} = 12 V, I_{OUT2} = 4 A	–	–	30	mVpp
I_{OUT2}	Output Current 2	V_{IN} = 8 V to 22 V	0		4	A
SYSTEMS CHARACTERISTICS						
F_{SW}	Switching Frequency		200	350	400	kHz
ηpk1	Peak Efficiency of Output 1	V_{IN} = 12 V	–	87%	–	
η1	Full Load Efficiency of Output 1	V_{IN} = 12 V, I_{OUT1} = 4 A	–	85%	–	
ηpk2	Peak Efficiency of Output 2	V_{IN} = 12 V	–	91%	–	
η2	Full Load Efficiency of Output 2	V_{IN} = 12 V, I_{OUT2} = 4 A	–	90%	–	

3 Schematics



NOTE: For Reference Only, See Table 3 for Specific Values.

Figure 1. TPS53128EVM-620 Schematic.

4 Connector and Test Point Descriptions

4.1 Enable Switches (SW1 and SW2)

TPS53128EVM-620 includes independent enable switches for each of the two outputs. When the switch is in the DIS position, the channel is disabled and discharged per the TPS53128's internal discharge characteristics.

To enable V_{OUT1}, place SW1 in the EN position. To enable V_{OUT2}, place SW2 in the EN position.

4.2 Switching Frequency Select Switch (SW3)

TPS53128EVM-620 does not populate SW3. When using TPS53128EVM-620 to evaluate the TPS53126 controller in the TSSOP package, SW3 can be populated to allow selection of the TPS53126 switching frequency between 350 kHz and 700 kHz.

4.3 Test Point Descriptions

Table 2 lists the test points, their labels, uses, and where additional information is located.

Table 2. TPS53128EVM-620 Test Points Description

Test Point	Label	Use	Section
TP1	SS1	Monitor Channel 1 Soft-Start Voltage	Section 4.3.4
TP2	SS2	Monitor Channel 2 Soft-Start Voltage	Section 4.3.4
TP3	GND	Ground for Input Voltage	Section 4.3.1
TP4	GND	Ground for Channel 1 Output Voltage	Section 4.3.2
TP5	SW1	Monitor Switching Node for Channel 1	Section 4.3.5
TP6	GND	Ground for Channel 2 Output Voltage	Section 4.3.3
TP7	VOUT2	Monitor Output Voltage for Channel 2	Section 4.3.3
TP8	VOUT1	Monitor Output Voltage for Channel 1	Section 4.3.2
TP9	VIN	Monitor Input Voltage	Section 4.3.1
TP10	VREG5	Monitor Output of VREG5 Regulator	Section 4.3.6
TP11	SW2	Monitor Switching Node for Channel 2	Section 4.3.5

4.3.1 Input Voltage Monitoring (TP3 and TP9)

TPS53128EVM-620 provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connectors. Measure all input voltage between TP9 and TP3. To use TP9 and TP3, connect a voltmeter positive terminal to TP9 and negative terminal to TP3.

4.3.2 Channel 1 Output Voltage Monitoring (TP4 and TP8)

TPS53128EVM-620 provides two test points for measuring the voltage generated at the VOUT1 output by the module. This allows the user to measure the actual output voltage without losses from output cables and connectors. Measure all dc output voltage measurements between TP8 and TP4. To use TP8 and TP4, connect a voltmeter positive terminal to TP8 and negative terminal to TP4.

For output ripple measurements, TP8 and TP4 allow a user to limit the ground loop area by using the tip and barrel measurement technique shown in Figure 2.

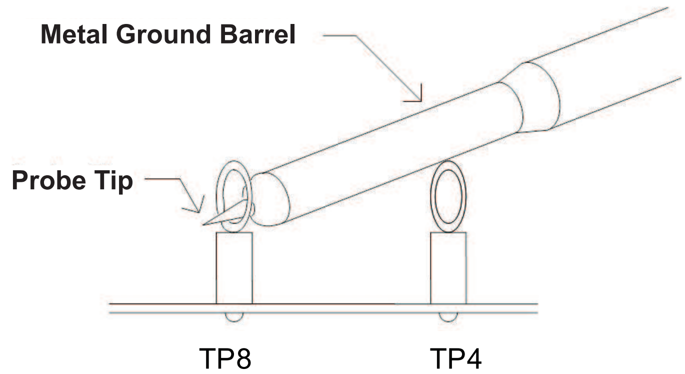


Figure 2. Tip and Barrel Measurement for Output Voltage Ripple

4.3.3 Channel 2 Output Voltage Monitoring (TP6 and TP7)

TPS53128EVM-620 provides two test points for measuring the voltage generated at the V_{OUT2} output by the module. This allows the user to measure the actual output voltage without losses from output cables and connectors. Measure all dc output voltage between TP7 and TP6. To use TP7 and TP6, connect a voltmeter positive terminal to TP7 and negative terminal to TP6.

For output ripple measurements, TP7 and TP6 allow a user to limit the ground loop area by using the tip and barrel measurement technique shown in Figure 2.

4.3.4 Soft-Start Voltage Monitoring (TP1, TP2 and TP3)

TPS53128EVM-620 provides two test points for measuring the soft-start ramp voltages. TP1 monitors the soft-start ramp of Channel 1. TP2 monitors the soft-start ramp of Channel 2. To use TP1 or TP2, connect an oscilloscope probe between TP1 or TP2 and TP3.

4.3.5 Switching Node Monitoring (TP3, TP5 and TP11)

TPS53128EVM-620 provides two test points for measuring the switching node waveform voltages. TP5 monitors the switching node of Channel 1. TP2 monitors the switching node of Channel 2. To use TP5 or TP11, connect an oscilloscope probe between TP5 or TP11 and TP3.

4.3.6 5-V Regulator Output Monitoring (TP3 and TP10)

TPS53128EVM-620 provides a test point for measuring the output of the internal 5-V regulator. TP10 monitors the output voltage of the internal 5-V regulator. To use TP10, connect a voltmeter positive terminal to TP10 and negative terminal to TP3.

5 Test Setup

5.1 Equipment

5.1.1 Voltage Source

The input voltage source (V_{IN}) shall be a 0-V to 25-V variable dc source capable of supplying 3.0 Adc minimum.

5.1.2 Meters

A1: 0-Adc to 5-Adc, ammeter

V1: V_{IN}, 0-V to 25-V voltmeter

V2: V_{OUT1}, 0-V to 2-V voltmeter

V3: V_{OUT2}, 0-V to 2-V voltmeter

5.1.3 Loads

LOAD1: One output load is an electronic load set for constant current mode capable of 0 Adc to 4 Adc at 1.05 Vdc.

LOAD2: The other output load is an electronic load set for constant current mode capable of 0 Adc to 4 Adc at 1.8 Vdc.

5.1.4 Oscilloscope and Probe

The oscilloscope, analog or digital, must be set for ac-coupled measurement with 20-MHz bandwidth limiting. Use 20 mV / division vertical resolution, 1.0 µs / division horizontal resolution for output ripple voltage test.

Oscilloscope probes with exposed conductive ground barrels are recommended.

5.1.5 Recommended Wire Gauge

V_{IN} to J3 – The connection between the source voltage VIN and J1 of TPS53128EVM-620 can carry as much as 2 Adc. The minimum recommended wire size is AWG #16 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

J1 to LOAD1 and J2 to LOAD2 – The connection between J1 and LOAD1, and J2 and LOAD2 of TPS53128EVM-620 can carry as much as 4 Adc each. The minimum recommended wire size is AWG #14 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

5.1.6 Other Test Equipment

FAN – The TPS53128EVM-620 Evaluation Module includes components that can get hot to touch. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is recommended to reduce component temperatures when operating.

5.2 Recommended Setup

Figure 3 shows the recommended test setup to evaluate the TPS53128EVM-620. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses also are recommended.

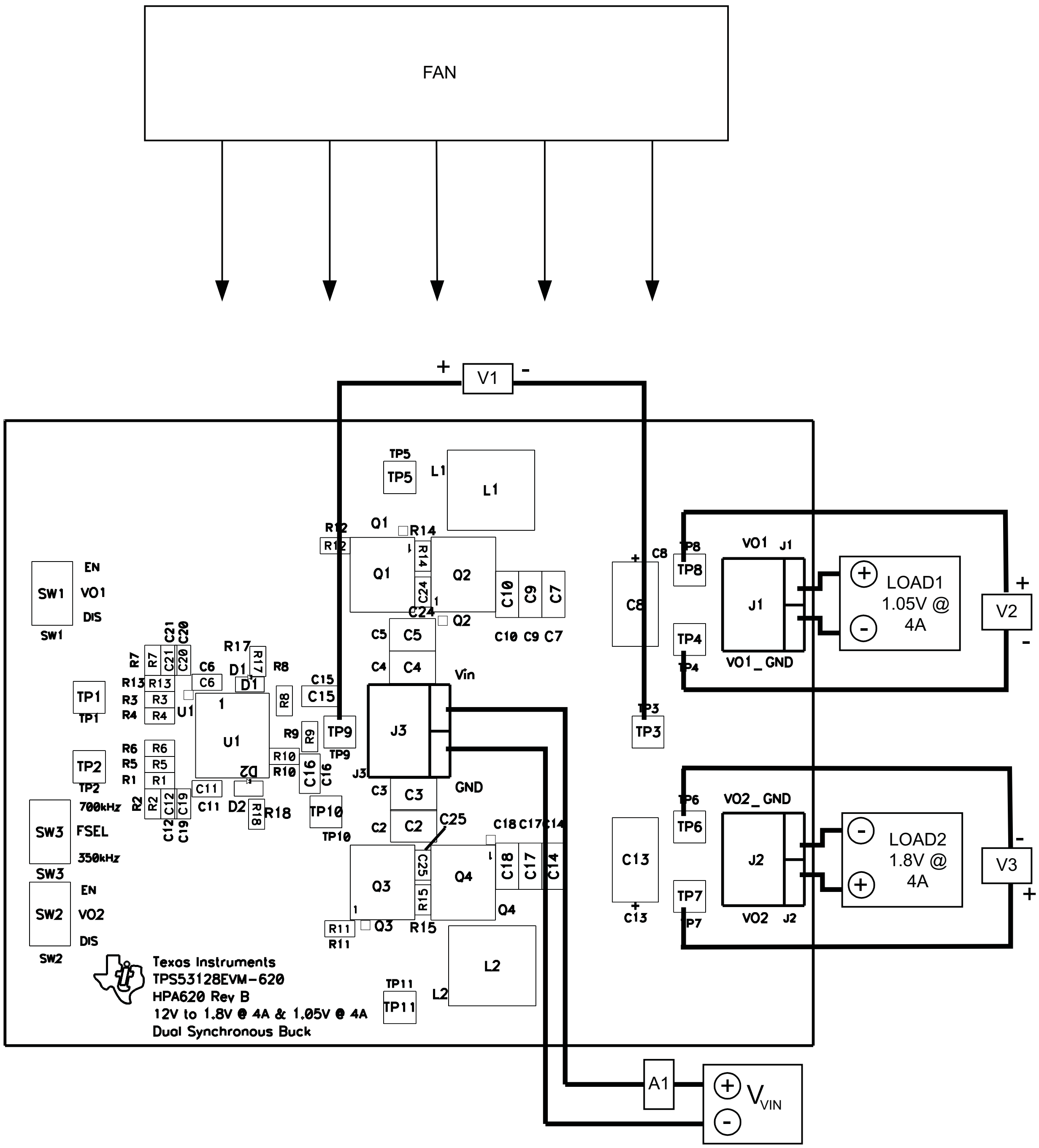


Figure 3. TPS53128EVM-620 Recommended Test Setup

6 Test Procedure

6.1 Start-up Procedure

1. Prior to connecting the dc input source V_{IN}, it is advisable to limit the source current from V_{IN} to 3.0 Adc maximum. Make sure V_{IN} is initially set to 0 V.
2. Ensure LOAD1 and LOAD2 are set to constant current mode to sink 0 A before V_{IN} is applied.
3. Verify SW1 and SW2 are in the desired position.
4. Place a fan as shown in Figure 3 and turn on, making sure air is flowing across the EVM.
5. Increase V_{IN} from 0 V to 12 Vdc.

6.2 Line/Load Regulation and Efficiency Measurement Procedure

1. Setup TPS53128EVM-620 per Section 5.2.
2. Start-up the TPS53128EVM-620 per Section 6.1.
3. Adjust V_{IN} to desired value between 8 Vdc and 22 Vdc.
4. Adjust LOAD1/LOAD2 to desired load between 0 A and 4 Adc.
5. Read input voltage, output voltage and input current from V1, V2/V3 and A1 respectively.
6. Shut down TPS53128EVM-620 per Section 6.4.

6.3 Output Ripple Voltage Measurement Procedure

1. Setup TPS53128EVM-620 per Section 5.2.
2. Start-up the TPS53128EVM-620 per Section 6.1.
3. Adjust V_{IN} to desired value between 8 Vdc and 22 Vdc.
4. Adjust LOAD1/LOAD2 to desired load between 0 A and 4 Adc.
5. Connect the oscilloscope probe to TP8 and TP4 for V_{OUT1}, or TP7 and TP6 for V_{OUT2} as shown in Figure 2.
6. Measure output ripple.
7. Shut down TPS53128EVM-620 per Section 6.4.

6.4 Shutdown Procedure

1. Set SW1 to DIS.
2. Set SW2 to DIS.
3. Decrease LOAD1 to 0 A and shut down LOAD1.
4. Decrease LOAD2 to 0 A and shut down LOAD2.
5. Decrease V_{IN} to 0 V and shut down V_{IN}.
6. Shut down the fan.

7 Performance Data and Typical Characteristic Curves

Figure 4 through Figure 11 present typical performance curves for the TPS53128EVM-620. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

7.1 Efficiency

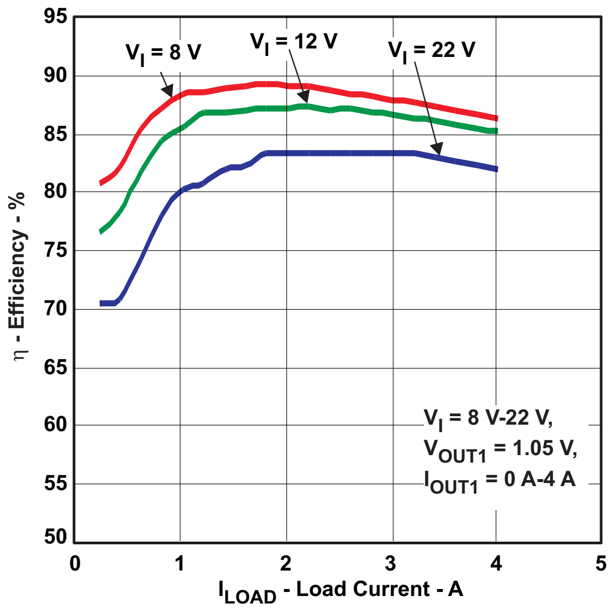


Figure 4. Efficiency vs Load

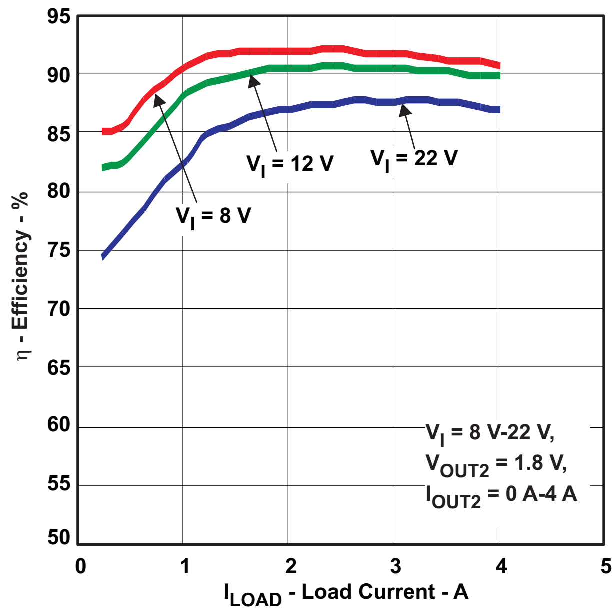


Figure 5. Efficiency vs Load

7.2 Line and Load Regulation

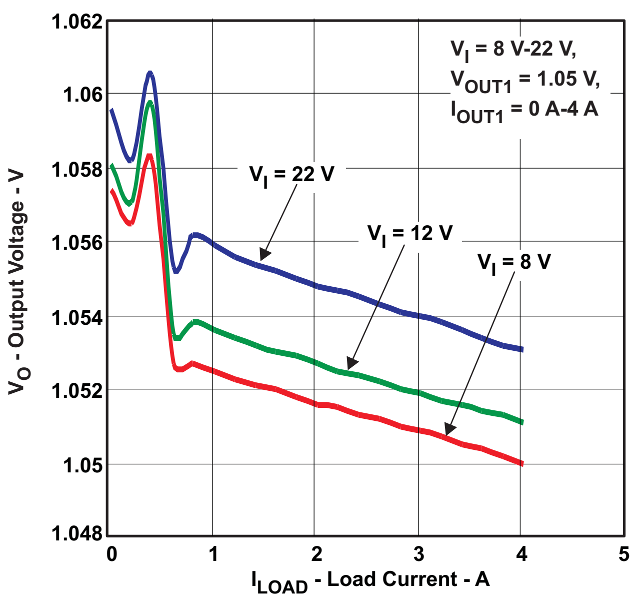


Figure 6. Output Voltage vs Load

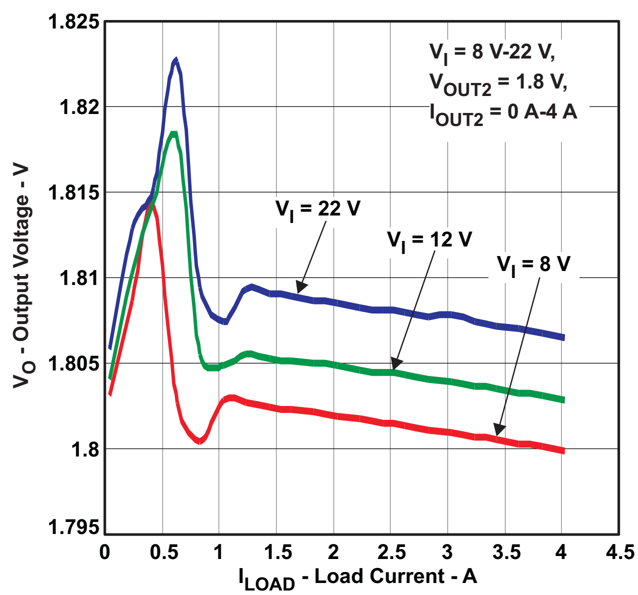


Figure 7. Output Voltage vs Load

7.3 Output Voltage Ripple

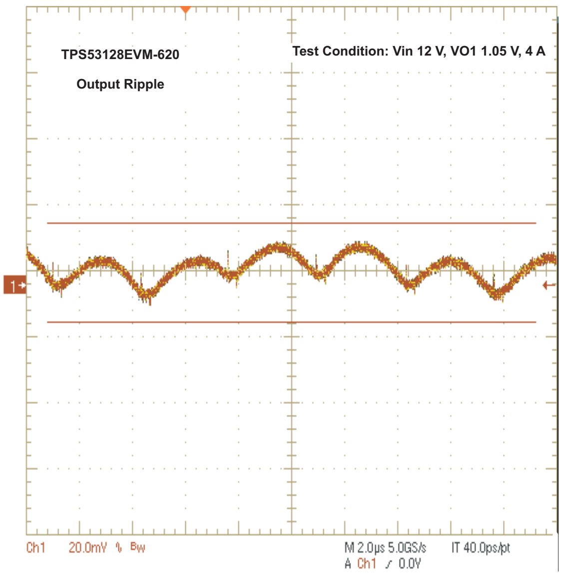


Figure 8. Output Voltage Ripple

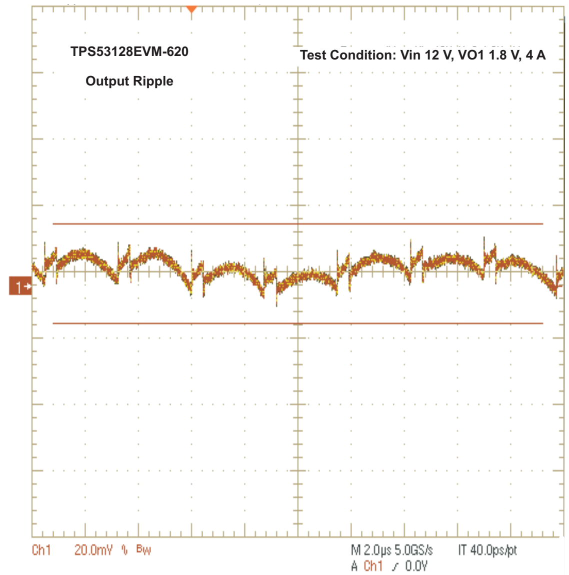


Figure 9. Output Voltage Ripple

7.4 Switch Node Waveforms

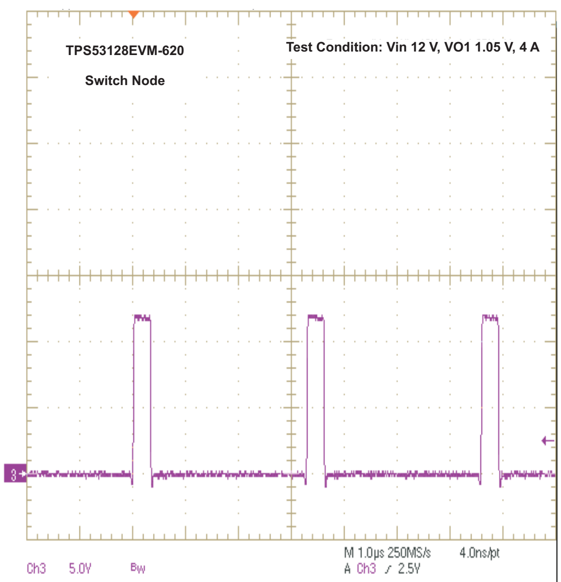


Figure 10. Switching Waveform

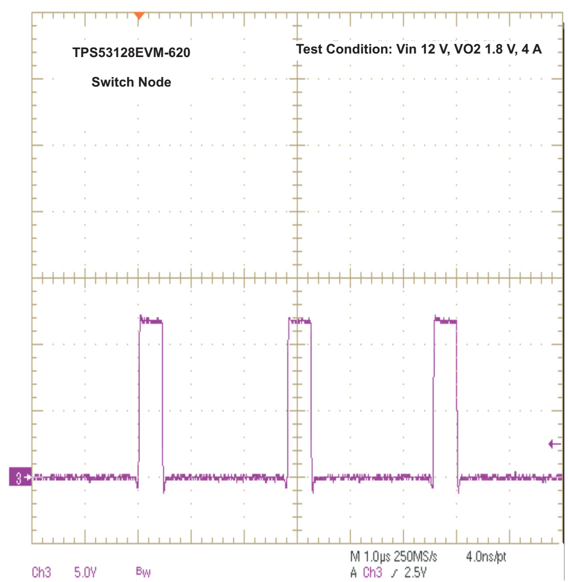


Figure 11. Switching Waveform

8 EVM Assembly Drawings and Layout

The following figures (Figure 12 through Figure 17) show the design of the TPS53128EVM-620 printed circuit board. The EVM has been designed using a 4-layer, 2-oz copper-clad circuit board of 3.5 inch by 2.7 inch to allow the user to easily view, probe and evaluate the TPS53128 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

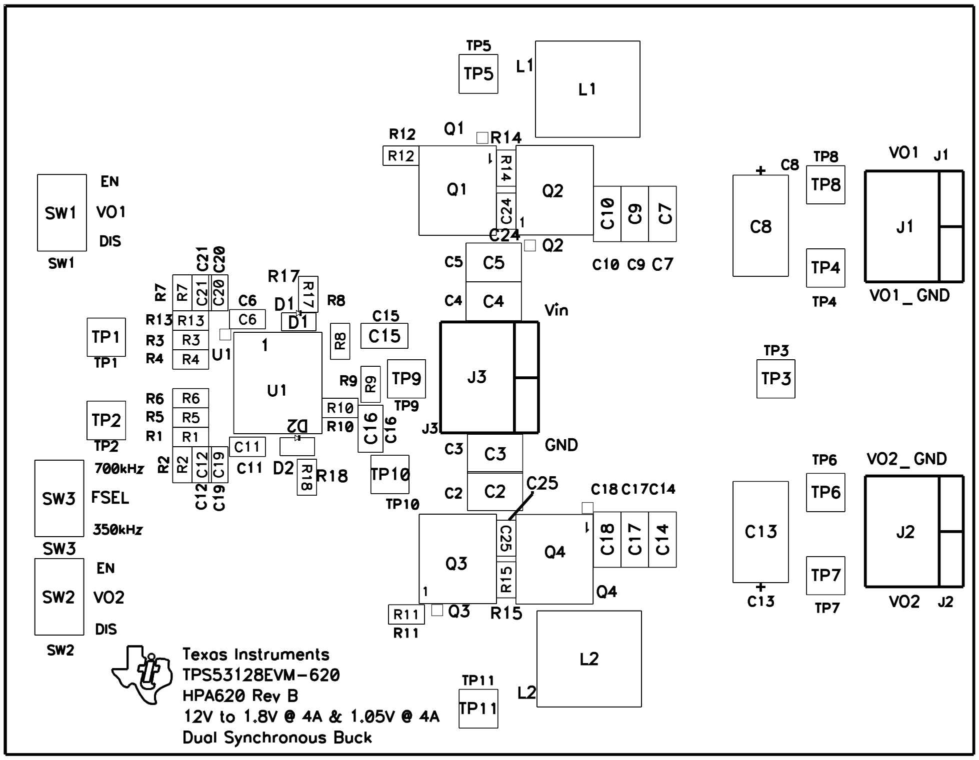


Figure 12. Top Assembly

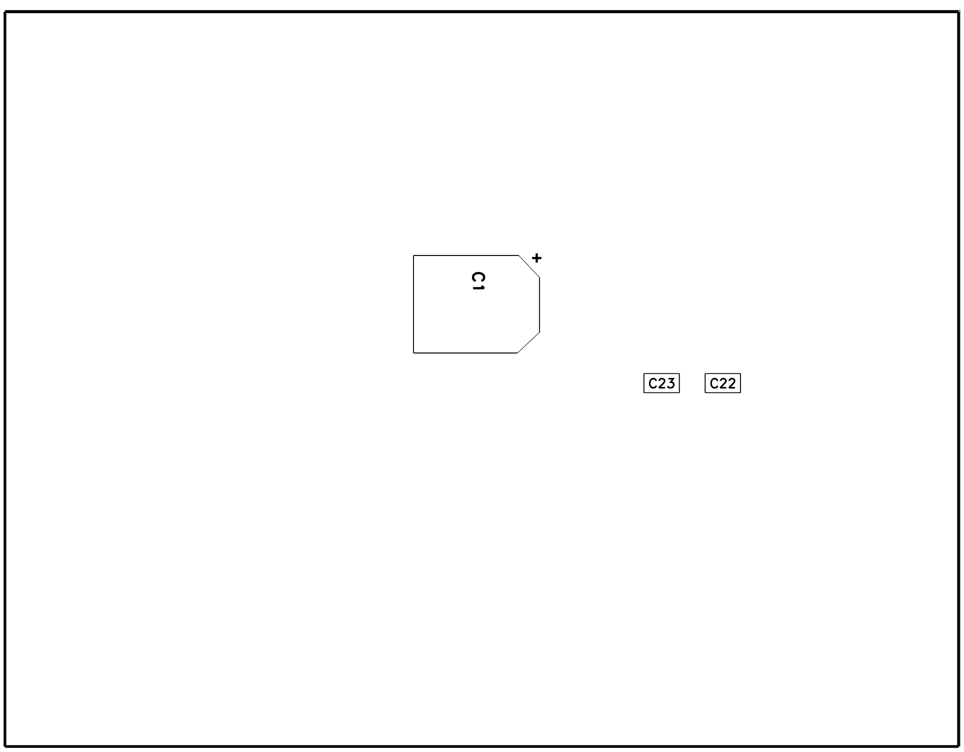


Figure 13. Bottom Assembly

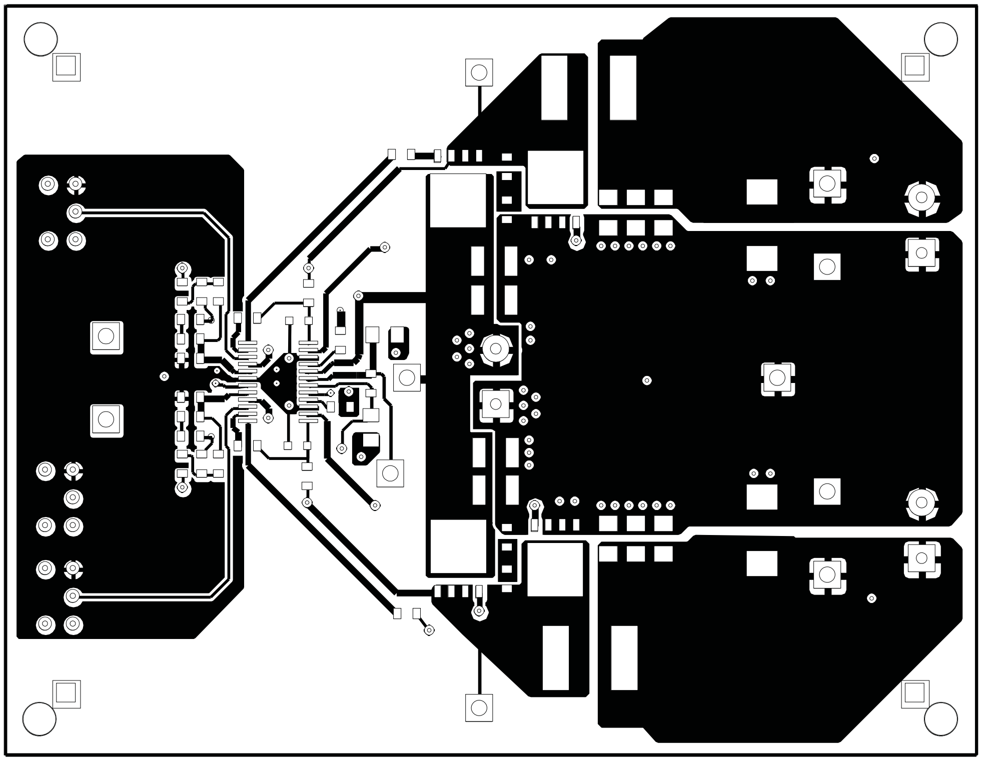


Figure 14. Top Layer

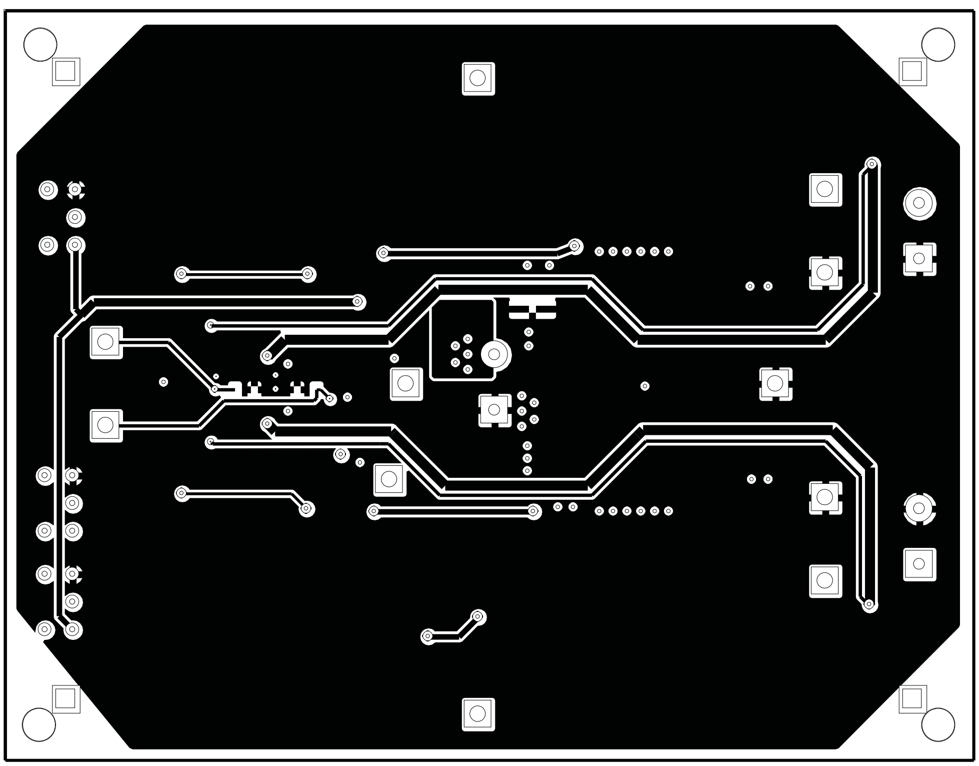


Figure 15. Bottom Layer

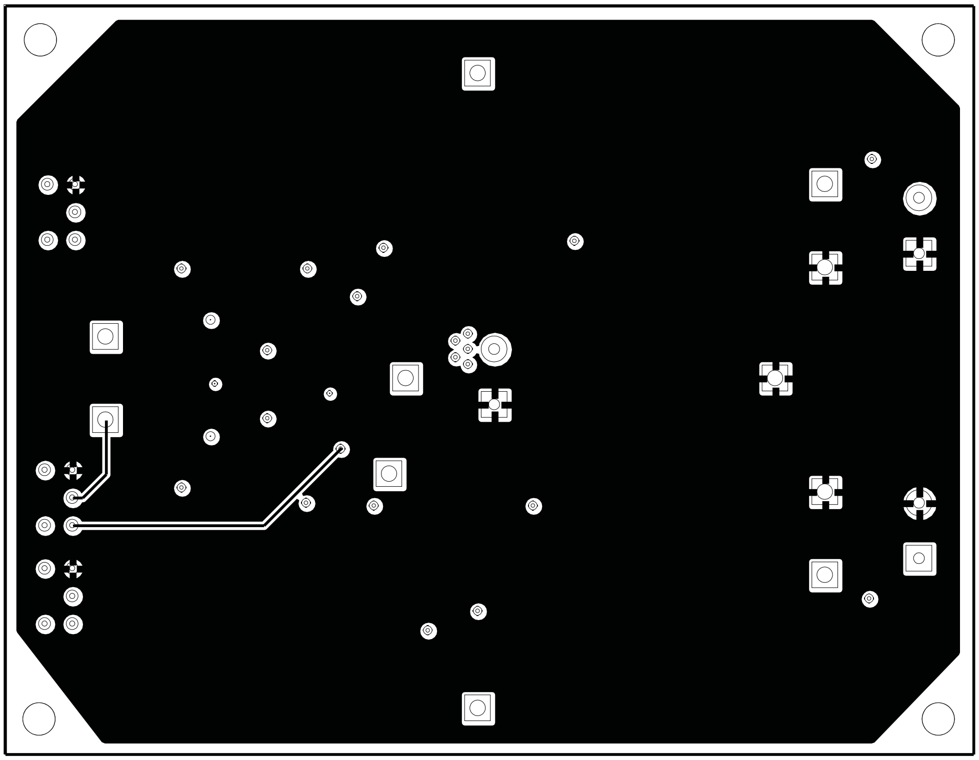


Figure 16. Internal Layer 1

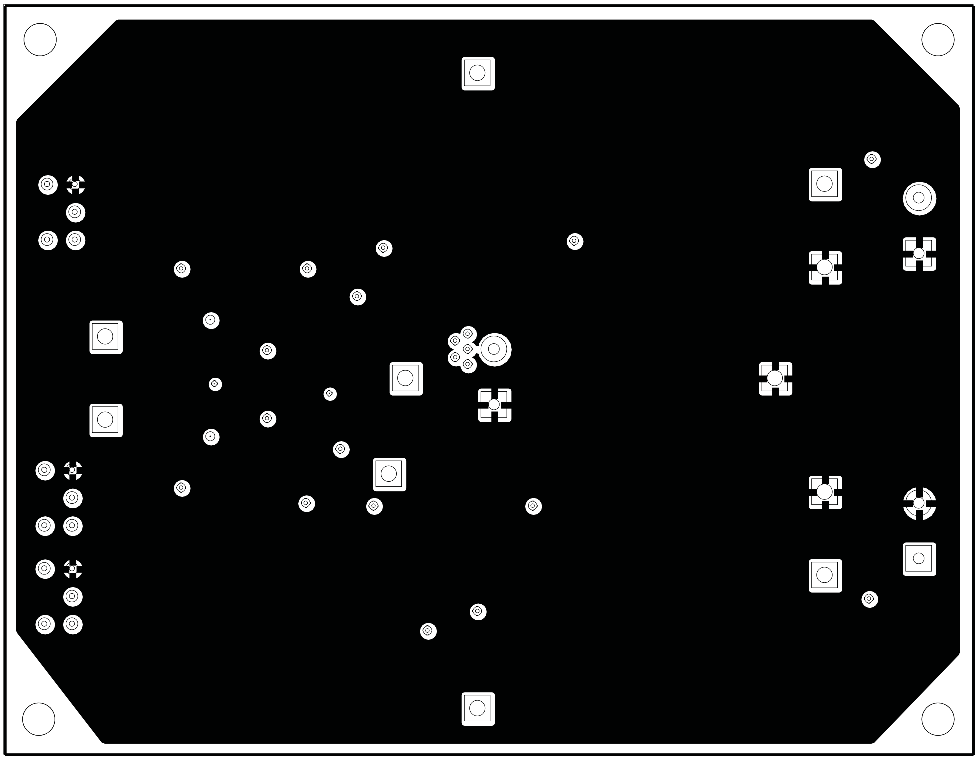


Figure 17. Internal Layer 2

9 Bill of Materials

Table 3 contains the Bill of Materials for TPS53128EVM-620. The reference designators reference the Schematic in Figure 1 and Assembly locations in Figure 12 and Figure 13. Components with a quantity of 0 listed are not populated on the PCB but are provided for reference.

Table 3. TPS53128EVM-620 Bill of Materials

Qty	RefDes	Value	Description	Size	Part Number	MFR
0	C1		Capacitor, Aluminum, 25V, 20%	0.328 x 0.390 inch	Std	Std
0	C12, C19, C20, C21		Capacitor, Ceramic	0603	Std	Std
1	C15	4.7uF	Capacitor, Ceramic, 10V, X5R, 20%	0805	Std	Std
1	C16	1uF	Capacitor, Ceramic, 16V, X5R, 20%	0805	Std	Std
4	C2, C3, C4, C5	10uF	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
2	C22, C23	4700pF	Capacitor, Ceramic, Low Inductance, 16V, X7R, 20%	0603	Std	Std
0	C24, C25		Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	C6, C11	0.1uF	Capacitor, Ceramic, 50V, X5R, 10%	0603	Std	Std
6	C7, C9, C10, C14, C17, C18	47uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	Std	Std
0	C8, C13	330uF	Capacitor, PXE, 4.0V, 15 milliohm, 20%	7343 (D)	APXE4R0ARA331MF61G	NIPPON CHEMI-CON
2	D1, D2	BAT54XV2T1G	Diode, Schottky, 200 mA, 30 V	SOD523	BAT54XV2T1G	On Semi
3	J1, J2, J3	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
2	L1, L2	3.3 uH	Inductor, SMT Chip Coil, ±30%	8 x 8 mm	LQH88PN3R3N38	Murata
4	Q1, Q2, Q3, Q4	CSD17507Q5A	MOSFET, N-Chan, 30V, 65A, 11.8 milliohm	QFN-8 POWER	CSD17507Q5A	TI
1	R1	1.27k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	R10, R4, R6, R8	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R11, R12	5.11	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R13	332	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R14, R15		Resistor, Chip, 1/8W, 5%	0603	Std	Std
2	R17, R18	2.00	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R2, R7, R9		Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	3.32k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	12.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	SW1, SW2	G12AP-RO	Switch, ON-ON Mini Toggle	0.28 x 0.18"	G12AP-RO	Nikkai
0	SW3	G12AP-RO	Switch, ON-ON Mini Toggle	0.28 x 0.18"	G12AP-RO	Nikkai
4	TP1, TP2, TP5, TP11	5012	Test Point, White, Thru Hole	0.125 x 0.125 inch	5012	Keystone
1	TP10	5013	Test Point, Orange, Thru Hole	0.125 x 0.125 inch	5013	Keystone
3	TP3, TP4, TP6	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
2	TP7, TP8	5014	Test Point, Yellow, Thru Hole	0.125 x 0.125 inch	5014	Keystone
1	TP9	5010	Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
1	U1	TPS53128PW	IC, Dual Synchronous Step-Down Controller For Low-Voltage Power Rails	TSSOP	TPS53128PW	TI
1	–		PCB, 2.70" x 3.50" x 0.063" FR-4	2.7" x 3.5"	HPA620	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8 V to 22 V and the output voltage range of 1.05 V and 1.8 V (up to 4 A max per output).

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 40° C. The EVM is designed to operate properly with certain components above 40° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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