TPS40071 Step Down Converter Delivers 10 A From 5-V to 12-V Bus Voltages

User’s Guide

EVM IMPORTANT NOTICE (CATEGORY B)

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It is important to operate this EVM within the maximum input voltage ranges of 4.75 V to 14 V, and an output voltage range given in Table 2..

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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TPS40071 Step Down Converter Delivers 10 A From 5-V to 12-V Bus Voltages

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System Power

ABSTRACT

The TPS40071EVM−001 evaluation module (EVM) is a synchronous buck converter operating from an input bus voltage ranging from 5 V to 12 V, utilizing Predictive Gate Drive™ (PGD) to efficiently deliver 1.8 V at up to 10 A of load current.

Contents

1 Introduction

The TPS40071EVM−001 evaluation module (EVM) is a synchronous buck converter which utilizes Predictive Gate Drive™ (PGD) to maximize conversion efficiency by minimizing the body diode conduction loss. The use of the TPS40071 midrange input synchronous buck controller allows the EVM to deliver 10 A from a bus voltage ranging from 5 V to 14 V. The output voltage is originally set to 1.8 V, but can also be configured to provide 1.2 V to 3.3 V at a load current up to 10 A by changing one surface mount resistor.

2 Description

The TPS40070/1 synchronous buck controller family offers a variety of user programmable functions including switching frequency, soft start, high side current limit, UVLO and external compensation. The controller operates with fixed frequency voltage mode control with an input voltage feed forward control input which improves performance in applications which have a variable input source. The TPS40071 is selected in the EVM because it operates in source-sink mode over the entire operating range.

The TPS40071 incorporates internal gate drivers for external N-channel MOSFETs in the high side switch and low side synchronous rectifier locations. The MOSFET drivers utilize TI’s proprietary Predictive Gate Drive™ technique which works to minimize the body diode conduction interval to reduce undesired power loss. The PowerPAD™ package allows the regulator bias power and the gate drive power to be safely dissipated without raising the junction an excessive amount. The high side current limit/short circuit protection senses the voltage drop across the top side MOSFET and compares it to a programmable reference to terminate output pulses on a pulse by pulse basis.

The TPS40071EVM−001 highlights the small size, high efficient solutions that can be attained using the TPS40071 controller. This user guide provides the collateral necessary to evaluate the TPS40071 in a typical application. The collateral includes the schematic, list of materials, test setup, assembly drawings, and PCB artwork.

The TPS40071EVM−001 offers the following performance features:

- Operates continuously over a 4.75-V to 14-V input range
- Delivers 1.8-V output at 10 A; configurable for other voltages
- Excellent line/load regulation – better than 0.1%
- 96% efficient with V_{IN} = 8 V, V_{OUT} = 3.3 V
- Power good signal
- Output short circuit protection

3 Schematic

The TPS40071EVM−001 schematic is shown in Figure 1. The switching frequency is chosen to be 300 kHz to enable the converter to operate efficiently over a wide range of input and output conditions. C1 is included on the board to represent the output capacitance of the upstream converter feeding the EVM, and no external capacitance should be required at the input. In typical applications with short input wiring (less than 1” to 3” depending on output power level) C1 might not be required. C12 and C14 are local high frequency bypass capacitors for the power circuitry.

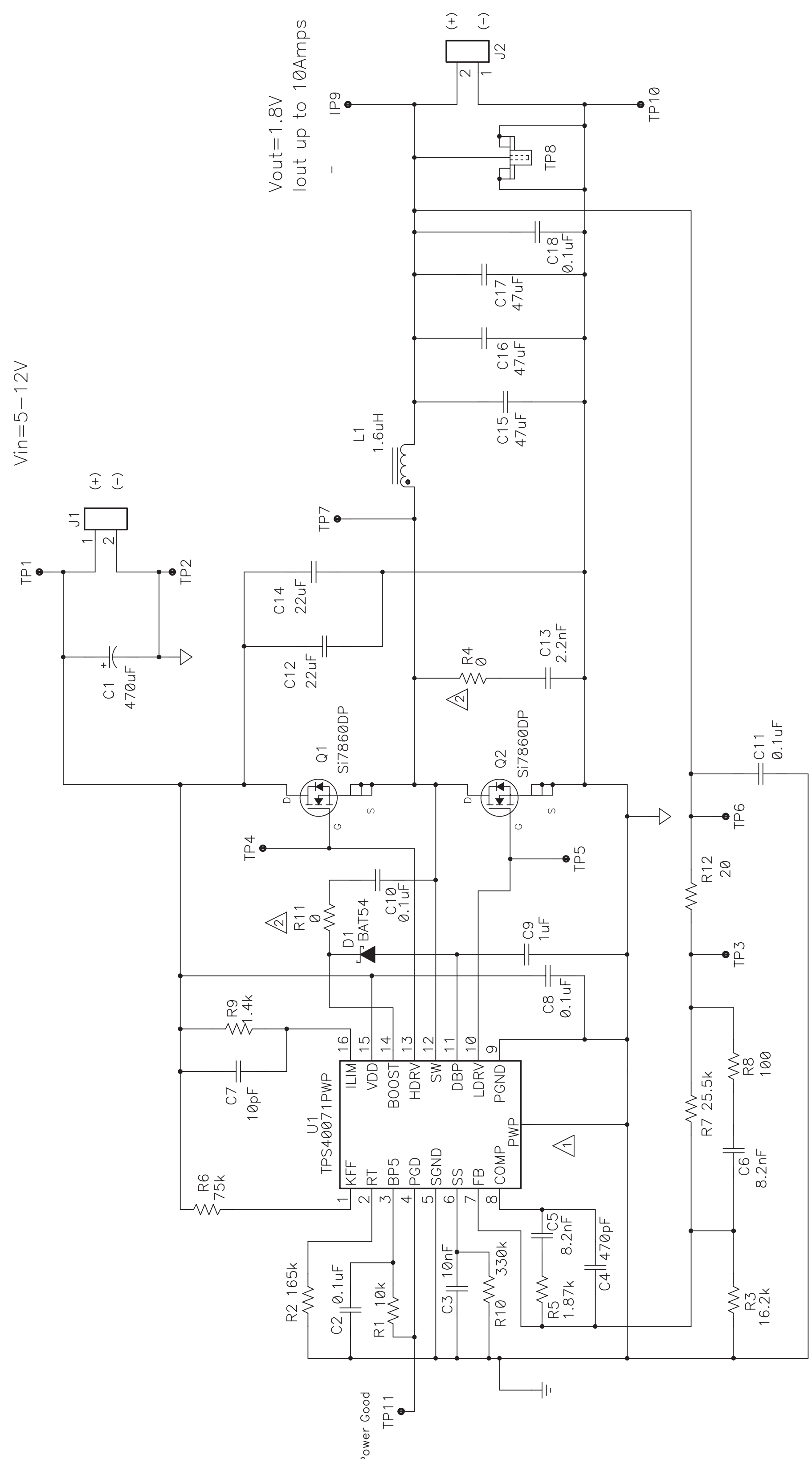


Figure 1. TPS40071EVM−001 Schematic

3.1 Output Filter Components

The power inductor is selected by calculating the range of peak-to-peak ripple current I_{PP} which is obtained with various values of inductance over the total input/output voltage range. In previous generations of buck converters, electrolytic capacitors with significant ESR were the norm, and the inductor ripple current would be selected to be 10% to 20% of I_{OUT} to minimize the output voltage ripple. Now, ceramic output capacitors with ESR in the range of 1 mΩ to 3 mΩ are readily available, so the ripple current can be allowed to be 20% to 50% of the output current. The following equation was used to calculate the ripple current; and complete results are presented for the selected inductor value of 1.6 µH.

$$\Delta I_{PP} = T_{ON} \times \frac{V_{IN} - V_{OUT}}{L} = \frac{V_{OUT}}{V_{IN} \times f_I} \times \frac{V_{IN} - V_{OUT}}{L}$$

Table 1.

V_{IN}	V_{OUT}	I_{RIPPLE}
12	3.3	4.98
12	1.8	3.19
12	1.2	2.25
8	3.3	4.04
8	1.8	2.91
8	1.2	2.12
5	3.3	2.34
5	1.8	2.4
5	1.2	1.9

Ceramic capacitors are selected for the output capacitors, and the minimum value is determined by output voltage ripple considerations:

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} = \frac{5\ A}{8 \times 300\ kHz \times 0.018\ V} = 116\ \mu F$$

Three 47-µF ceramic capacitors are selected to handle the worst case ripple current of 5 A when V_{IN} = 12 V and V_{OUT} = 3.3 V. As the output voltage gets lower the corresponding ripple current is reduced, so excessive output voltage ripple should not be an issue.

3.2 MOSFET Selection

The power MOSFET selection is made with the knowledge that it is difficult to choose one set of components that are optimum over the entire operation range. From maximum V_{IN} to minimum V_{IN} the switch duty cycle can vary from approximately 10% to over 66%. The Vishay Si7860DP is found to be a robust choice for both upper and lower positions with 8-mΩ $R_{DS(on)}$ and less than 30-nC gate charge to keep switching losses low. D1 is included to add to provide maximum boost voltage when V_{IN} is a the low end of its range.

3.3 Frequency and Feed Forward Resistor Selection

To program the switching frequency of 300 kHz R2 is selected according to the TPS40071[1] datasheet equation:

$$R_t = R = \frac{1}{F_{SW} \times 17.82 \times 10^{-6}} - 23 = 164\ k\Omega$$

A standard 1% value of 165 kΩ is selected.

After the switching frequency is selected, the value of R_{kff} would normally be selected to program the minimum desired startup voltage by rearranging the equation for V_{UVLO_ON}. However, the UVLO threshold is not a tightly controlled specification, so a low value startup voltage cannot be accurately programmed. In this case the converter will be allowed to start at the fixed UVLO threshold of 4.5 V. This requires that the value of R_{kff} should be selected to be less than the minimum value on the programmable UVLO V_{ON}, V_{OFF} versus R_{kff} graph in the datasheet. In this converter R_{kff} is selected to be 75 kΩ.

3.4 Output Voltage Setpoint

The output voltage can be easily adjusted from 1.2 V to 3.3 V by changing the value of R3 from its nominal value. The following equation is derived from the output voltage divider R7 and R3, and the internal reference of 0.7 V.

$$R3 = \frac{0.7\ V \times R7}{\left(V_{OUT} - 0.7\right)}$$

The following table specifies the value of R3 for V_{OUT} ranging from 1.2 V to 3.3 V.

Table 2. R3 Values

V_{OUT}	R3 VALUE
1.2 V	35.7 kΩ
1.8 V	16.2 kΩ
3.3V	6.81 kΩ

3.5 Short Circuit Protection Resistor Selection

The current limit resistor R9 is selected using the following datasheet equation:

$$R_{LIM} = \frac{I_{LIM} \times R_{DS(on)} - V_{ILIM(offset)}}{I_{SNK}}$$

In this equation, $I_{LIM} = I_{OUT(max)}$ x 1.3, $R_{DS(on)}$ = 0.0085 Ω x 1.3 (for temperature correction), $V_{LIM(offset)}$ = −0.030 V, and I_{SNK} = 80 µA. Using these conditions leads to selection of R9 = 1.4 kΩ. The capacitor C7 is chosen to be 10 pF to program a brief blanking interval.

3.6 Miscellaneous Parts

Locations for R4 and R11 are present but shorted out in this EVM. The locations were kept to allow evaluation of other MOSFETs and snubbers. C13 is populated with a 2.2 nF to shunt some of the high frequency ringing on the switch node to ground. Since this EVM has a startup voltage below 6.2 V, R10 is populated with 330 kΩ as required in the datasheet.

3.7 Control Loop Compensation

The TPS40071 incorporates voltage mode control with feed-forward compensation to minimize gain variations with a variable supply voltage. A type-3 compensation circuit is utilized to provide two zeroes and three poles as detailed below.

The power circuit LC double pole corner frequency f_C is found to be 10.6 kHz, and the output capacitor ESR zero occurs in the vicinity of 1.1 MHz. The first pole is located at placed at the origin to improve dc regulation.

The first zero is placed at 758 Hz,

$$f_{Z1} = \frac{1}{2 \times \pi \times \left(R_7 + R_8\right) \times C_6}$$

The second zero is selected to be near the LC corner frequency at 10.4 kHz,

$$f_{Z1} = \frac{1}{2 \times \pi \times R_5 \times C_6}$$

The second and third poles are placed at 192 kHz and 194 kHz to roll off the high frequency gain.

$$f_{P2} = \frac{1}{2 \times \pi \times R_5 \times \left(\frac{C_4 - C_5}{\left(C_4 + C_5\right)}\right)}$$

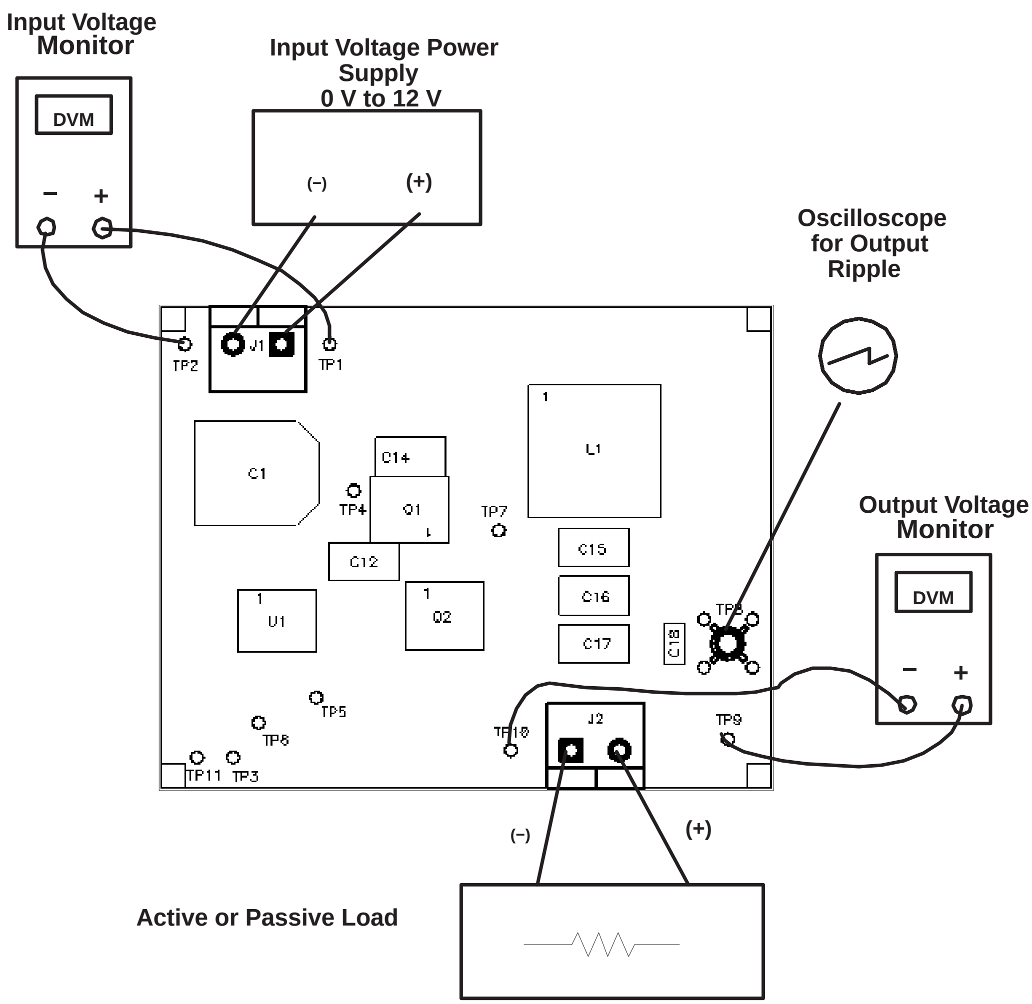
$$f_{P3} = \frac{1}{2 \times \pi \times R_8 \times C_6}$$

4 Test Setup

The basic test setup to power up the TPS40071EVM−001 is shown in Figure 2. The input power source should be capable of supplying the input current to the EVM operating in the intended conditions. This input current can be estimated by the following equation which allows for approximately 20% headroom over the actual input current requirement:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times 0.7}$$

It is extremely important to monitor V_{IN} and V_{OUT} at the test jacks provided to perform accurate efficiency and regulation tests. Voltage drops through the connectors and input/output wiring can contribute significant errors in these measurements.



NOTE: Some components are omitted for clarity. See Figure 9 for more detail.

Figure 2. TPS40071EVM−001 Test Setup

5 Results

The following charts show the efficiency of the TPS40071EVM−001 with V_{OUT} = 1.2 V, 1.8 V, and 3.3 V in Figures 3, 4, and 5, respectively. The converter is seen to perform very efficiently throughout the operating range. With V_{IN} = 5 V the gate drive is reduced and the efficiency can be seen to decreases more rapidly as load current increases.

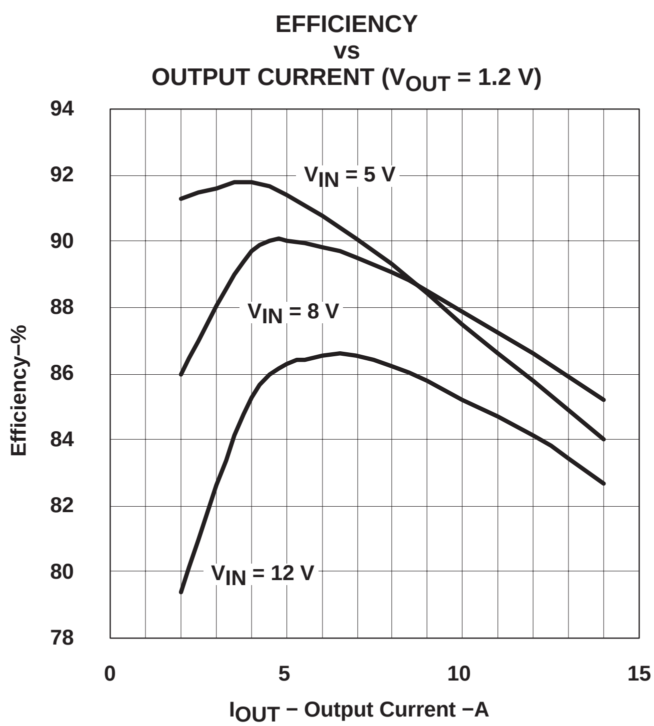


Figure 3

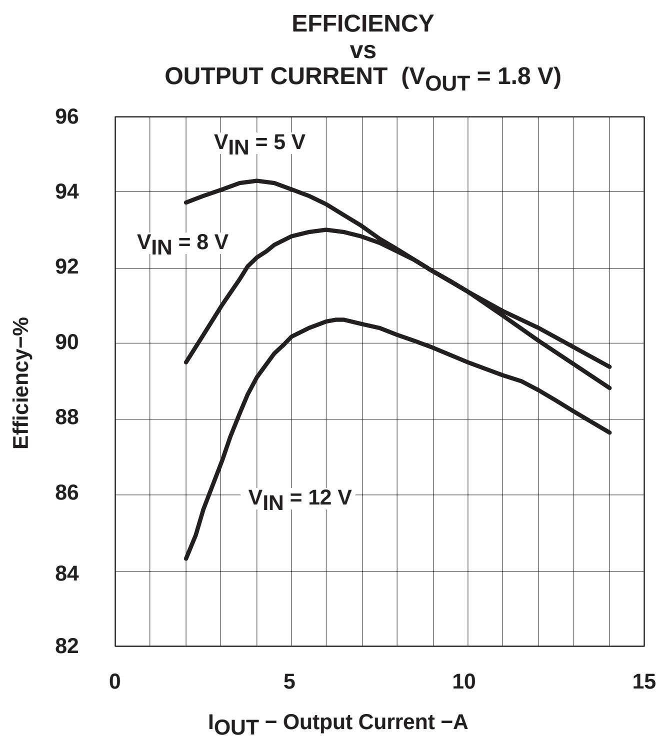


Figure 4

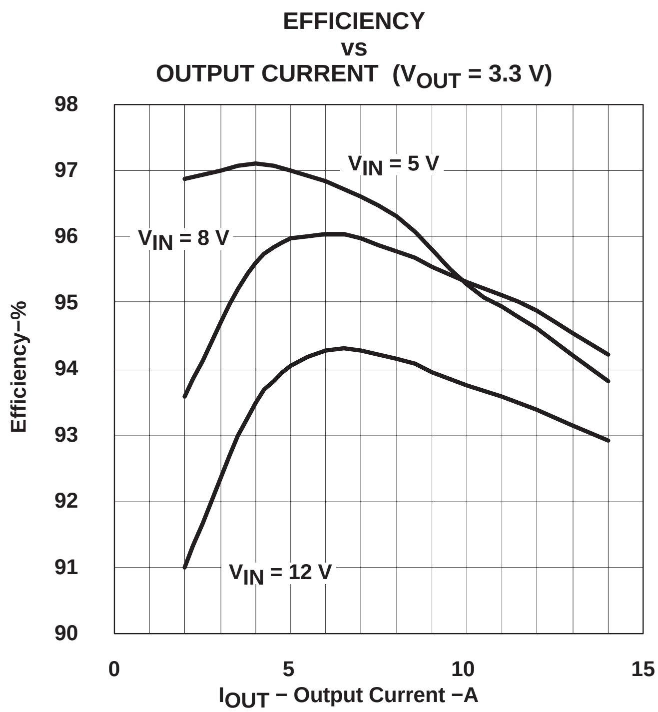


Figure 5

The total watts loss is relatively constant as the output voltage varies from 1.2 V to 3.3 V, but the output power varies with V_{OUT}. This causes the measured efficiency to decrease markedly as the output voltage is lowered.

The transient response for a 50% load step (from 2.5 A to 7.5 A) is shown in Figure 6 for V_{IN} = 12 V, and is essentially unchanged with V_{IN} = 8 V or 5 V.

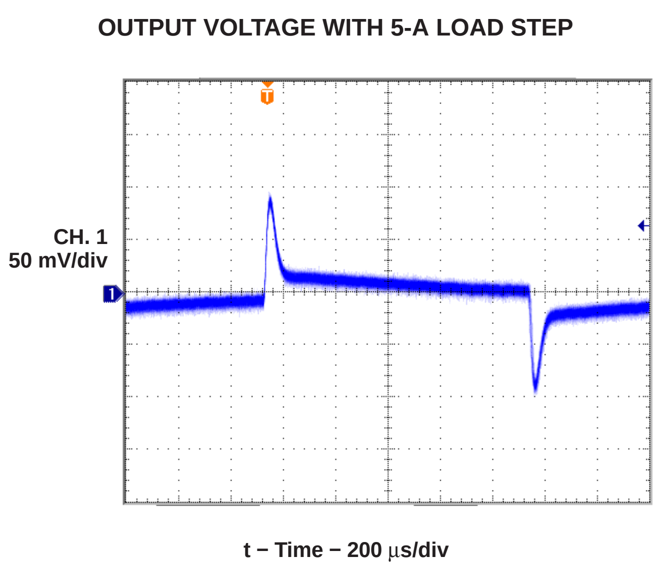


Figure 6

5.1 Control Loop Characteristics

A signal can be injected across R12 at TP3 and TP6 to examine the gain and phase frequency response of this circuit with a network analyzer. Figures 7 and 8 detail the loop gain and phase with V_{IN} = 5 V and V_{IN} = 12 V. Due to the feed forward circuitry implemented in the circuit the gain is seen to be relatively constant as V_{IN} varies more than 2 to 1. There is approximately 50 degrees of phase margin at the loop crossover frequency near 45 kHz.

GAIN/PHASE vs FREQUENCY (V_{IN} = 5 V)

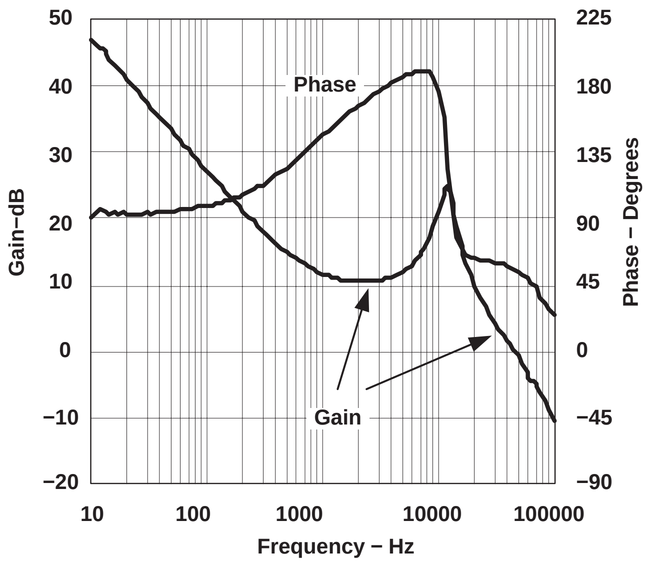


Figure 7

GAIN/PHASE vs FREQUENCY (V_{IN} = 12 V)

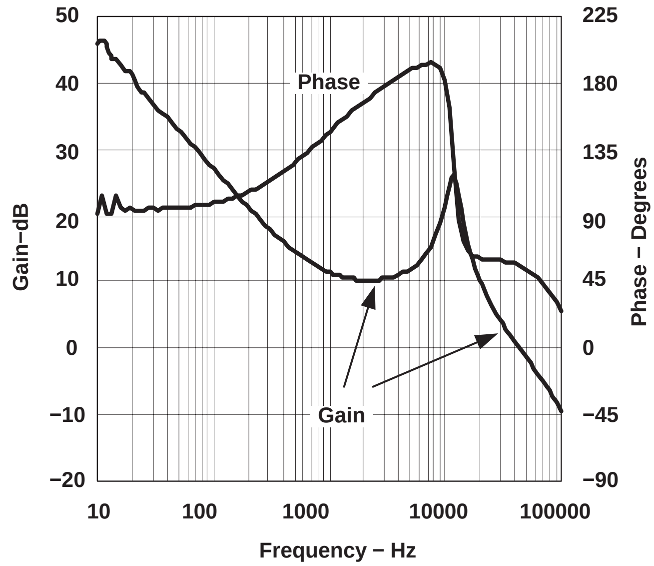


Figure 8

6 Assembly Drawing and PCB Layout

The assembly drawing which shows the PCB outline and the parts placement is shown in Figures 9 through 13.

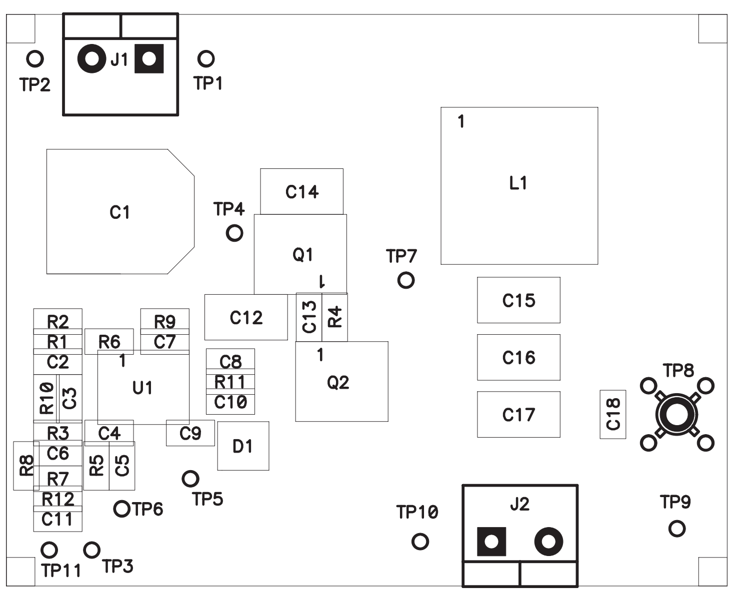


Figure 9. Assembly Drawing

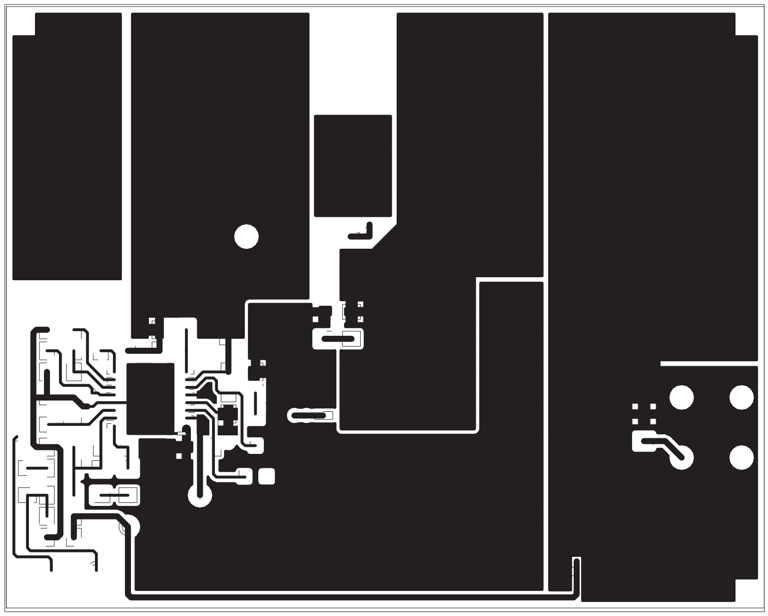


Figure 10. Top Layer Copper

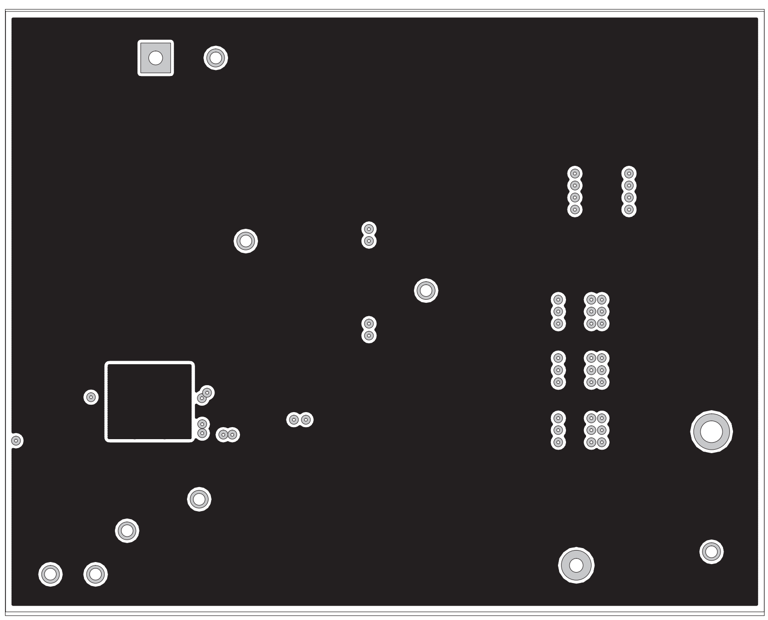


Figure 11. Inner layer 1 Copper

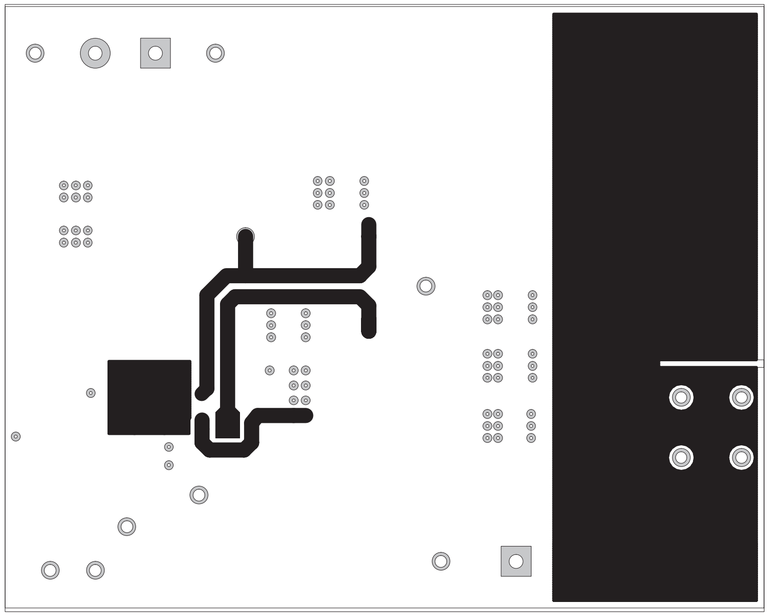


Figure 12. Inner Layer 2 Copper

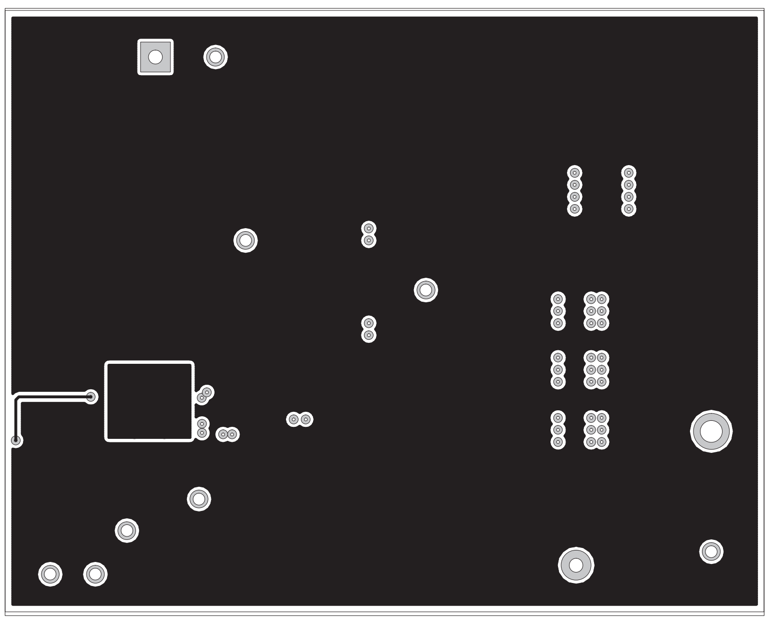


Figure 13. Bottom Layer Copper

7 List of Materials

Table 3. Evaluation Module List of Materials (HPA038)

REFERENCE	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
C1	1	Capacitor, aluminum, 470 µF, 25 V, 20%, 0.457 x 0.406	Panasonic	EEVFK1E471P
C12, C14	2	Capacitor, ceramic, 22 µF, 16 V, X5R, 20%, 1812	TDK	C4532X5R1C226MT
C13	1	Capacitor, ceramic, 2.2 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y222KXAAT
C15, C16, C17	3	Capacitor, ceramic, 47 µF, 6.3 V, X5R, 20%, 1812	TDK	C4532X5R0J47MT
C2, C8, C10, C11, C18	5	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 10%, 805	Vishay	VJ0805Y104KXXAT
C3	1	Capacitor, ceramic, 10 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y103KXAAT
C4	1	Capacitor, ceramic, 470 pF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y471KXAAT
C5, C6	2	Capacitor, ceramic, 8200 pF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y822KXAAT
C7	1	Capacitor, ceramic, 10 pF, 50 V, NPO, 10%, 805	Vishay	VJ0805A100KXAAT
C9	1	Capacitor, ceramic, 1 µF, 16 V, X5R, 10%, 805	TDK	C2012X5R1C105KT
D1	1	Diode, schottky, 200 mA, 30 V, SOT23	Vishay − Liteon	BAT54
J1, J2	2	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 x 0.35	OST	ED1609
L1	1	Inductor, SMT, 1.6 µH, 14.5 A, 2.5 mΩ, 0.515 x 0.516	COEV	DXM1306−1R6
Q1, Q2	2	MOSFET, N-channel, 30 V, 18 A, 8.0 mΩ, PWRPAK S0−8	Vishay − Siliconix	Si7860DP
R1	1	Resistor, chip, 10 kΩ, 1/10 W, 1%, 805	Std	Std
R10	1	Resistor, chip, 330 kΩ, 1/10 W, 5%, 805	Std	Std
R12	1	Resistor, chip, 20 Ω, 1/10 W, 5%, 805	Std	Std
R2	1	Resistor, chip, 165 kΩ, 1/10 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 16.2 kΩ, 1/10 W, 1%, 805	Std	Std
R4, R11	2	Resistor, chip, 0 Ω, 1/10 W, 5%, 805	Std	Std
R5	1	Resistor, chip, 1.87 kΩ, 1/10 W, 1%, 805	Std	Std
R6	1	Resistor, chip, 75 kΩ, 1/10 W, 1%, 805	Std	Std
R7	1	Resistor, chip, 25.5 kΩ, 1/10 W, 1%, 805	Std	Std
R8	1	Resistor, chip, 100 Ω, 1/10 W, 1%, 805	Std	Std
R9	1	Resistor, chip, 1.4 kΩ, 1/10 W, 1%, 805	Std	Std
TP1, TP3, TP4, TP5, TP6, TP7, TP9, TP11	8	Jack, test point, red	Farnell	240−345
TP2, TP10	2	Jack, test point, black	Farnell	240−333
TP8	1	Adaptor, 3.5-mm probe clip (or 131−5031−00), 0.2	Tektronix	131−4244−00
U1	1	IC, PWP16	Texas Instruments	TPS40071PWP
−−	1	PCB, 2.5 In x 2 in x 0.062 in	Std	HPA038

8 References

1. Data sheet, *TPS40070/1/2 Midrange Input Synchronous Buck Controller*, Texas Instruments Literature Number SLUS582

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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