TEXAS INSTRUMENTS

TPD2EUSB30, TPD2EUSB30A, TPD4EUSB30

SLVSAC2F – AUGUST 2010 – REVISED OCTOBER 2015

# TPDxEUSB30 2-, 4-Channel ESD Protection for Super-Speed USB 3.0 Interface

## 1 Features

- Supports USB 3.0 Data Rates (5 Gbps)
- IEC 61000-4-2 ESD Protection (Level 4 Contact)
- IEC 61000-4-5 Surge Protection
  - 5 A (8/20 µs)
- Low Capacitance
  - DRT: 0.7 pF (Typ)
  - DQA: 0.8 pF (Typ)
- Dynamic Resistance: 0.6 Ω (Typ)
- Space-Saving DRT, DQA Packages
- Flow-Through Pin Mapping

## 2 Applications

- Notebooks
- Set-Top Boxes
- DVD Players
- Media Players
- Portable Computers

## 3 Description

The TPD2EUSB30, TPD2EUSB30A, and TPD4EUSB30 are 2 and 4 channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode arrays. The TPDxEUSB30/A devices are rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Contact). These devices also offer 5 A (8/20 µs) peak pulse current ratings per IEC 61000-4-5 (Surge) specification.

The TPD2EUSB30A offers low 4.5-V DC break-down voltage. The low capacitance, low break-down voltage, and low dynamic resistance make the TPD2EUSB30A a superior protection device for high-speed differential IOs.

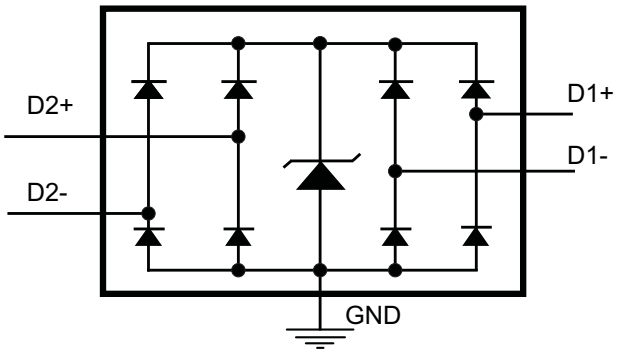
The TPD2EUSB30 and TPD2EUSB30A are offered in space saving DRT (1 mm × 1 mm) package. The TPD4EUSB30 is offered in space saving DQA (2.5 mm × 1.0 mm) package.

**Device Information(1)**

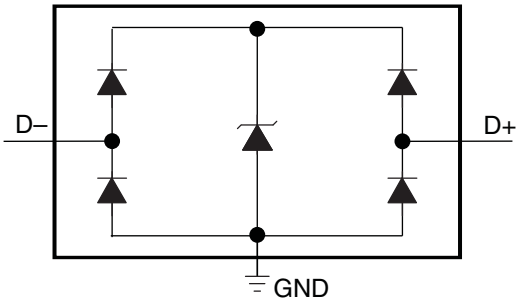
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPD2EUSB30 | SOT (3) | 1.00 mm x 0.80 mm |
| TPD2EUSB30A | | |
| TPD4EUSB30 | USON (10) | 2.50 mm x 1.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**TPD4EUSB30 Circuit**




**TPD2EUSB30/A Circuit**



## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (August 2014) to Revision F** — **Page**

- Moved the storage temperature to the *Absolute Maximum Ratings* table and updated the *Handling Ratings* table to an *ESD Ratings* table ... 3
- Added test condition frequency to capacitance ... 4
- Added *Community Resources* ... 13

**Changes from Revision D (August 2012) to Revision E** — **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision C (December 2011) to Revision D** — **Page**

- Updated Dynamic Resistance value ... 1
- Updated Dynamic Resistance value ... 4

**Changes from Revision B (July 2011) to Revision C** — **Page**

- Added Insertion Loss graphic to TYPICAL OPERATING CHARACTERISTICS section. ... 6

**Changes from Revision A (December 2010) to Revision B** — **Page**

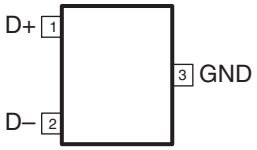
- Changed TOP-SIDE MARKING column in the Ordering Information Table ... 3

**Changes from Original (August 2010) to Revision A** — **Page**

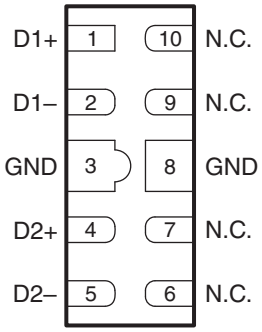
- Added TPS2EUSB30A part to document. ... 1

# 5 Pin Configuration and Functions

**DRT Package**
**3-Pin SOT**
**Top View**




**DQA Package**
**10-Pin USON**
**Top View**




**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | DRT | DQA | | |
| Dx+, Dx– | 1, 2 | 1, 2, 4, 5 | ESD port | High-speed ESD clamp, provides ESD protection to the high-speed differential data lines |
| GND | 3 | 3, 8 | GND | Ground |
| N.C. | — | 6, 7, 9, 10 | — | Not normally connected |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | IO voltage (D+ and D- pins) | TPD2EUSB30, TPD4EUSB30 | 0 | 6 | V |
| | | TPD2EUSB30A | 0 | 4 | |
| | IEC 61000-4-5 surge current ($t_p$ = 8/20 µs) | D+, D– pins | | 5 | A |
| | IEC 61000-4-5 surge peak power ($t_p$ = 8/20 µs) | D+, D– pins | | 45 | W |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 125 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | | 2500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | | 1500 | |
| | | IEC 61000-4-2 Contact Discharge | D+, D– pins | 8000 | |
| | | IEC 61000-4-2 Air-Gap Discharge (TPD2EUSB30/A) | D+, D– pins | 8000 | |
| | | IEC 61000-4-2 Air-Gap Discharge (TPD4EUSB30) | D+, D– pins | 9000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_A$ operating free-air temperature | | –40 | 85 | °C |
| Operating Voltage | TPD2EUSB30, TPD4EUSB30 | 0 | 5.5 | V |
| | TPD2EUSB30A | 0 | 3.6 | |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPD2EUSB30 | TPD2EUSB30A | TPD4EUSB30 | UNIT |
|---|---|---|---|---|---|
| | | DRT (SOT) | DRT (SOT) | DQA (USON) | |
| | | 3 PINS | 3 PINS | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 610.2 | 610.2 | 162.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 288.0 | 288.0 | 128.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 118.4 | 118.4 | 56.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 20.2 | 20.2 | 13.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 116.4 | 116.4 | 56.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | 8.1 | °C/W |

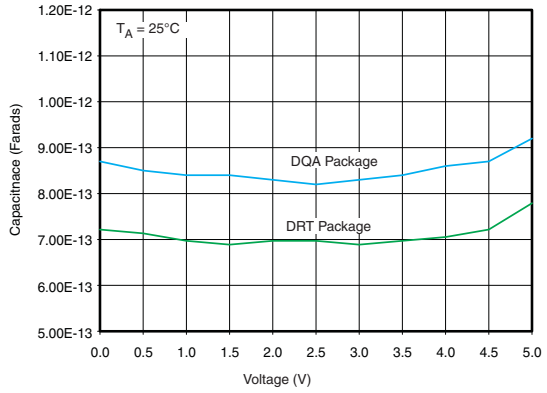
(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

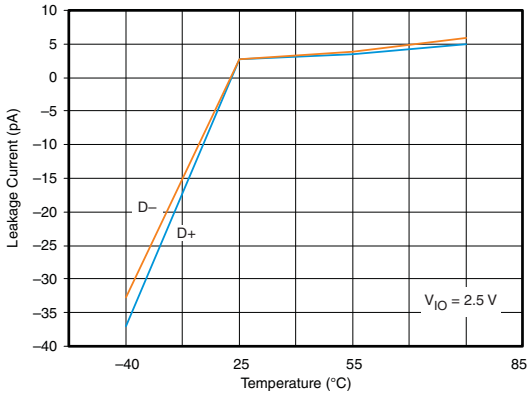
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse stand-off voltage (D+ and D- pins) | TPD2EUSB30, TPD4EUSB30 | | | | 5.5 | V |
| | | TPD2EUSB30A | | | | 3.6 | V |
| $V_{clamp}$ | Clamp voltage | D+,D– pins to ground, | $I_{IO}$ = 1 A | | | 8 | V |
| $I_{IO}$ | Current from IO port to supply pins | $V_{IO}$ = 2.5 V, | $I_D$ = 8 mA | | 0.01 | 0.1 | µA |
| $V_D$ | Diode forward voltage | D+,D– pins, lower clamp diode, | $V_{IO}$ = 2.5 V, $I_D$ = 8 mA | 0.6 | 0.8 | 0.95 | V |
| $R_{dyn}$ | Dynamic resistance | D+,D– pins | I = 1 A | | 0.6 | | Ω |
| $C_{IO-IO}$ | Capacitance IO to IO | D+,D– pins | $V_{IO}$ = 2.5 V; $f$ = 100 kHz | | 0.05 | | pF |
| $C_{IO-GND}$ | Capacitance IO to GND | D+,D– pins (DRT) | $V_{IO}$ = 2.5 V; $f$ = 100 kHz | | 0.7 | | pF |
| | | D1+, D1-, D2+, D2- (DQA ) | | | 0.8 | | |
| $V_{BR}$ | Break-down voltage, TPD2EUSB30, TPD4EUSB30 | $I_{IO}$ = 1 mA | | 7 | | | V |
| | Break-down voltage, TPD2EUSB30A | $I_{IO}$ = 1 mA | | 4.5 | | | V |

## 6.6 Typical Characteristics



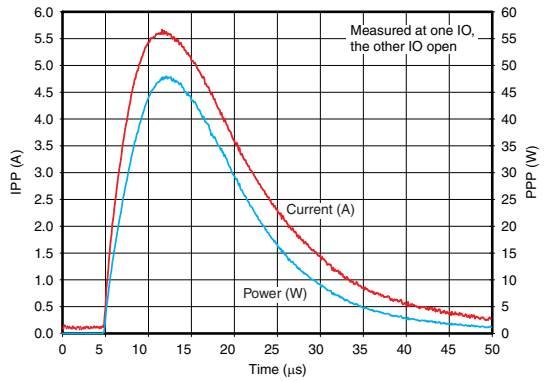

$T_A$ = 25 °C

**Figure 1. IO Capacitance vs IO Voltage**




$V_{IO}$ = 2.5 V

**Figure 2. Leakage Current vs Temperature**




Measured at one IO, the other IO open

**Figure 3. Peak Pulse Waveforms**

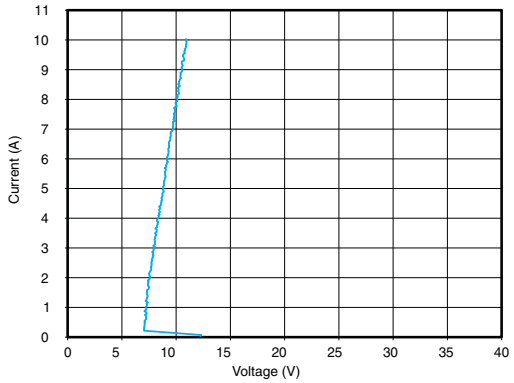



**Figure 4. D+,D– Transmission Line Pulser Plot for TPD2EUSB30 (100 ns Pulse, 10 ns Rise Time)**

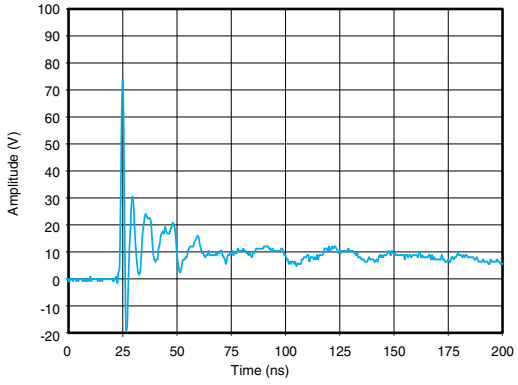



**Figure 5. IEC Clamping Waveforms (8 kV Contact)**

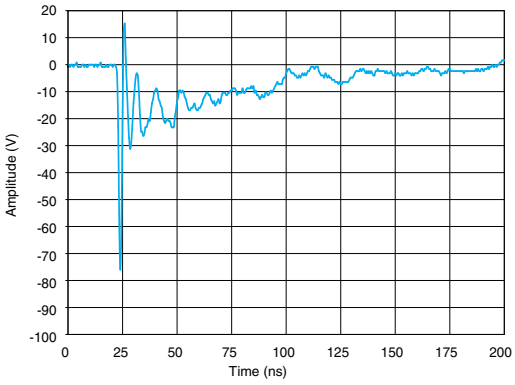
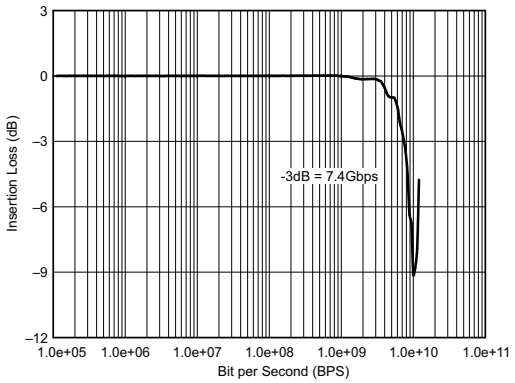



**Figure 6. IEC Clamping Waveforms (–8 kV Contact)**

## Typical Characteristics (continued)




–3 dB = 7.4 Gbps

**Figure 7. Insertion Loss**

# 7 Detailed Description

## 7.1 Overview

The TPD2EUSB30, TPD2EUSB30A, and TPD4EUSB30 are 2 and 4 channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode arrays. The TPDxEUSB30/A devices are rated to dissipate ESD strikes at the maximum contact level specified in the IEC 61000-4-2 international standard (Contact). These devices also offer 5 A (8/20 µs) peak pulse current ratings per IEC 61000-4-5 (surge) specification.

## 7.2 Functional Block Diagrams

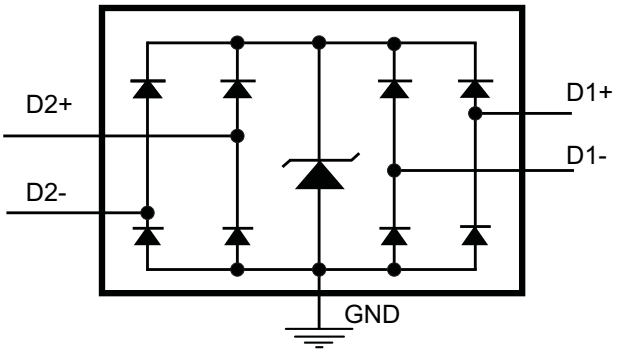



**Figure 8. TPD4EUSB30 Circuit**

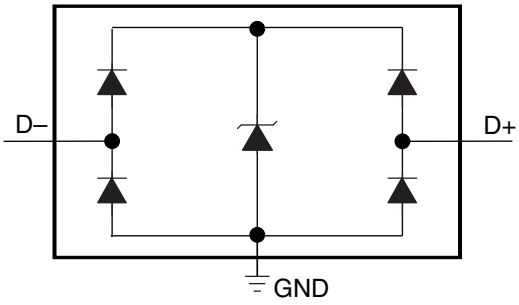



**Figure 9. TPD2EUSB30/A Circuit**

## 7.3 Feature Description

TPDxEUSB30/A is a family of uni-directional Electrostatic Discharge (ESD) protection devices with low capacitance. Each IO line is rated to dissipate ESD strikes at or above the maximum level specified in the IEC 61000-4-2 (Level 4 Contact) international standard. The TPDxEUSB30/A's low loading capacitance makes it ideal for protection super speed high-speed signals.

## 7.4 Device Functional Modes

The TPDxEUSB30/A family of devices are passive integrated circuits that activate whenever voltages above $V_{BR}$ or below the lower diodes $V_{forward}$ (–0.6V) are present upon the circuit being protected. During ESD events, voltages as high as ±8 kV (contact) can be directed to ground via the internal diode network. Once the voltages on the protected lines fall below the trigger voltage of the device (usually within 10's of nano-seconds) the device reverts to passive.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPDxEUSB30/A family is a family of diode array type transient voltage suppressors (TVS) which are typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low $R_{DYN}$ of the triggered TVS holds this voltage, $V_{CLAMP}$, to a tolerable level to the protected IC.

## 8.2 Typical Application

This application describes a TPDxEUSB30/A eye pattern test. Figure 17 shows the lab board that was designed to demonstrate the degradation of the eye pattern quality with and without the TPD2EUSB30/A in the USB 3.0 signal path. The measurements show that there is only ~2 ps jitter penalty to the differential signal when the TPD2EUSB30/A device is added in the signal path. A similar setup was employed to measure the eye diagram for the TPD4EUSB30.

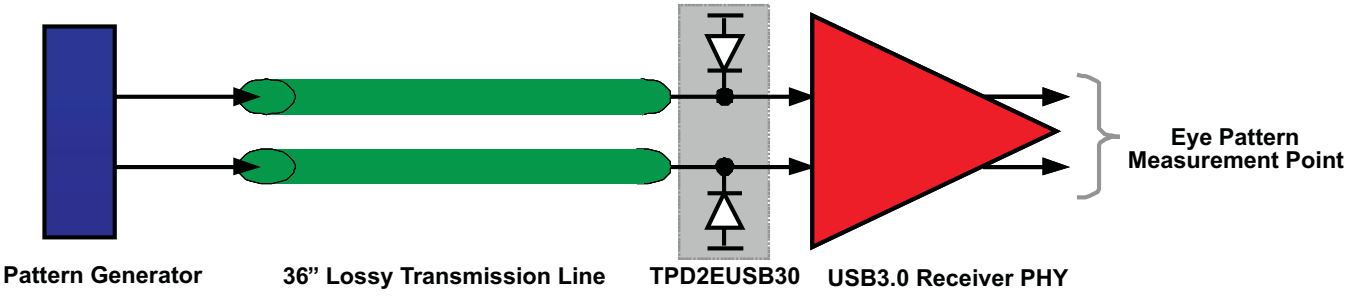



**Figure 10. Measurement Setup to collect the Eye Pattern on a Reference Board with TPD2EUSB30/A**

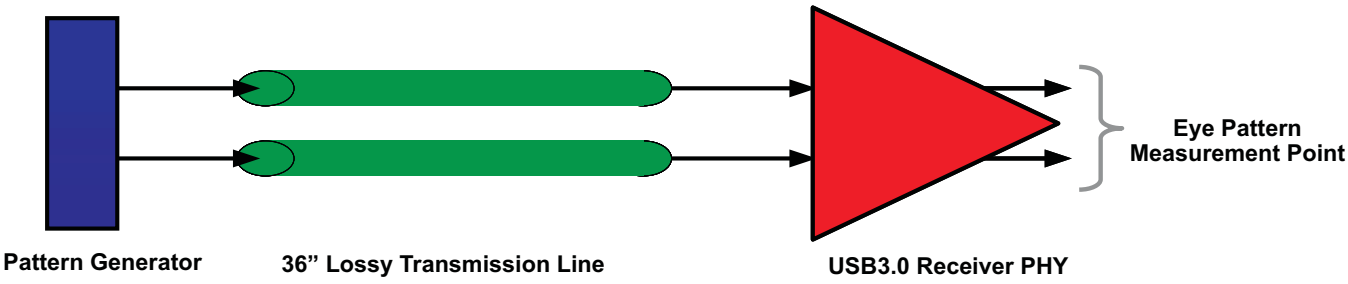



**Figure 11. Measurement Setup to collect the Eye Pattern on a Reference Board with TPD2EUSB30/A**

### 8.2.1 Design Requirements

For this design example, a single TPD2EUSB30/A is used to protect a differential data pair lines, similar to a USB 3.0 application. Given the USB application, the following parameters are known.

**Table 1. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Signal range on D+, and D– | 0 V to 3.3 V |
| Operating Frequency | 2.5 GHz |

### 8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

#### *8.2.2.1 Signal Range on D+, D- Pins*

The TPD2EUSB30 has 2 pins which support 0 to 5.5 V and the TPD2EUSB30A has 2 pins which support 0 to 3.6 V.

#### *8.2.2.2 Operating Frequency*

The 0.7 pF (TPD2EUSB30/A typ) line capacitance supports data rates in excess of 5 Gbps.

### 8.2.3 Application Curves

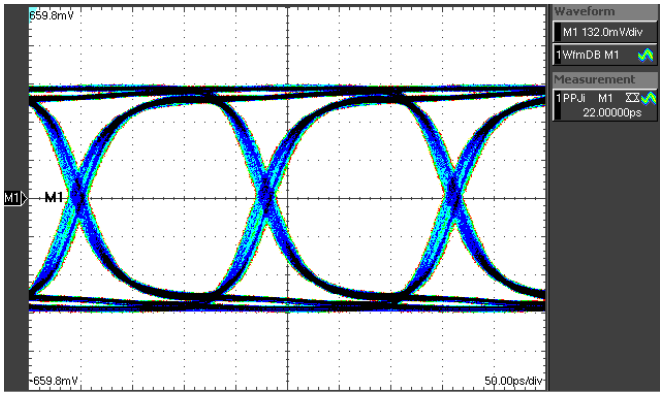



**Figure 12. Output Eye Diagram Without TPD2EUSB30A (Figure 11 Setup, 5 Gbps Data Rate)**

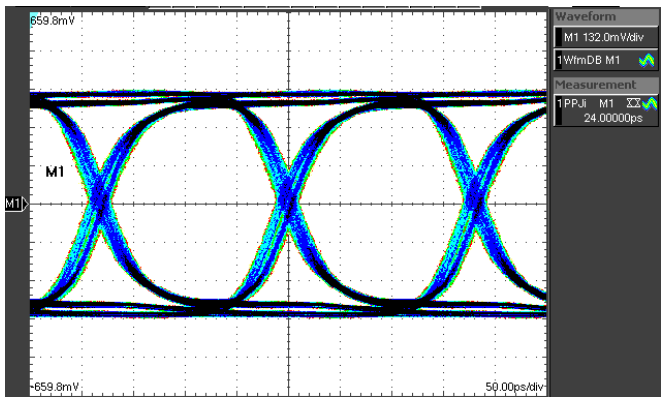



**Figure 13. Output Eye Diagram With the TPD2EUSB30A (Figure 11 Setup, 5 Gbps Data Rate)**

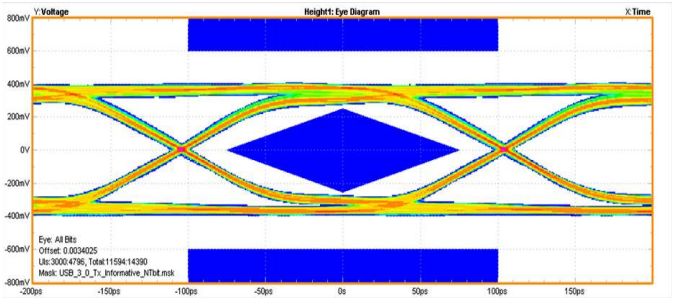



**Figure 14. Output Eye Diagram Without the TPD4EUSB30 (5 Gbps Data Rate)**

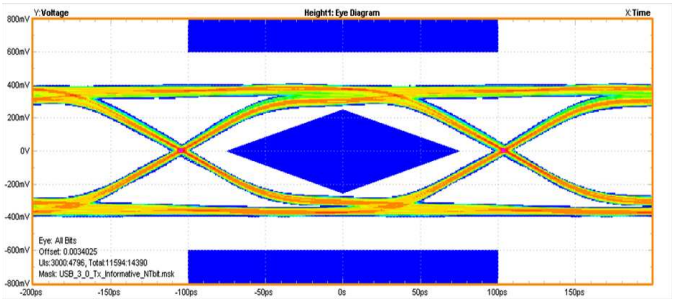



**Figure 15. Output Eye Diagram with the TPD4EUSB30 (5 Gbps Data Rate)**

# 9 Power Supply Recommendations

This family of devices are passive ESD protection devices and there is no need to power them. Care should be taken to not violate the maximum voltage specification to ensure that the device functions properly. The D+ and D– lines share a TVS diode which can tolerate up to 6 V.

# 10 Layout

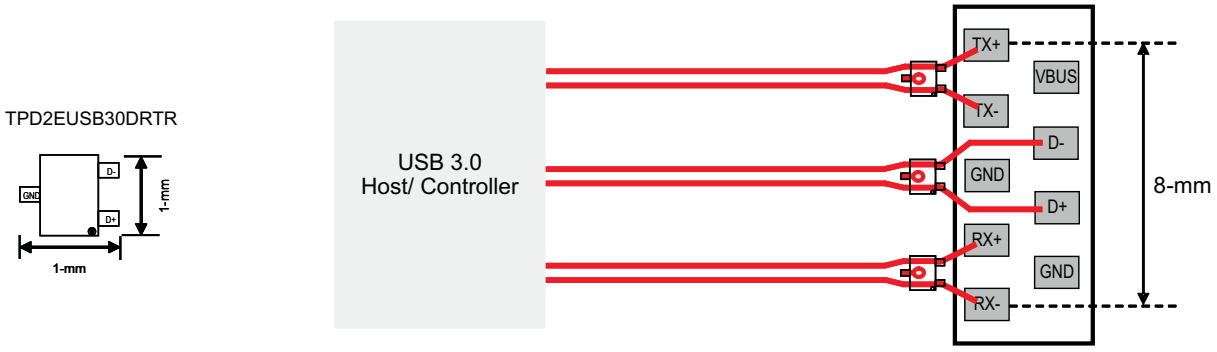
## 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

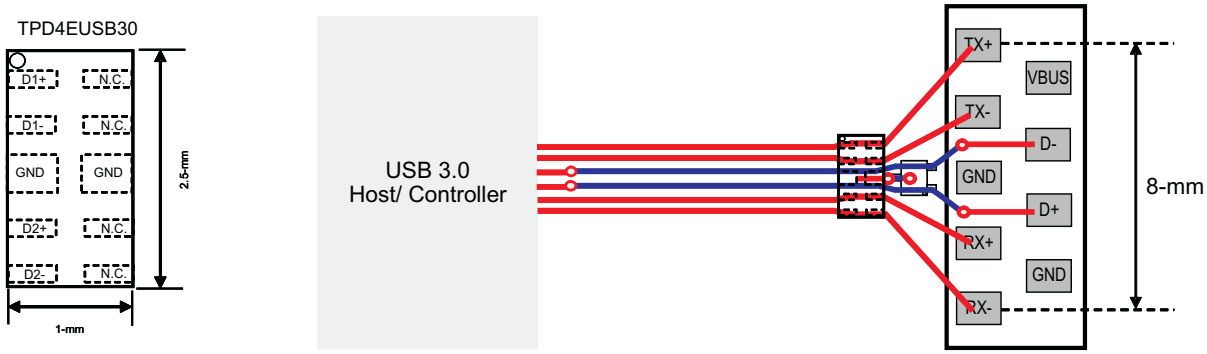
Refer to Figure 16, the TPD2EUSB30/A are offered in space saving DRT package. The DRT is a 1-mm × 1-mm package with flow-through pin-mapping for the high-speed differential lines. The TPD4EUSB30 is offered in space saving DQA package. The DQA is a 1-mm × 2.5-mm package with flow-through pin-mapping for the high-speed differential lines. It is recommended to place the package right next to the USB 3.0 connector. The GND pin should connected to GND plane of the board through a large VIA. If a dedicated GND plane is not present right underneath, it is recommended to route to the GND plane through a wide trace. The current associated with IEC ESD stress can be in the range of 30Amps or higher momentarily. A good, low impedance GND path ensures the system robustness against IEC ESD stress.

The TPDxEUSB30/A can provide system level ESD protection to the high-speed differential ports (> 5 Gbps data rate). The flow-through package offers flexibility for board routing with traces up to 15 mills wide. It allows the differential signal pairs couple together right after they touch the ESD ports of the TPDxEUSB30/A.

## 10.2 Layout Examples




Three TPD2EUSB30 to Protect USB3.0 Class A connector (One Layer Routing)




One TPD4EUSB30 & One TPD2EUSB30 to Protect USB3.0 Class A connec tor (Two Layer Routing)

**Figure 16. TPDxEUSB30/A at the USB3.0 Class A Connector**

## Layout Examples (continued)

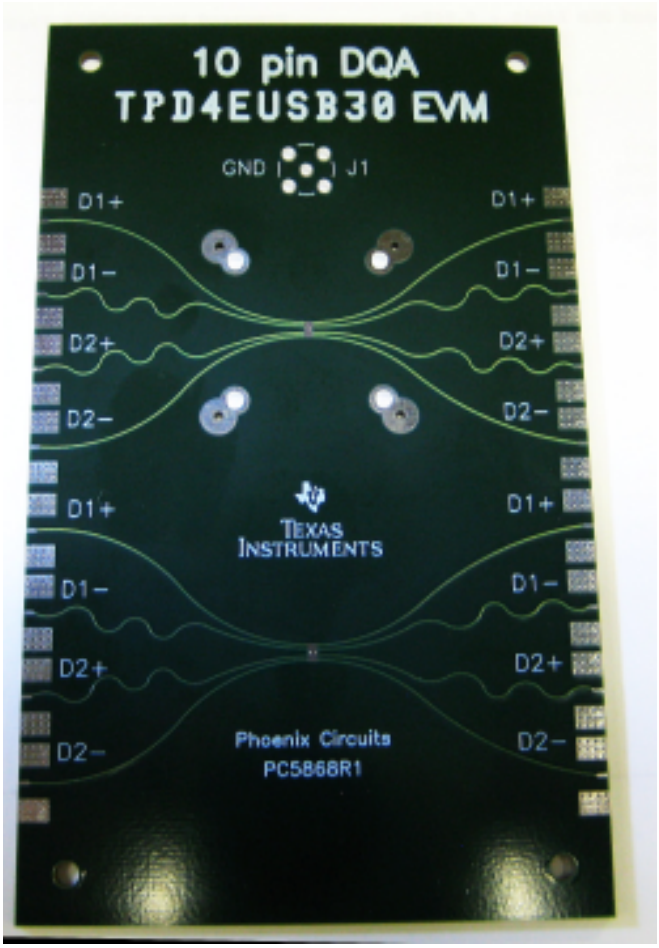



Figure 17. TPDxEUSB30/A EVM – TPD4EUSB30 Side

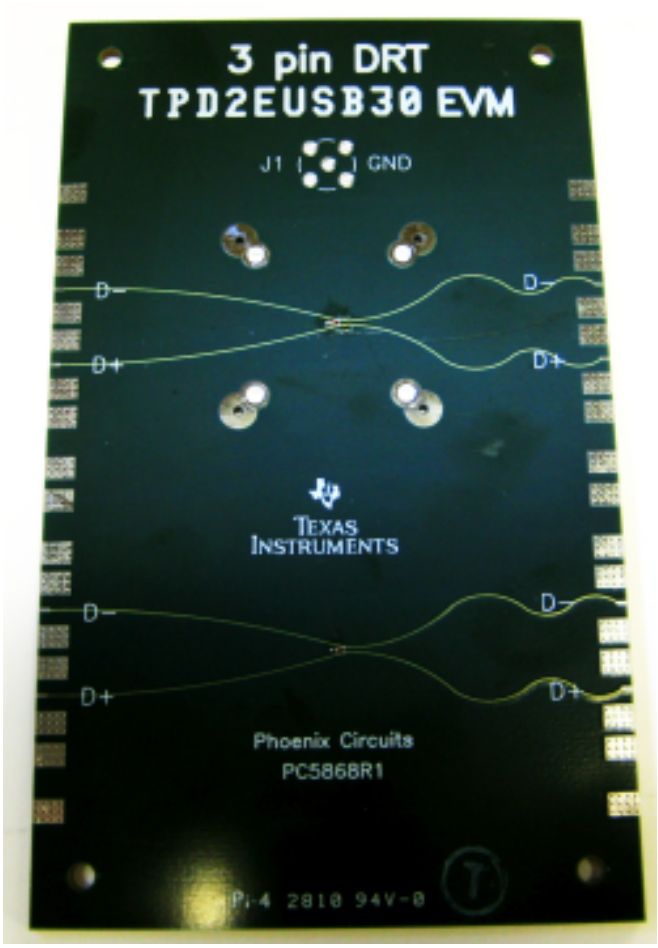



Figure 18. TPDxEUSB30/A EVM – TPD2EUSB30/A Side

# 11 Device and Documentation Support

## 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPD2EUSB30 | Click here | Click here | Click here | Click here | Click here |
| TPD2EUSB30A | Click here | Click here | Click here | Click here | Click here |
| TPD4EUSB30 | Click here | Click here | Click here | Click here | Click here |

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD2EUSB30ADRTR | ACTIVE | SOT | DRT | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5S | Samples |
| TPD2EUSB30DRTR | ACTIVE | SOT | DRT | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5P | Samples |
| TPD4EUSB30DQAR | ACTIVE | USON | DQA | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (667 ~ 66O ~ 66R ~ 66V) | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

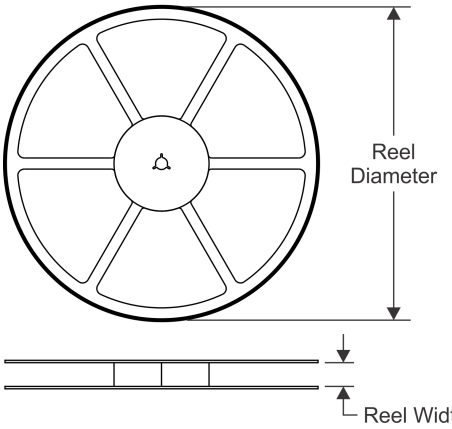
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

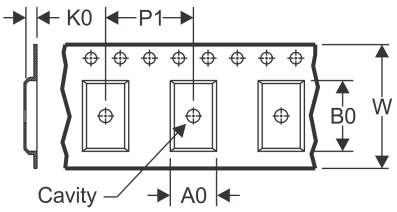
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

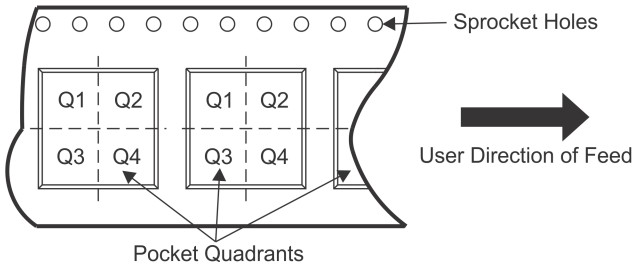



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

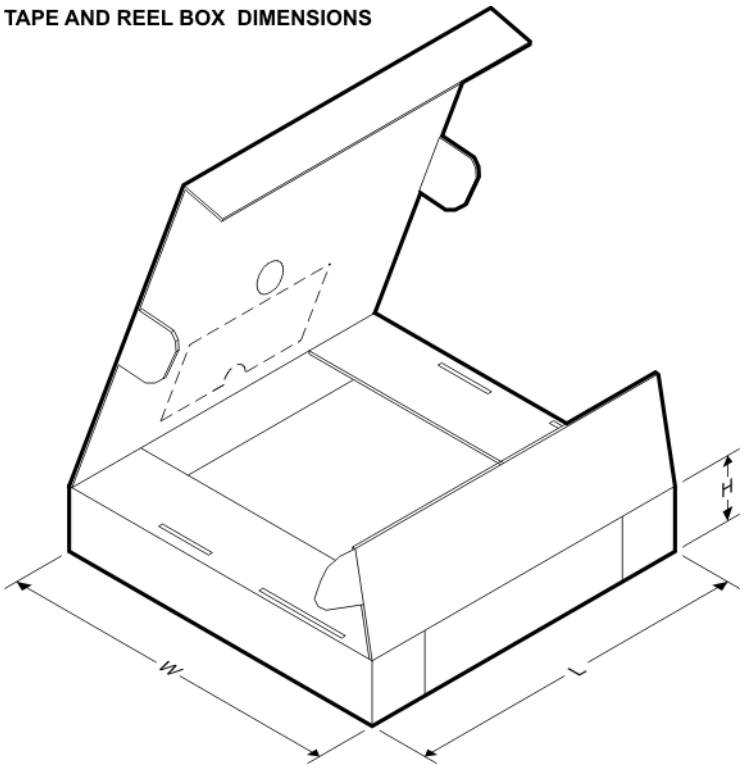
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

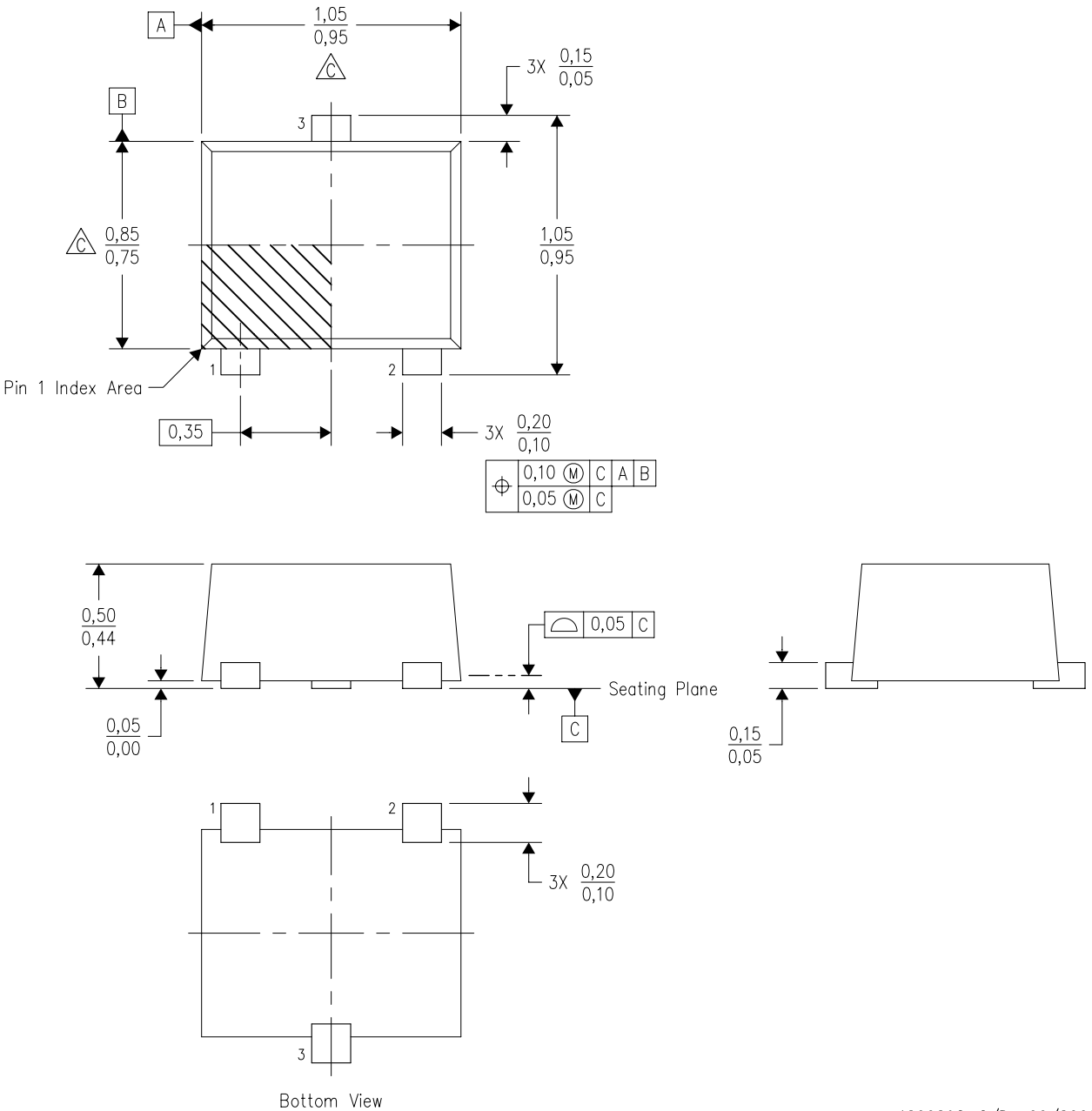
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD2EUSB30ADRTR | SOT | DRT | 3 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.63 | 4.0 | 8.0 | Q3 |
| TPD2EUSB30DRTR | SOT | DRT | 3 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.63 | 4.0 | 8.0 | Q3 |
| TPD4EUSB30DQAR | USON | DQA | 10 | 3000 | 180.0 | 9.5 | 1.23 | 2.7 | 0.7 | 4.0 | 8.0 | Q1 |
| TPD4EUSB30DQAR | USON | DQA | 10 | 3000 | 180.0 | 8.4 | 1.3 | 2.83 | 0.65 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



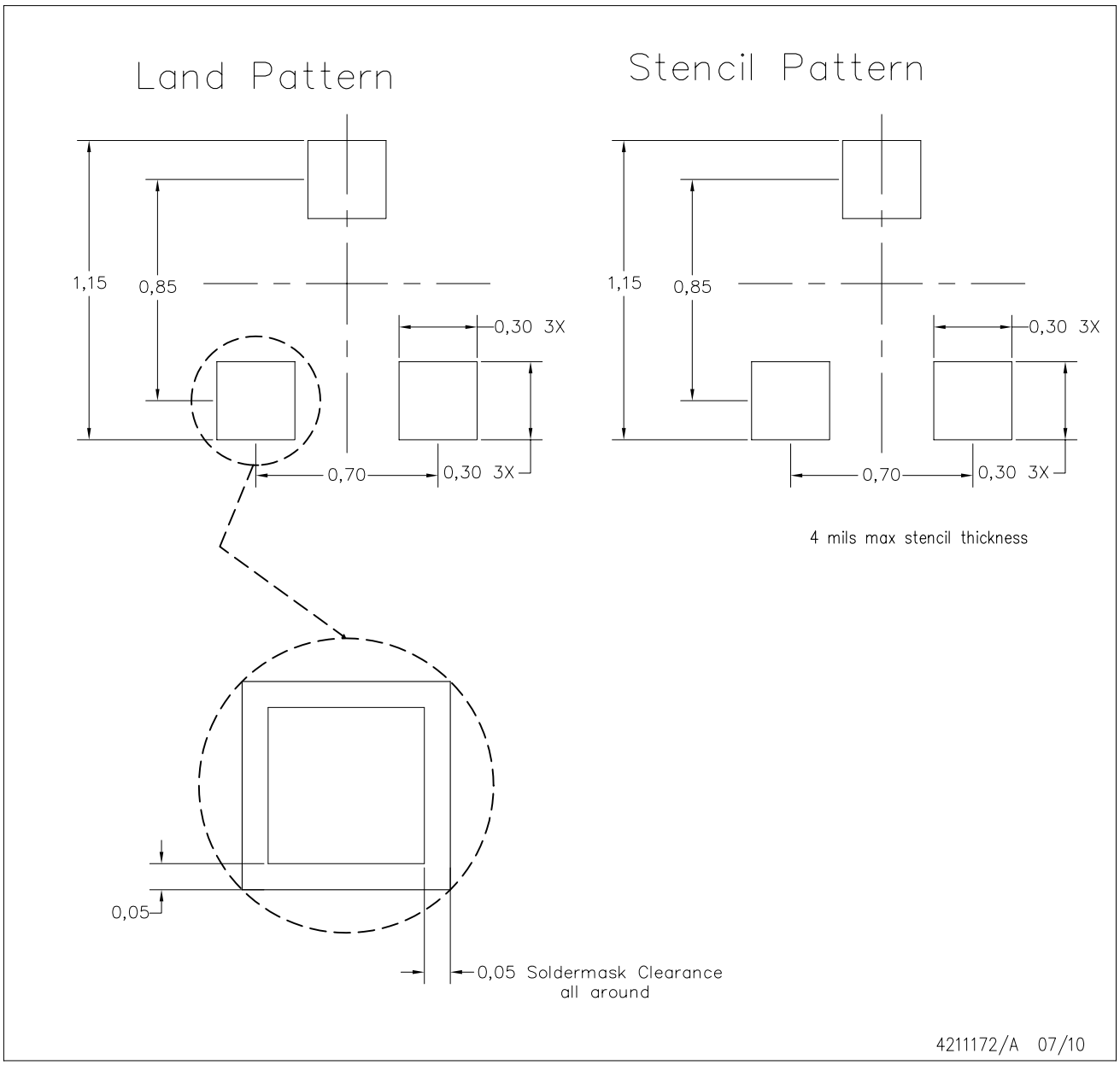

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD2EUSB30ADRTR | SOT | DRT | 3 | 3000 | 202.0 | 201.0 | 28.0 |
| TPD2EUSB30DRTR | SOT | DRT | 3 | 3000 | 202.0 | 201.0 | 28.0 |
| TPD4EUSB30DQAR | USON | DQA | 10 | 3000 | 184.0 | 184.0 | 19.0 |
| TPD4EUSB30DQAR | USON | DQA | 10 | 3000 | 202.0 | 201.0 | 28.0 |



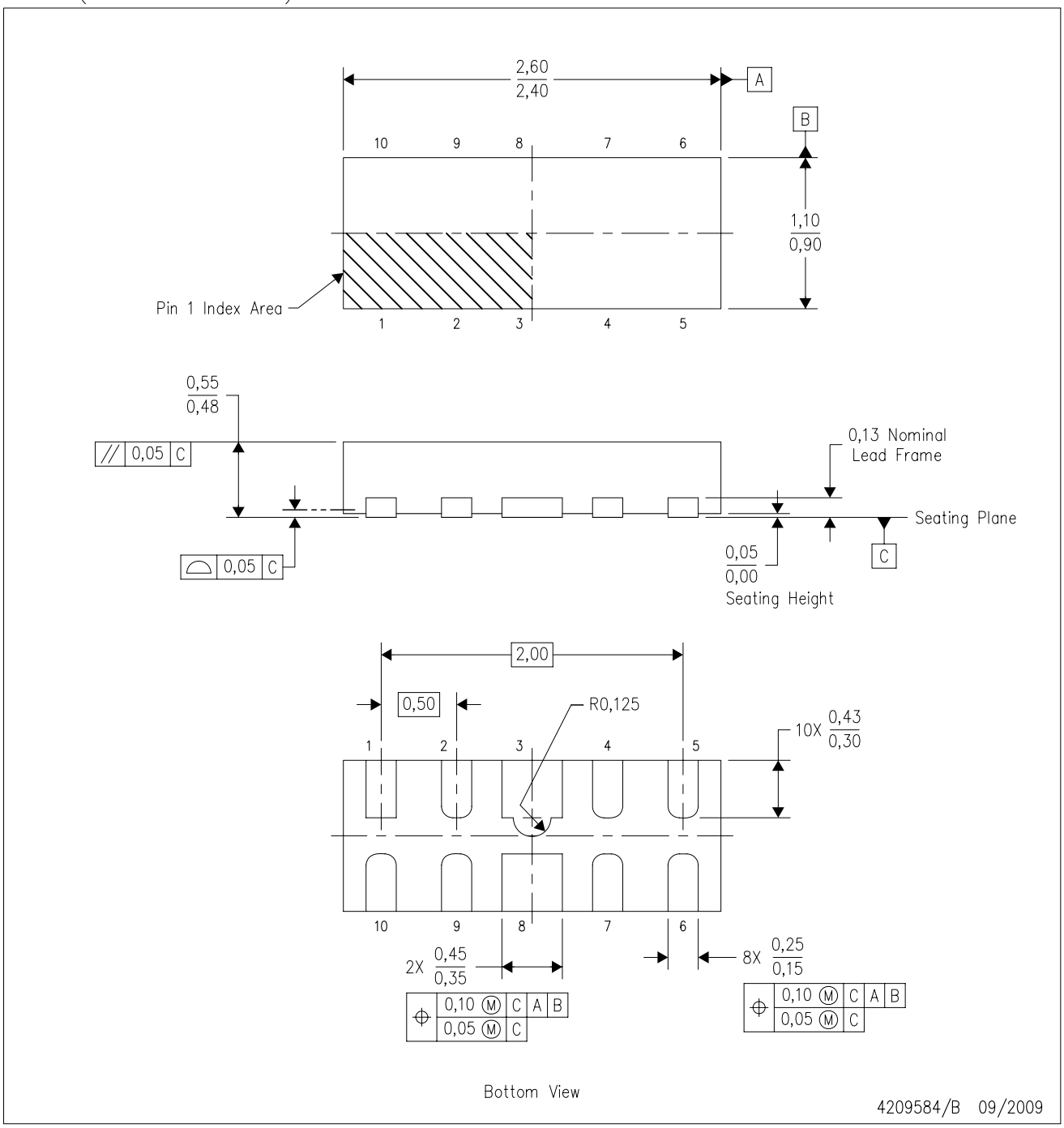

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,10 per end or side.
D. JEDEC package registration is pending.

DRT (S–PDSO–N3) PLASTIC SMALL OUTLINE



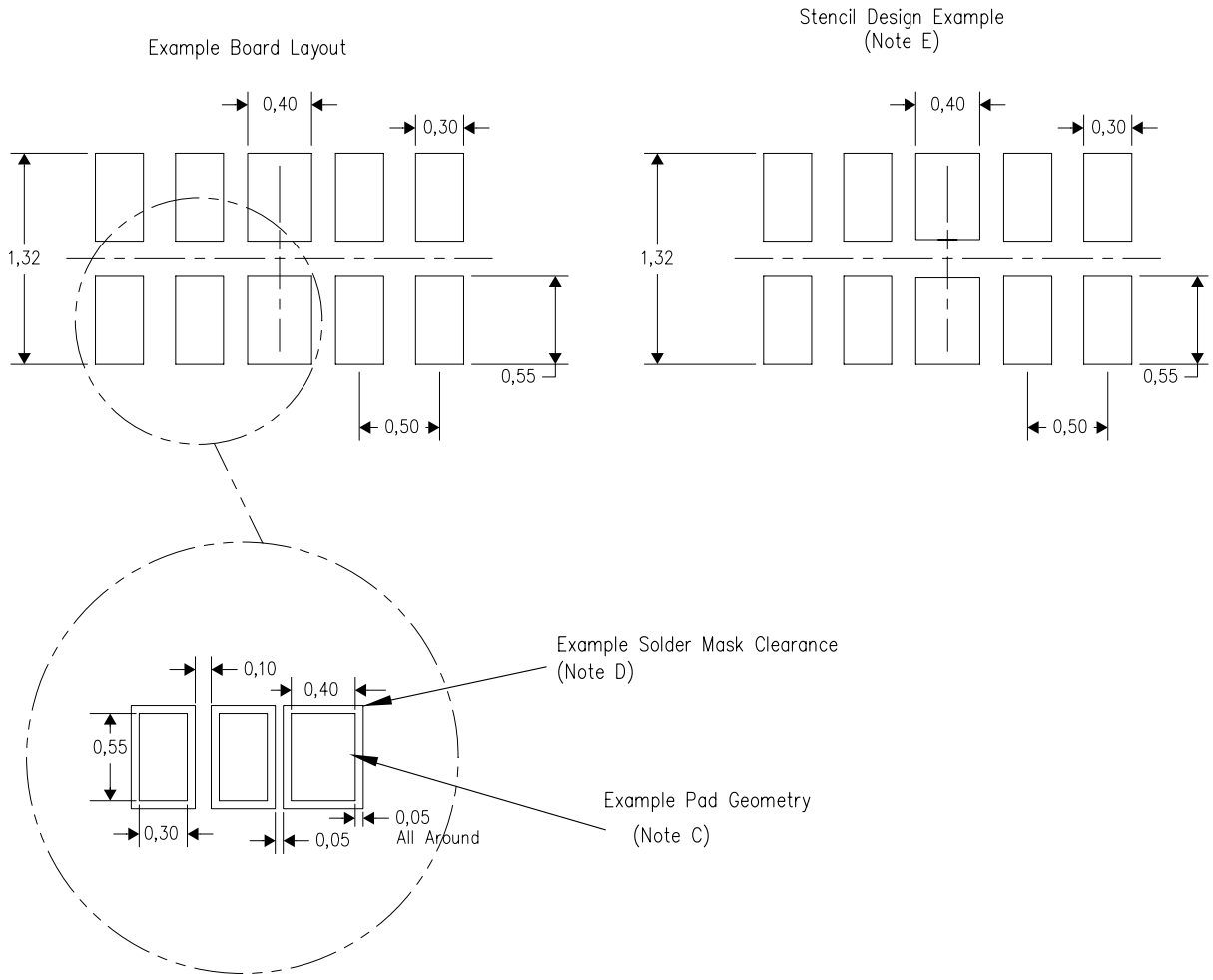

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQA (R–PSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQA (R–PUSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265