1, 4, 6 Channel ESD Protection Device for Super-Speed (up to 6 GBPS) Interface

Check for Samples: TPD1E05U06, TPD4E05U06, TPD6E05U06

FEATURES

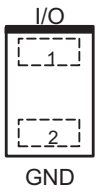
- **Provides System Level ESD Protection for Low- Voltage IO Interface**
- **IEC 61000-4-2 Level 4**
  - **±15kV (Air gap discharge)**
  - **±12kV (Contact discharge)**
- **IO Capacitance 0.42pF to 0.5pF (Typ)**
- **DC Breakdown Voltage 6.5V (Min)**
- **Ultra low Leakage Current 10nA (Max)**
- **Low ESD Clamping Voltage**
- **Industrial Temperature Range: -40°C to 125°C**
- **Easy Straight-through Routing Packages**

APPLICATIONS

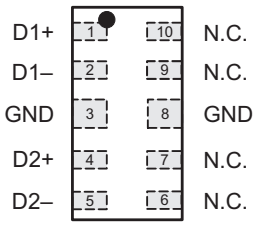
- **HDMI1.4**
- **HDMI2.0 (TPD1E05U06)**
- **USB3.0**
- **MHL**
- **LVDS Interfaces**
- **DisplayPort**
- **PCI Express**
- **eSata Interfaces**

DESCRIPTION

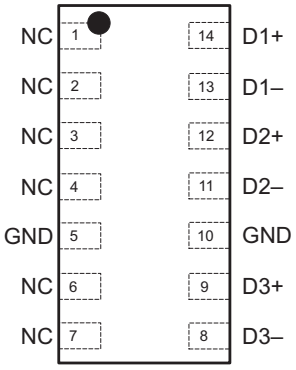
The TPDxE05U06 is a family of unidirectional ESD protection devices with ultra low capacitance. This family of devices is constructed with a central ESD clamp with two hiding diodes to reduce the capacitive loading. They are rated to dissipate ESD strikes above the maximum level specified in the IEC61000-4-2 level 4 international standard. Its ultra low loading capacitance makes it ideal for protecting any high-speed signal pins.



DPY
TOP VIEW
1 mm x 0.6 mm x 0.35 mm
(0.65-mm pitch)



DQA
TOP VIEW
2.5 mm x 1 mm x 0.5 mm
(0.5-mm pitch)



RVZ
TOP VIEW
3.5 mm x 1.35 mm x 0.5 mm
(0.5-mm pitch)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Functional Block Diagram

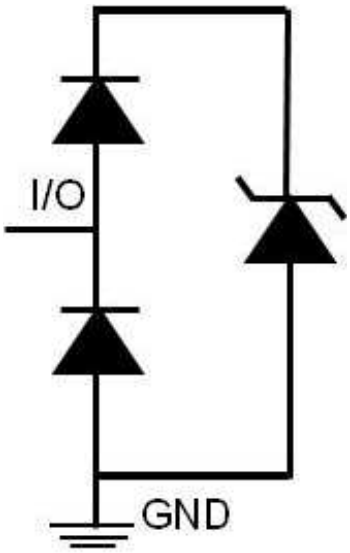


Figure 1. Single Channel Schematic Diagram

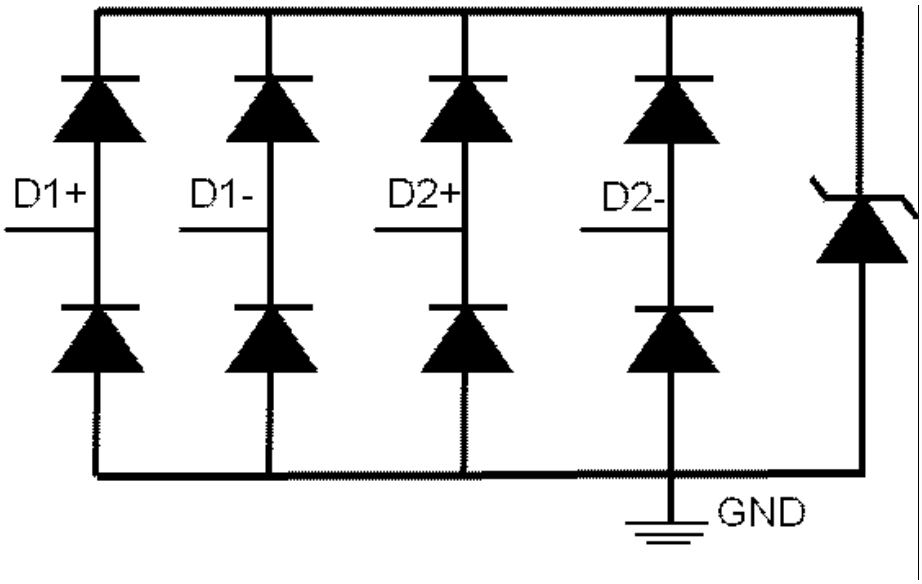


Figure 2. Quad Channel Schematic Diagram

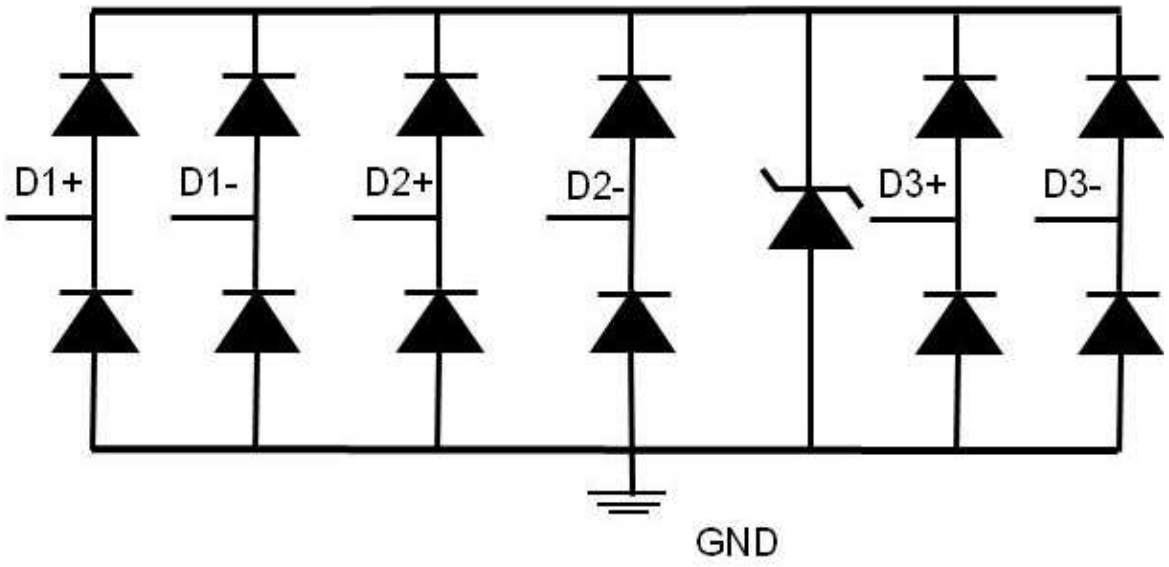


Figure 3. 6-Channel Schematic Diagram

Single Channel Terminal Functions

TERMINAL		TYPE	DESCRIPTION	USAGE
NAME	PIN NO.			
I/O	1	I/O	ESD protected channel	Connect pin 1 as close to the connector as possible
GND	2	GND	Ground	Connect to ground

Quad Channel Terminal Functions

TERMINAL		TYPE	DESCRIPTION	USAGE
NAME	PIN NO.			
D1+	1	I/O	ESD protected channel	Connect it as close to the connector as possible
D1–	2	I/O	ESD protected channel	Connect it as close to the connector as possible
D2+	4	I/O	ESD protected channel	Connect it as close to the connector as possible
D2–	5	I/O	ESD protected channel	Connect it as close to the connector as possible
NC	6, 7, 9, 10	NC	No connect	Used for optional straight-through routing from D+; otherwise can be left floating or grounded
GND	3, 8	GND	Ground	Connect to ground

Six Channel Terminal Functions

TERMINAL		TYPE	DESCRIPTION	USAGE
NAME	PIN NO.			
D1+	14	I/O	ESD protected channel	Connect it as close to the connector as possible
D1–	13	I/O	ESD protected channel	Connect it as close to the connector as possible
D2+	12	I/O	ESD protected channel	Connect it as close to the connector as possible
D2–	11	I/O	ESD protected channel	Connect it as close to the connector as possible
D3+	9	I/O	ESD protected channel	Connect it as close to the connector as possible
D3–	8	I/O	ESD protected channel	Connect it as close to the connector as possible
NC	1, 2, 3, 4, 6, 7	NC	No connect	Used for optional straight-through routing from D+; otherwise can be left floating or grounded
GND	5, 10	GND	Ground	Connect to ground

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
T_A	Operating free-air temperature range		–40	125	°C
T_{stg}	Storage temperature range		–65	155	°C
	ESD protection	IEC 61000-4-2 Contact Discharge(2)		±12	kV
		IEC 61000-4-2 Air-Gap Discharge(2)		±15	kV
I_{PP}	Peak pulse current (t_p = 8/20 µs)(2)			2.5	A
P_{PP}	Peak pulse power (t_p = 8/20 µs)(2)			40	W

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) Measured at 25°C.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 µA				5.5	V
V_{clamp}	Clamp voltage	I = 1A, TLP, I/O to ground(1)			10		V
		I = 5A, TLP, I/O to ground(1)			14		
		I = 1A, TLP, ground to I/O(1)			3		
		I = 5A, TLP, ground to I/O(1)			7		
R_{DYN}	DPY package dynamic resistance	I/O to GND(2)			0.65		Ω
		GND to I/O (2)			0.8		
	DQA package dynamic resistance	I/O to GND(2)			0.8		Ω
		GND to I/O(2)			0.8		
	RVZ package dynamic resistance	I/O to GND(2)			0.8		Ω
		GND to I/O(2)			0.8		
C_L	Line capacitance(3)	V_{IO} = 2.5 V, F = 1 MHz, I/O to GND	DPY package		0.42		pF
			DQA package		0.5		
			RVZ package		0.47		
C_{CROSS}	Channel to channel input capacitance	GND Pin = 0 V, F = 1 GHz, V_{BIAS} = 2.5 V, between channel pins			0.01	0.06	pF
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of channel input capacitance	GND Pin = 0 V, F = 1 GHz, V_{BIAS} = 2.5 V, channel_x pin to gnd – channel_y pin to gnd			0.05	0.07	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA		6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V			1	10	nA

(1) Transition line pulse with 100ns width, 200ps rise time.
(2) Extraction of RDYIN using least squares fit of TLP characteristics between I = 10 A and I = 20 A.
(3) Capacitance data is taken at 25°C.

Typical Characteristics

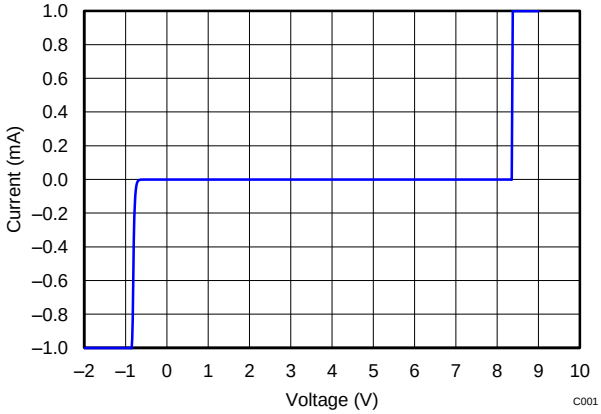


Figure 4. DC Voltage Sweep I-V Curve

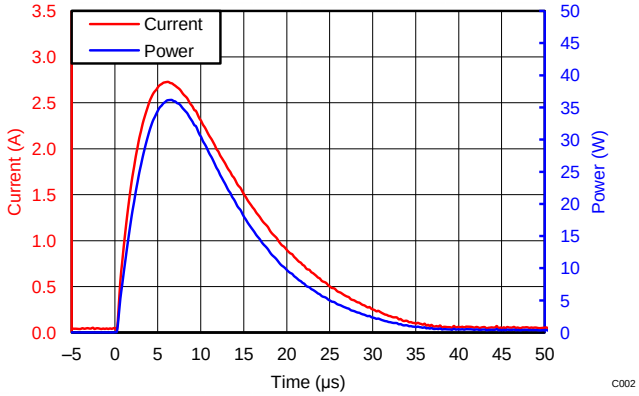


Figure 5. Surge Curve (tp = 8/20µs), Pin IO to GND

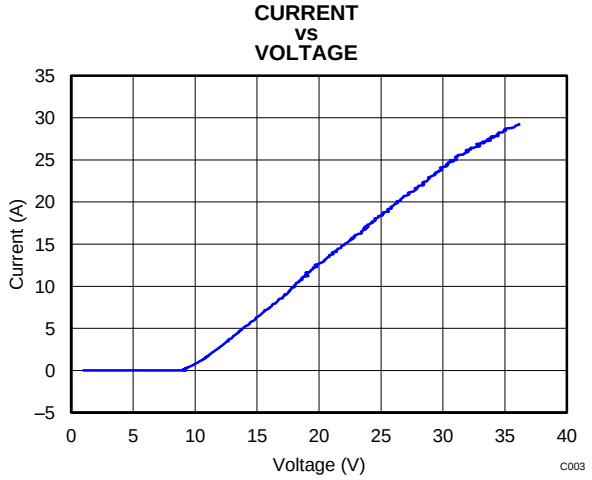


Figure 6. Positive TLP Plot IO to GND

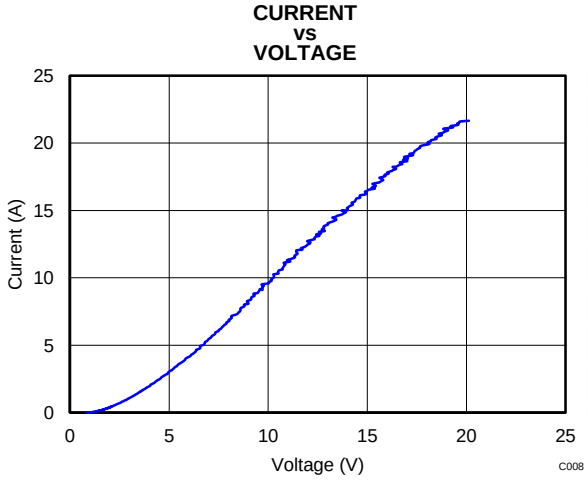


Figure 7. Negative TLP Plot IO to GND

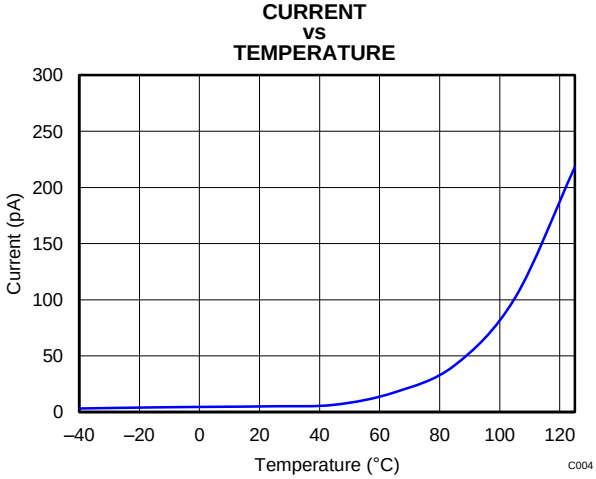


Figure 8. Leakage vs Temp

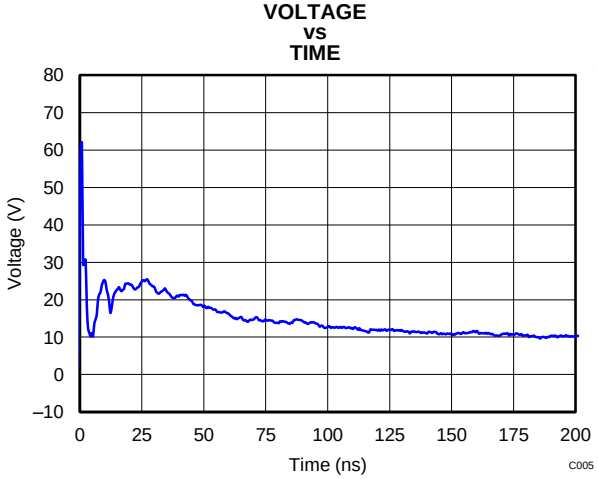


Figure 9. +8kV IEC Waveform

Typical Characteristics (continued)

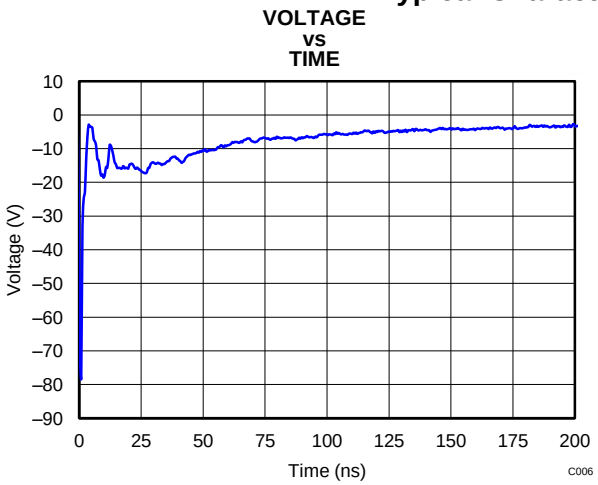


Figure 10. –8kV IEC Waveform

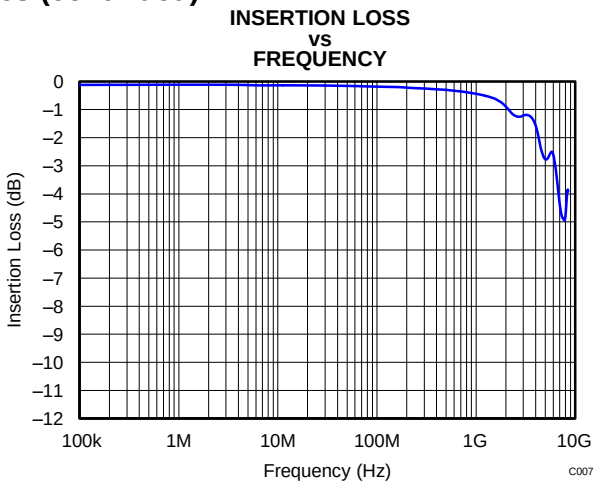


Figure 11. TPD1E05U06 Insertion Loss

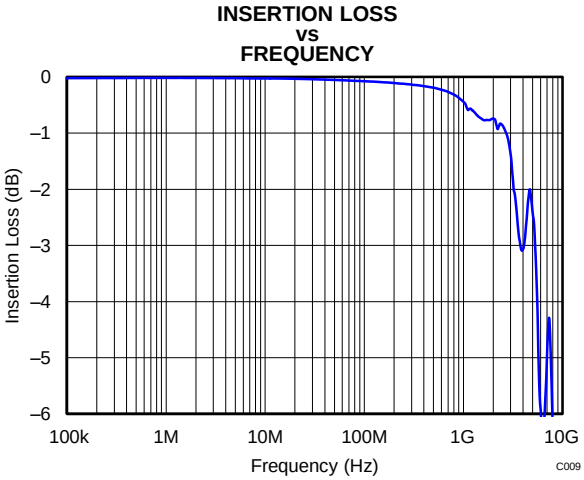


Figure 12. TPD4E05U06 Insertion Loss

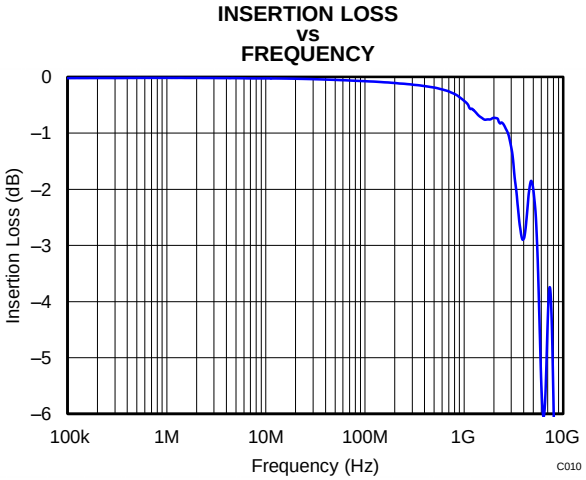
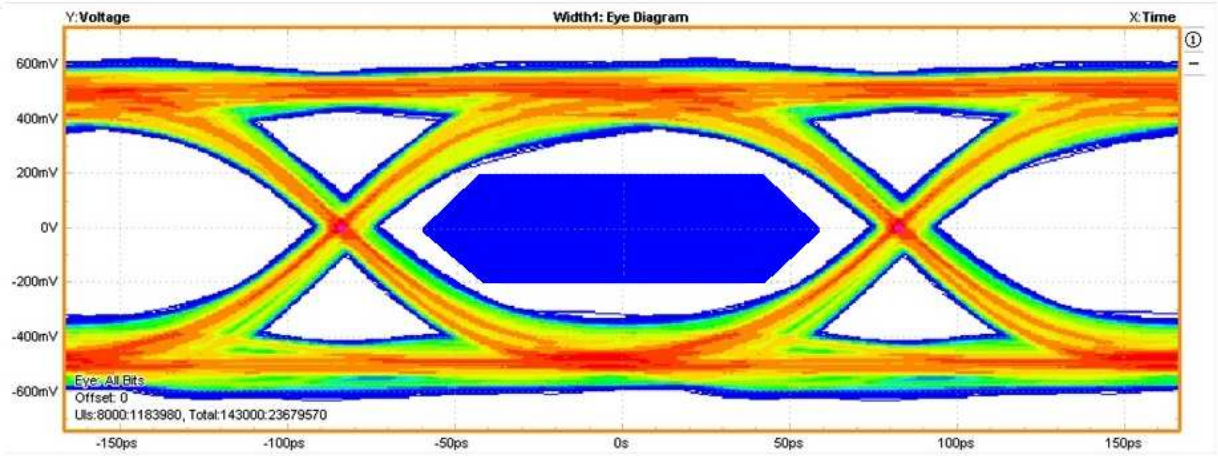


Figure 13. TPD6E05U06 Insertion Loss

Typical Characteristics (continued)

6 Gbps HDMI Eye Diagram



3.4 Gbps HDMI Eye Diagram

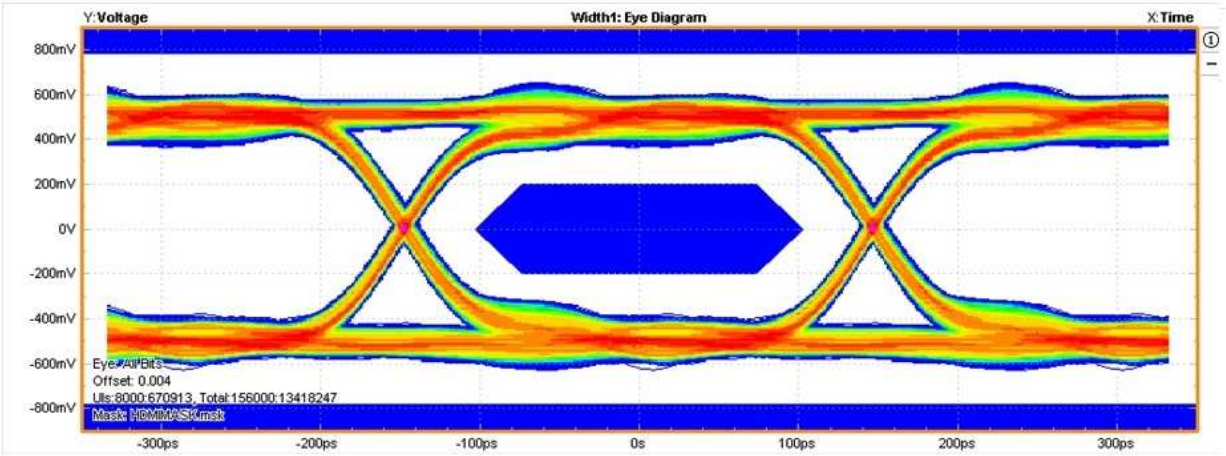


Figure 14. TPD1E05U06 Eye Diagrams

Typical Characteristics (continued)

3.4 Gbps HDMI Eye Diagram

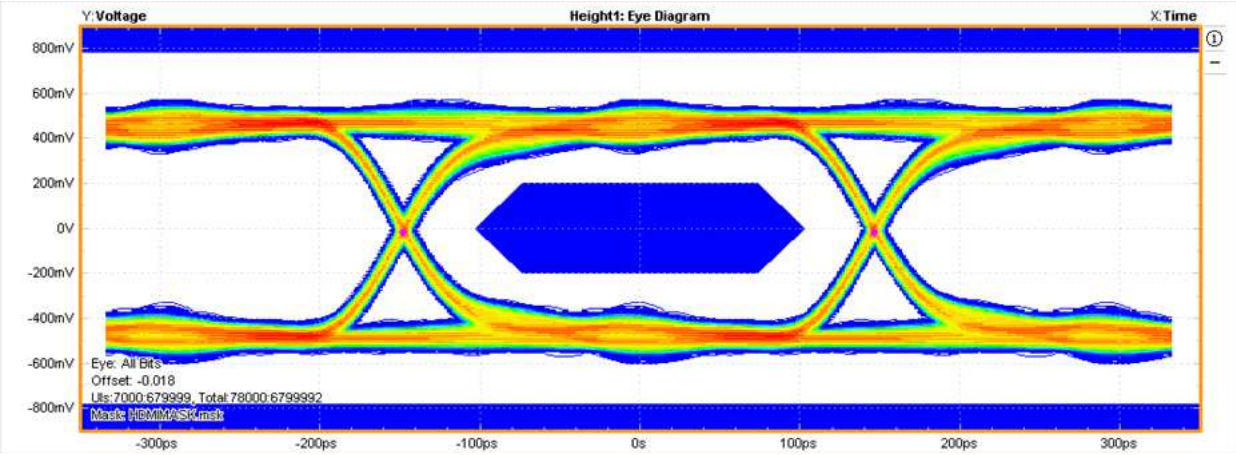


Figure 15. TPD4E05U06 Eye Diagram

3.4 Gbps HDMI Eye Diagram

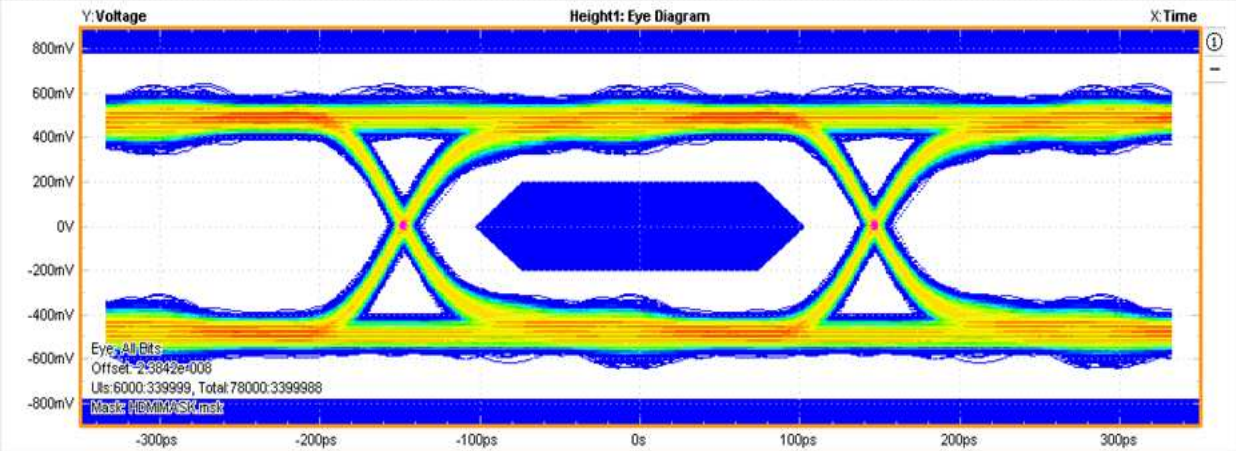


Figure 16. TPD6E05U06 Eye Diagram

REVISION HISTORY

Changes from Original (December 2012) to Revision A **Page**

- Added TPS2EUSB30A part to document. 1

Changes from Revision A (December 2012) to Revision B **Page**

- Added Insertion Loss Graphic. 6
- Added Eye Diagrams. 8

Changes from Revision B (January 2013) to Revision C **Page**

- Changed IO Capacitance range 1
- Changed test conditions and typ values for V_{clamp} 5
- Added typ R_{DYN} values for DQA and RVZ packages 5
- Added C_L values for DQA and RVZ packages 5
- Changed table note (1) 5
- Changed CURRENT vs VOLTAGE graphic 6
- Changed Insertion Loss graphic 6
- Changed HDMI Eye Diagrams 8

Changes from Revision C (March 2013) to Revision D **Page**

- Updated Title. 1
- Removed Ordering Information table. 2

Changes from Revision D (August 2013) to Revision E **Page**

- Updated document formatting. 1
- Added additional application. 1

Changes from Revision E (November 2013) to Revision F **Page**

- Updated pin out image. 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E05U06DPYR	ACTIVE	X2SON	DPY	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1	Samples
TPD1E05U06DPYT	ACTIVE	X2SON	DPY	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1	Samples
TPD4E05U06DQAR	ACTIVE	SON	DQA	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BRL	Samples
TPD6E05U06RVZR	ACTIVE	UQFN	RVZ	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BVL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

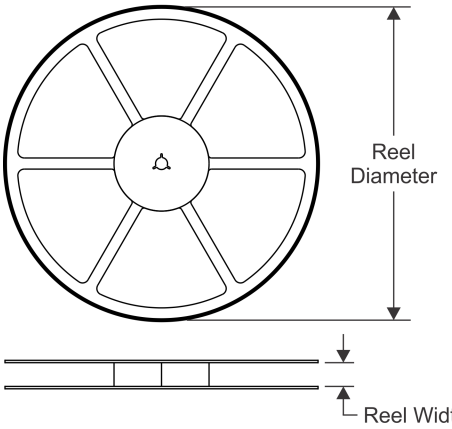
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

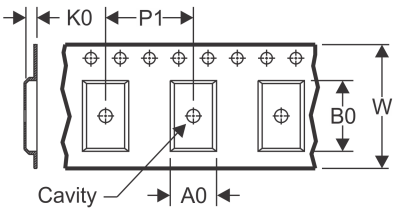
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

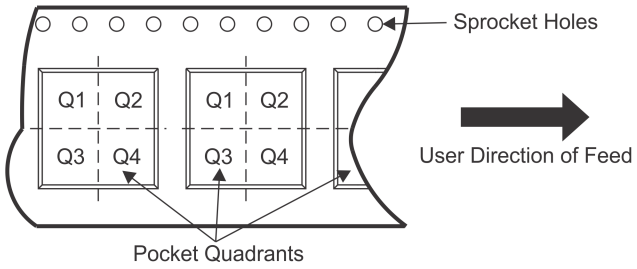


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

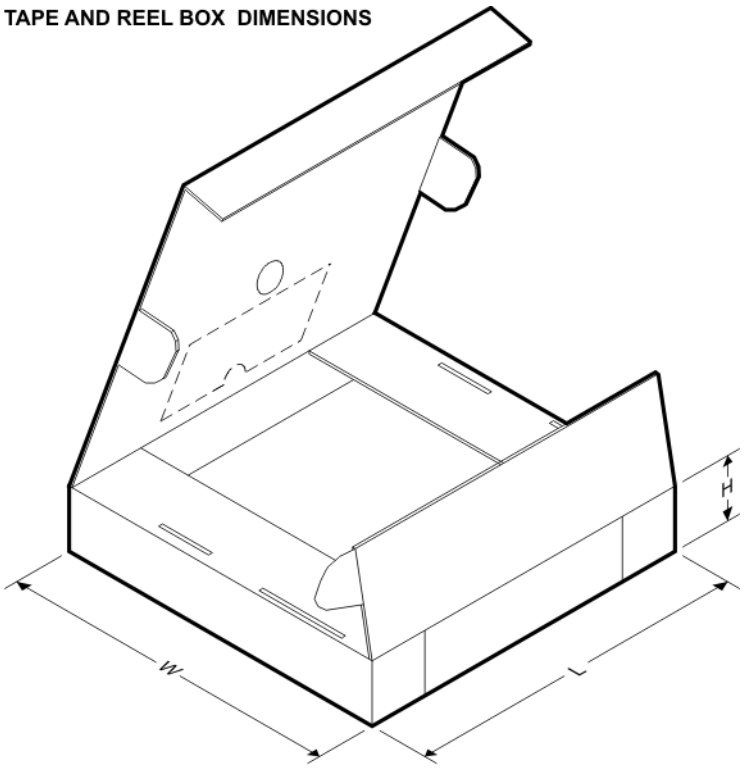
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E05U06DPYR	X2SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	4.0	8.0	Q1
TPD1E05U06DPYT	X2SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	4.0	8.0	Q1
TPD4E05U06DQAR	SON	DQA	10	3000	180.0	9.5	1.23	2.7	0.7	4.0	8.0	Q1
TPD6E05U06RVZR	UQFN	RVZ	14	3000	180.0	13.2	1.65	3.8	0.7	4.0	12.0	Q1

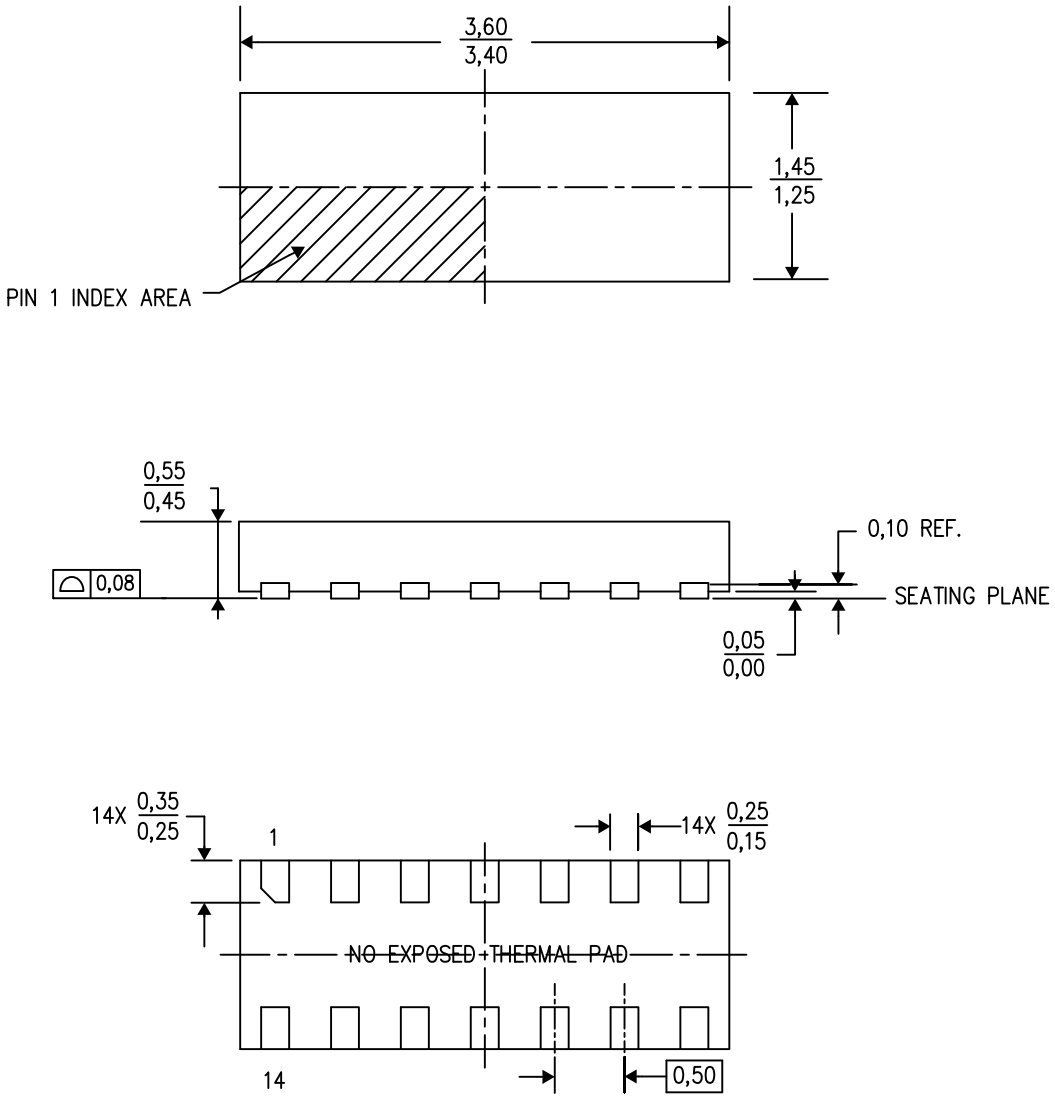
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E05U06DPYR	X2SON	DPY	2	10000	180.0	180.0	30.0
TPD1E05U06DPYT	X2SON	DPY	2	250	180.0	180.0	30.0
TPD4E05U06DQAR	SON	DQA	10	3000	180.0	180.0	30.0
TPD6E05U06RVZR	UQFN	RVZ	14	3000	180.0	180.0	30.0

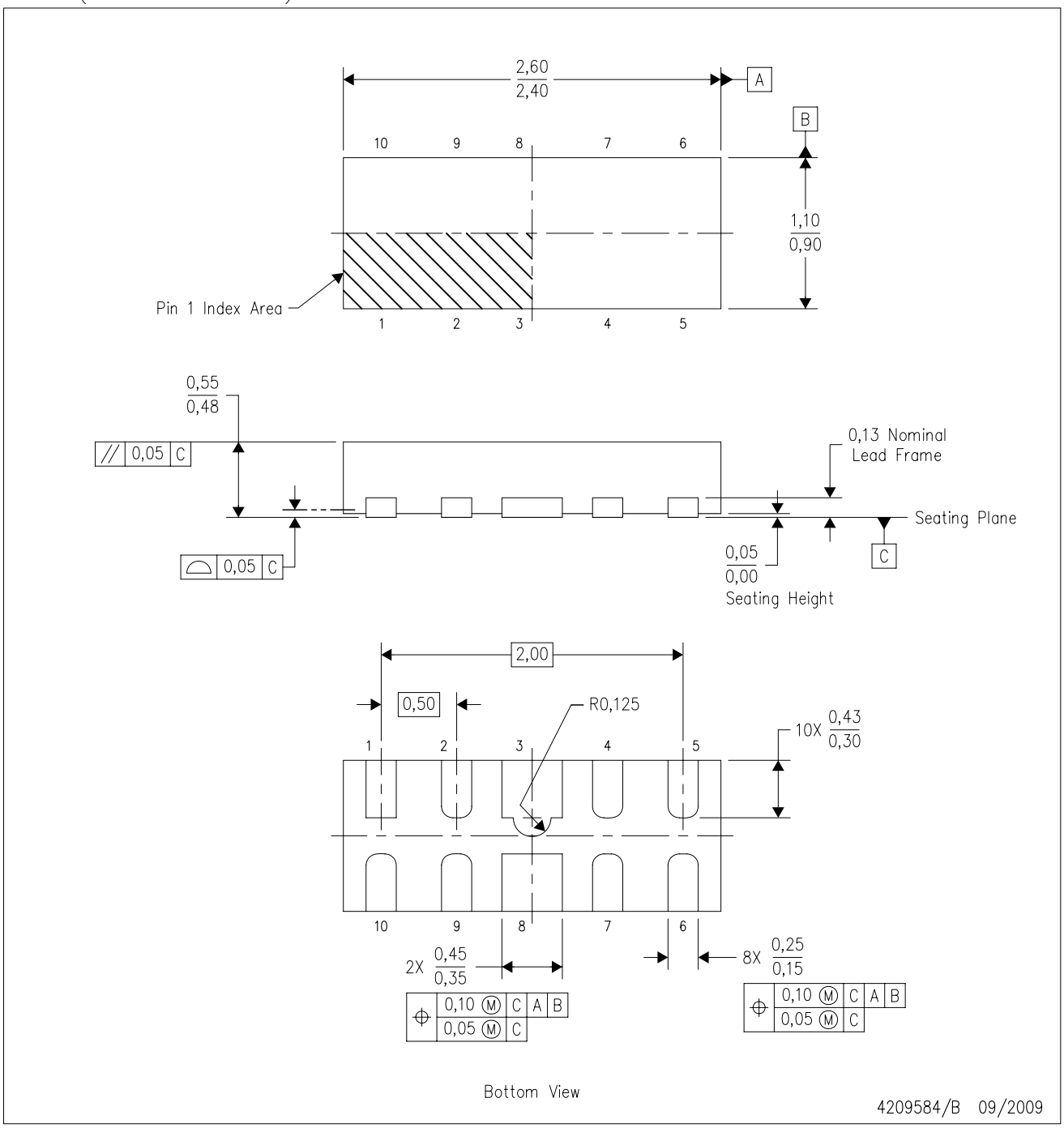
RVZ (R–PUQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



4218112/A 09/12

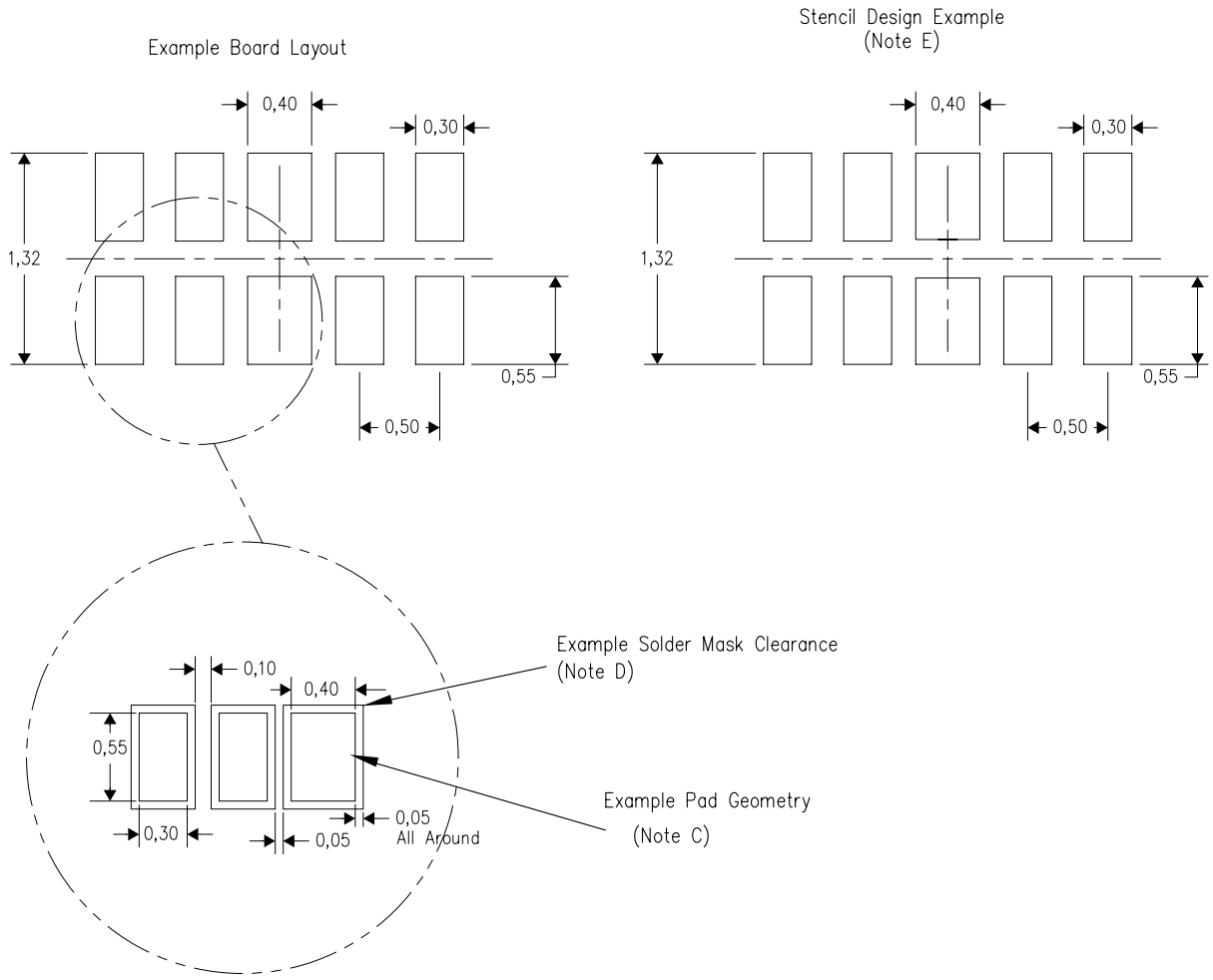
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

DQA (R–PSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



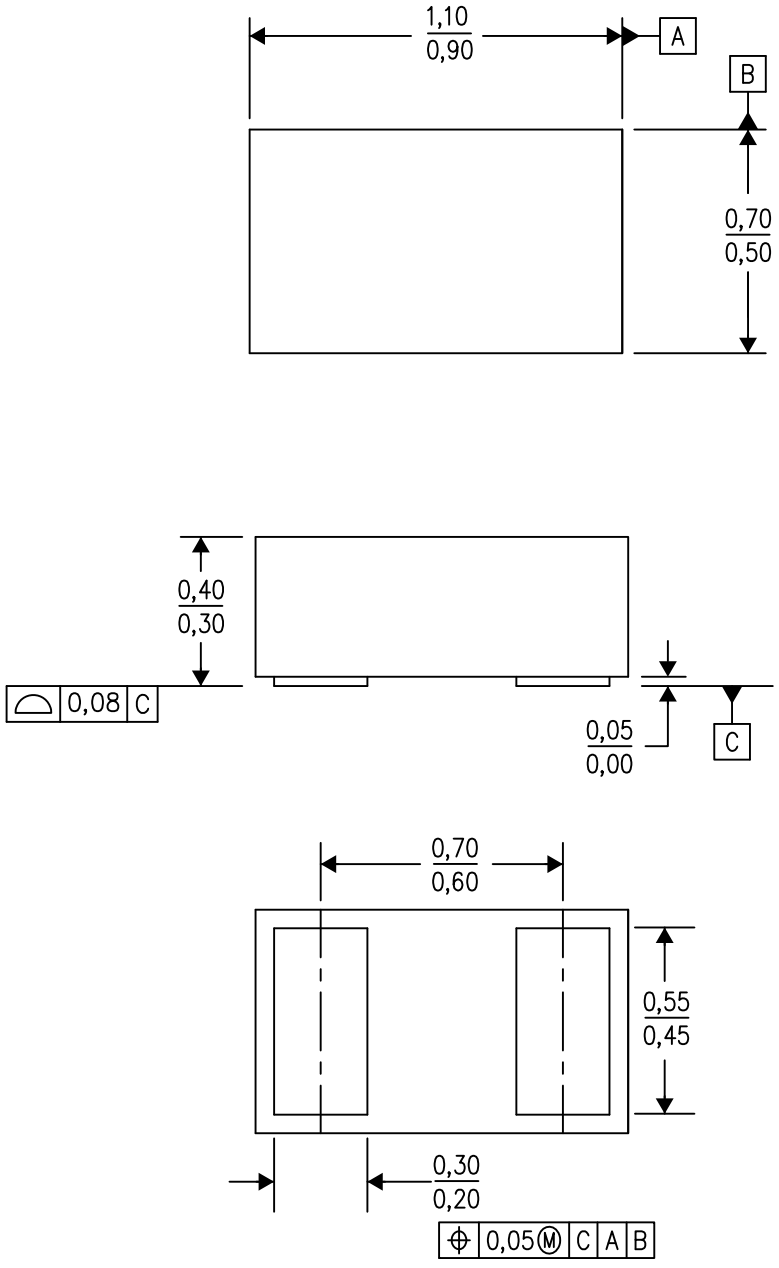
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQA (R–PUSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DPY (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

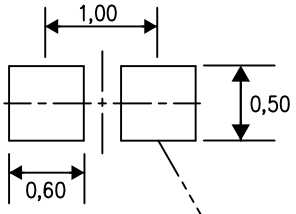


4211012/B 08/12

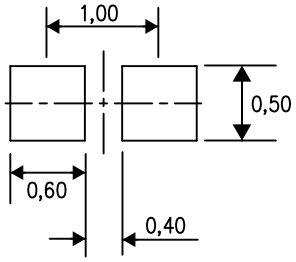
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

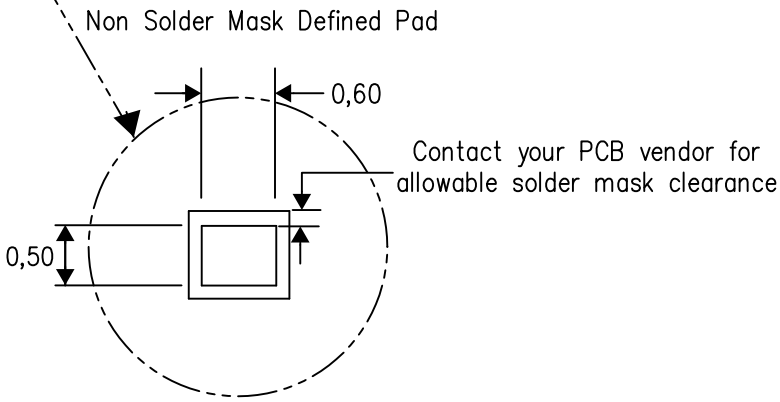
DPY (S–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)





4215270/A 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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