National Semiconductor

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TP3094 COMBO®
Quad PCM Codec/Filter

General Description

The TP3094 is a monolithic PCM Codec and Filter device implemented using a digital signal processing architecture. It provides four voice channels, combining transmit bandpass and receive low pass channel filters with companding A-law or m-law PCM encoders and decoders. The device is fabricated using National's advanced CMOS process.

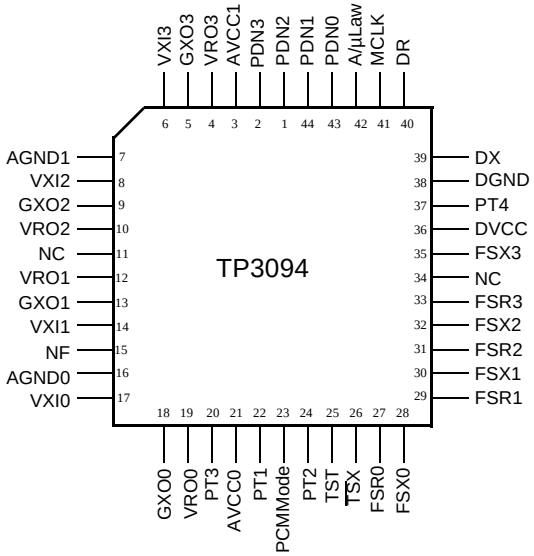
The device includes anti-aliasing filters and sigma-delta converters dedicated to each channel, and by a common signal processing unit which performs all the remaining filtering and processing for the four channels.

The TP3094 includes a flexible PCM digital interface, which allows the device to be connected to PCM busses of different formats. It can also be connected with other TP3094 devices in a cascade fashion, for a system with up to 128 POTS interfaces (when a 2.048MHz PCM bus is used).

Features

- Handles four voice channels
- Complete Codec and Filter system including:
  - Transmit and receive channel filters
  - A-law or µ-law companding encoder/decoder
- Power down mode for low power consumption
- Compatible to standard time division multiplexed PCM bus
  - 8 bit mode, frame signal from external reference
  - 32 bit mode, internal TSA, with consecutive TS
- Up to 128 channels (32 devices) can be cascaded
- Programmable functions (common for all 4 channels):
  - A-law or µ-law
  - Single MCLK clock,automatically selectable from 8.192MHz, 4.096MHz, 2.048MHz and 1.536/1.544MHz
  - Digital and Analog loopback test modes
- Designed for CCITT and LSSGR applications
- Single +5V power supply
- 44 lead PLCC surface mount package
- Maximize line card circuit density
- Use in Central Office, Loop Carrier, and PBX equipment subscriber line and trunk cards
- Wide operating temperature range -40°C to 85°C

Connection Diagram



Order Number TP3094V
See NS Package V44A

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Simplified Block Diagram

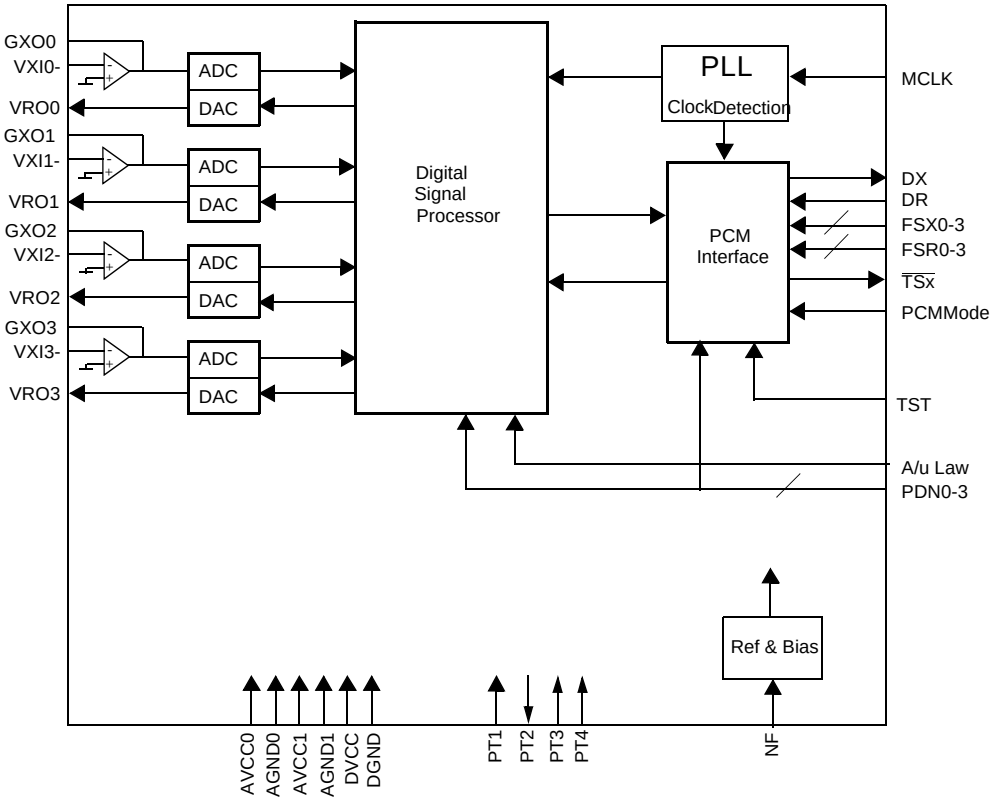


FIGURE 1. Simplified block diagram

Pin Descriptions

MCLK (input)
Master and PCM bit clock input. Must be either 1.536MHz/1.544MHz, 2.048MHz, 4.096MHz or 8.192MHz. Its value is automatically detected internally on power up with the valid frame sync input.

AVCC0, AVCC1
Positive supply pins for the analog circuitry. AVCC0 is for channel 0 and channel 1. AVCC1 is for channel 2 and channel 3.
AVCC0=AVCC1=+5V ±5%. These two pins should be connected together outside the device.

AGND0, AGND1
Analog ground. All analog signals are referenced to AGND0 and AGND1. AGND0 is the analog ground for channel 0 and channel 1. AGND1 is the analog ground for channel 2 and channel 3. These two pins should be connected together outside the device.

DVCC
Positive supply for the digital circuitry.
DVCC=+5V ±5%.

DGND
Digital ground. All logic signals are referenced to DGND. This ground has to be connected to the ground of other digital devices at board level.

Analog ports

VXI0-, VXI1-, VXI2-, VXI3- (inputs)
Inverting analog inputs of the transmit input amplifiers of channels 0-3. They are referenced to an internal reference voltage of about 2.4V.

GXO0, GXO1, GXO2, GXO3 (outputs)
Outputs of the transmit input amplifiers of channels 0-3. They are referenced to an internal reference voltage of about 2.4V

VRO0, VRO1, VRO2, VRO3 (ouputs)
Analog outputs of the receive amplifiers for channels 0-3. They are referenced to an internal reference voltage of about 2.4V

PCM Port

DX (ouput)
Transmit PCM data output. Serial PCM data is shifted out on the rising edge of MCLK during the assigned transmit time-slot. Tristated when the assigned transmit time-slot is not active.

$\overline{\text{TSx}}$ (ouput)
Open drain output that pulses low during the assigned transmit time-slots (for all four channels).

DR (input)
Receive PCM data input. Serial PCM data is shifted into the device on the falling edge of MCLK during the assigned receive time-slot.

FSX0, FSR0 (inputs)
Transmit and Receive Frame synchronization inputs for channel 0. They identify the beginning of a new frame in the transmit and receive direction. They are 8 KHz logic signals, and must be synchronous to MCLK. Short Frame Sync and Long Frame Sync are both supported.
In 32-bit mode these signals constitute the 8kHz reference for all channels. Only Short Frame Sync is supported in 32-bit mode.

FSX1, FSR1 (inputs/outputs)
Transmit and Receive Frame synchronization inputs for channel 1.
In 32-bit mode these pins become outputs and generate a frame sync signal with the last bit of the 32-bit stream, in order to allow to cascade another TP3094 in 32-bit mode. FSX1 is the Transmit Frame output and FSR1 is the Receive Frame output.

FSX2,FSX3, FSR2,FSR3 (inputs)
Transmit and Receive Frame synchronization inputs for channel 2 and 3. These pins are recommended to be connected to analog ground when in 32-bit mode.

A/u LAW select (input)
A/u law select. Through this pin either A-law (+5V) or u-law (0V) is selected.

PDN0-3 (input)
Power Down control signals. Each channel has a dedicated Power Down input. When active high, these pins set the low power mode, shutting down most of the circuitry dedicated to it and reducing the power consumption. The relative analog outputs VROi and GXOi, and the digital output DX are put in high impedance.

TST (input)
Test Modes Enable. When active (HIGH), together with the PDNi pins selects one of the available test modes (see the text for a full description of these modes).

PCMMode (input)
PCM Mode selection. When this signal is LOW (0V), the 8 bit mode is selected and each channel

Pin Descriptions (continued)

expects its individual transmit and receive frame signal. When it is HIGH, the 32 bit mode is selected; in this mode FSX0 and FSR0 are used as framing signals and the TS are allocated consecutively from these frames, starting from Ch0 to Ch3. In this mode FSX1 and FSR1 become outputs and produce 1 bit long frame signals with the last bit of the 32 bit stream. These Frame signals can be used to cascade another device in 32 bit mode.

NF
Noise Filter Pin. For optimal noise rejection a 100nF capacitor must be connected between this pin and the analog ground AGND0.

PT1, PT2, PT3, PT4 (inputs)
These pins are used by National for internal manufacturing test. They must be connected to digital ground for normal device operation.

NC
All NC pins must be connected to nearest analog ground, to reduce the device noise sensitivity.

Functional Description

The TP3094 performs the complete CODEC/filter functions for four voice channels using a digital signal processing architecture. MCLK provides the clock reference to the whole circuitry and the bit clock for the PCM bus. Its value can be either 8.192MHz, 4.096MHz, 2.048MHz or 1.536/ 1.544MHz, and it is automatically selected internally. The TP3094 handles the conversion between the analog signals on the subscriber line and the PCM data samples on a PCM highway. Digital filters are used to band-limit the voice signals.
The device can work in a 8 bit mode where each channel has an independently selected Time Slot, or in the 32 bit mode, where the four channels use four consecutive Time Slots. The time-division multiplexed PCM data is transferred to the PCM highway through the standard serial PCM bus.
Each channel has its dedicated Power Down input.

Power Initialization
When power is first applied to the device, power-on reset circuitry initializes the device and places it in the power down state. All non-essential circuits are de-activated. PCM output DX and analog outputs VRO_{0-3} are placed in the high impedance state, while FSX1 and FSR1 outputs are held low (in case 32-bit mode is selected). In the power down mode, power consumption is reduced to a minimum, typically 2mW. The device will remain in this state as long as no MCLK is applied and no Frame Signal is applied (just FSX0 and FSR0 in case of 32-bit mode).
For each channel, when the PDN input is not active, MCLK is applied, and a FS (receive or transmit) pulse is running, the device enters the active power up mode. The MCLK frequency is detected with any available FS signal; the clock rate detection may last for up to 4ms, after which the device is ready for powering up**.** Analog and PCM output signals will be available after a few frames; it will take about 100ms until the first activated channel is fully functional.
The device will only power up when at least one of the FS signals and the MCLK signal are in a valid frequency ratio.

Power Down and Reset
When one channel is in Power Down Mode, the DX output will remain in high impedance state and the input on the DR will be ignored when its FS signal is active; the analog output VRO will be in high impedance.
Each channel will enter the power down mode when at least one of the following conditions occurs

- The PDN signal is active for more than 16 MCLK cycles (and TST is not active at the same time)
- More than 4 pulses of the respective FS are missing.
- MCLK is missing for a 12us.

When the PDN input is active (HIGH) for at least 16 MCLK clock cycles, the channel will go into power down mode and reset its state within a frame sync. The channel will recover from Power Down, after having detected the PDN signal inactive (LOW) for at least 16 MCLK clock cycles and after 1 frame sync pulse.
This power down mode will work only in presence of the master clock at the pin MCLK.

When both the transmit and receive frame sync of a channel are missing the channel will go into Power Down Mode (if only one of them is missing the channel will not go into Power Down). A maximum of 32 frame sync pulses must be missing for power down and the channel will achieve its reset state after 32.5us. The channel will recover from power down, within the time of 4ms after the frame syncs (transmit or receive) will be active.
When the device is in 32-bit mode, missing FSX0, FSR0 for 512us, will force all channels in power down mode.

When the master clock MCLK is missing, all the channels will go into the Global Power Down Mode, with the lowest possible power consumption. The device will recover from this mode, when the clock signal comes back (and at least one frame sync is present), and then the active channels will operate after less than 100ms.
The device will go into the same Global Power Down Mode when all the frame syncs (of all the channels, in case of 8bit mode, the FSX0, FSR0 in case of 32-bit mode) are not present or when all 4 PDN signals are active. The recovery time from this mode for the first active channel is less than 100ms.

Transmit Section

The transmit section input is an operational amplifier, with provision for gain adjustment using two external resistors. Only the inverting input is provided (together with the output), this allows, beside the adjustment of the gain, to implement the echo balance function with external passive components.
The opamp drives the antialiasing input filter, followed by the A to D converter, which provides the digital input to the signal processing unit.
The signal processing unit accepts the signal samples from each channel input stage, performs the necessary decimation and filtering function, PCM compression and provides the eight bit samples to the PCM interface block.
The analog input is dc biased at the value of 2.4V. A DC decoupling is necessary between this input and the SLIC output. The maximum analog signal level, at the op-amp output, is 1.12Vrms.
Maximum recommended transmit gain is 20dB (10x).

Receive Section

This section takes the 8 bit samples from the PCM interface block and performs all the signal processing functions, such as PCM expansion according to the ALaw or uLaw and signal filtering. Then, for each channel it drives the Digital to Analog converter, through the proper interpolation stages and filters. Finally the signal is filtered and buffered to the output receive pin. The maximum output level voltage on the VRO pins on a load of 5kOhm+100pF is 1.12Vrms.

PCM Interface

The PCM interface consists of the following signals

- DX, DR - transmit and receive digital signals, carrying the pcm samples
- FSX0-3, FSR0-3 - transmit and receive frame signals
- $\overline{TSX}$ - output time slots signal, indicating the time slot occupied on the DX by the device
- PCMMode - PCM interface select

PCMMode = HIGH	PCMMode = LOW
32 bit	8 bit

- A/uLaw - A-law/ u-law select signal
-

TABLE 1. A/uLaw Coding

A/uLaw = HIGH	A/uLaw = LOW
A-law	u-law

- MCLK - bit clock signal

MCLK is both the system master clock and the PCM bus bit clock, and it is selected internally to be either 8.192MHz, 4.096MHz, 2.048MHz, or 1.536/ 1.544MHz.
The internal clock selection is perfomed, based on the relative ratio between the frame signals (FS) and the clock signals. For proper functionality all the channel FS must have the same valid rate of 8kHz (giving a valid clock rate). In case one of the frame syncs runs other than 8kHz, the device will not function properly.
Each bit on DX is clocked out on the rising edges of the bit clock (MCLK), starting from the Most Significant Bit (Sign bit). Each bit on DR is clocked in on the falling edges of the bit clock, starting from the MSB.
The device may operate on to the PCM bus in two modes, selected by the input pin PCMMode; when PCMMode is “0V” the 8bit mode is selected and when PCMMode is “+5V” the 32-bit mode is selected.

Functional Description (continued)

8-bit Mode

In the 8-bit mode, PCM data is transferred independently for each of the four channels. Each channel has its dedicated transmit and receive frame signals, which determine the time-slots to be taken on the PCM bus. Both short sync and long sync frame are supported.

All the channels must have the same FS format (either short or long sync), in case a channel will have a valid frame with different FS format, the device will not function properly.

In the short sync, the frame signals must be one bit long; with FSX high during a falling edge of MCLK, the next rising edge of MCLK enables the DX tristate output buffer, which will output the sign bit. The following 7 rising edges clock out the remaining 7 bits, and the next rising edge (9th) disables the DX output. With FSR high during a falling edge of MCLK, the next falling edge of MCLK latches in the sign bit. The following 7 negative edges of MCLK will then latch the remaining 7 bit of the incoming byte.

In the long sync frame, the Frame signals must be at least three bits long. The DX output buffer is enabled with the rising edge of FSX or on the rising edge of MCLK, whichever comes later, and the first bit (sign) is clocked out. The following 7 rising edges of MLCK clock out the remaining 7 bits. The DX output is disabled by the 9th rising edge of MCLK. A rising edge on FSR will cause the PCM data at DR to be latched in on the next falling edges of MCLK.

For timing diagrams refer to Fig.2, Fig.4, Fig.5 and Fig.6.

32-bit Mode

In the 32-bit mode, the four PCM data bytes of the four channels are treated as a single 32-bit data word. The PCM transfer is started by the positive pulses on the transmit or receive frame sync (FSX0, FSR0) inputs. The following 32 negative edges of MCLK will then latch the input PCM data at DR, for all 4 channel starting from channel 0; while the positive edges will clock out the transmit PCM data at DX, from channel 0 to channel 3. In this mode the pins FSX1 and FSR1 become the frame signal carry-out signals, providing a single-bit-long frame pulse during the last bit of the 32-bit stream and allowing another TP3094 to be connected in 32-bit mode.

In case any channel is powered down (through the PDN pin) during its assigned time slot the DX pin will be set in tristate and the DR signal will be ignored.

In case all the channels are placed in power down, the device will still generate the FS carry output on FSX1, FSR1. For timing diagrams refer to Fig.7 and Fig.8.

Test Modes

The TP3094 includes the following test modes

- digital loopback
- analog loopback
- DC conversion

These modes can be programmed per channel or for all 4 channels simultaneously.

The device is programmed into any test mode by exercising the pins TST, PDN0, PDN1, PDN2, PDN3 together. The signals to this pins must be stable for at least 16 MCLK cycles before the device enters any selected test mode. When exiting the test mode, the PDN must return to the previous state to resume the original operating state.

During any test mode (TST=1), it will not be possible to change the PU/PD state for any channel not involved in the test mode configuration (e.g. not in test mode). The channel(s) under test must be placed in power up prior the test mode selection, in case left in power down, any programmed test mode will not be operational.

When the device exits the test mode, normal operation will return, and the PU/PD programmability will be available, by the state of the PDN signals.

The programming of the test modes is according to the table below.

The digital loopback is a bit true feedback from the PCM highway to the PCM highway, performed exactly at the PCM internal interface. Each byte is looped back from RX to TX on the programmed time slot (FS). The analog output is forced to 0Vac level (typically 2.4Vdc), with low output impedance**.**

The analog loopback is performed from the output of the D/A converter (before the output amplifier) and the input of the A/D, so the RX signal is looped back towards the TX direction, through the device. The analog output is at 0Vac level, with high output impedance.

In the DC conversion mode, the channel under test is programmed to transfer any DC signal (within the available range) in the TX direction, from the analog GXO to the DX digital output, by

Functional Description (continued)

bypassing the low frequency filter.

Test Modes	TST	PDN0	PDN1	PDN2	PDN3	Description
Normal Operation	0	x	x	x	x	
Single Channel Digital Loopback	1	1	1	A0	A1	Ch. select with PDN2, PDN3
Single Channel Analog Loopback	1	0	1	A0	A1	Ch. select with PDN2, PDN3
Single Channel DC Conversion	1	1	0	A0	A1	Ch. select with PDN2, PDN3
4 Channels Digital Loopback	1	0	0	0	0	
4 Channels Analog Loopback	1	0	0	0	1	
4 Channels DC Conversion	1	0	0	1	0	
Invalid States	1	0	0	1	1	

Where A0, A1 select the channel under test, according to the following table

A0	A1	Channel Selected
0	0	Channel 0
1	0	Channel 1
0	1	Channel 2
1	1	Channel 3

Timing Diagrams

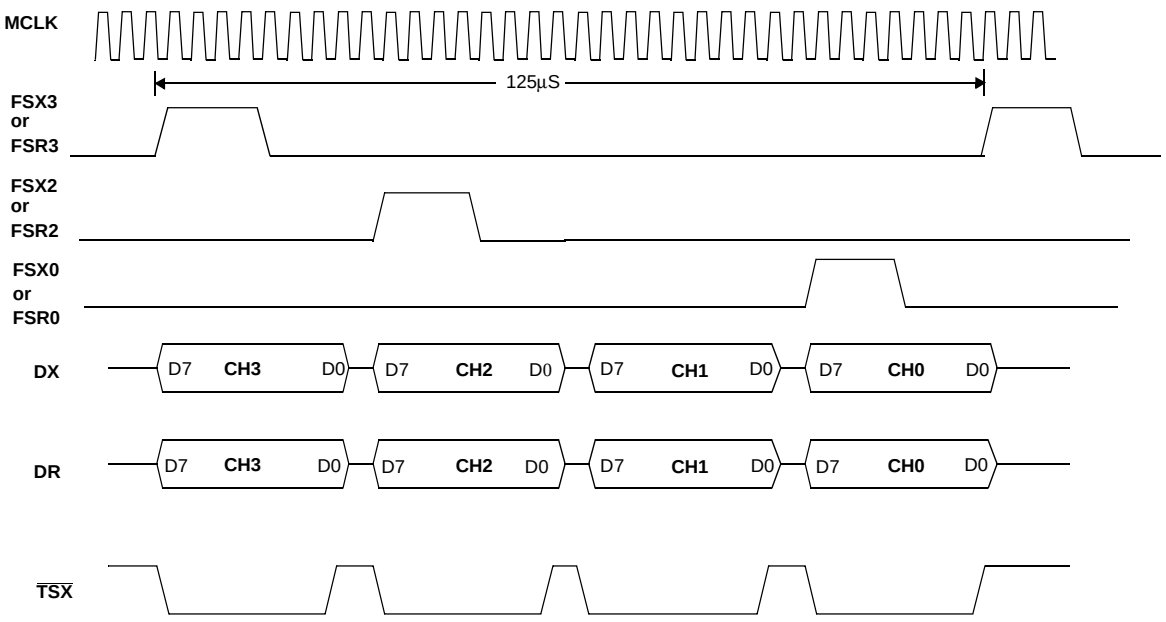


FIGURE 2. Timing diagram for PCM Interface, 8-bit mode (Long Frame Sync)

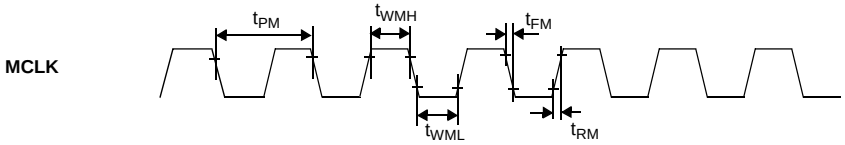


FIGURE 3. MCLK Timing

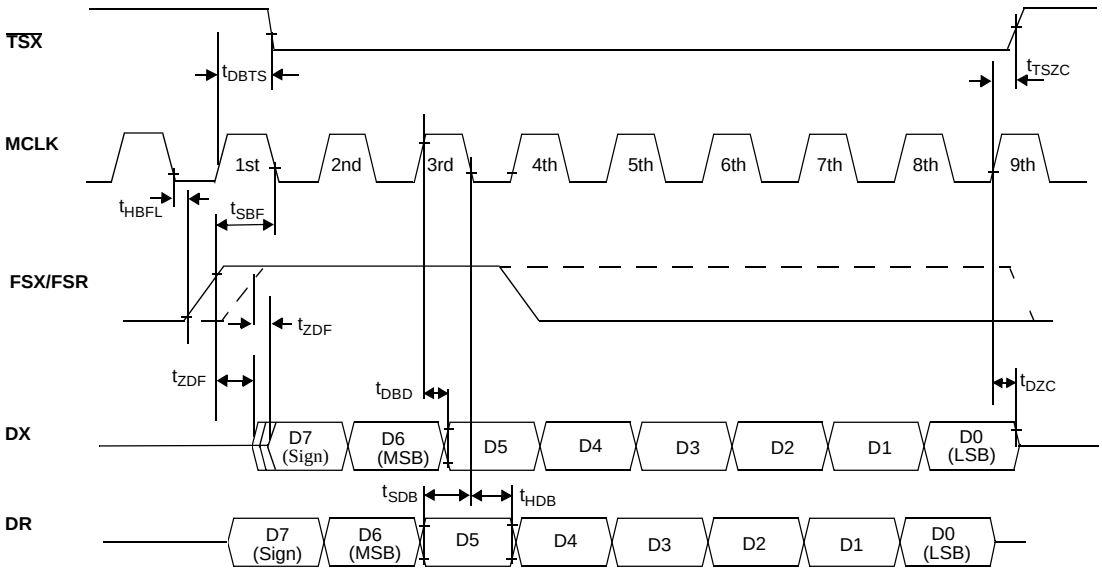


FIGURE 4. Timing diagram for PCM Interface, 8-bit mode (Long Frame Sync)

Timing Diagrams (continued)

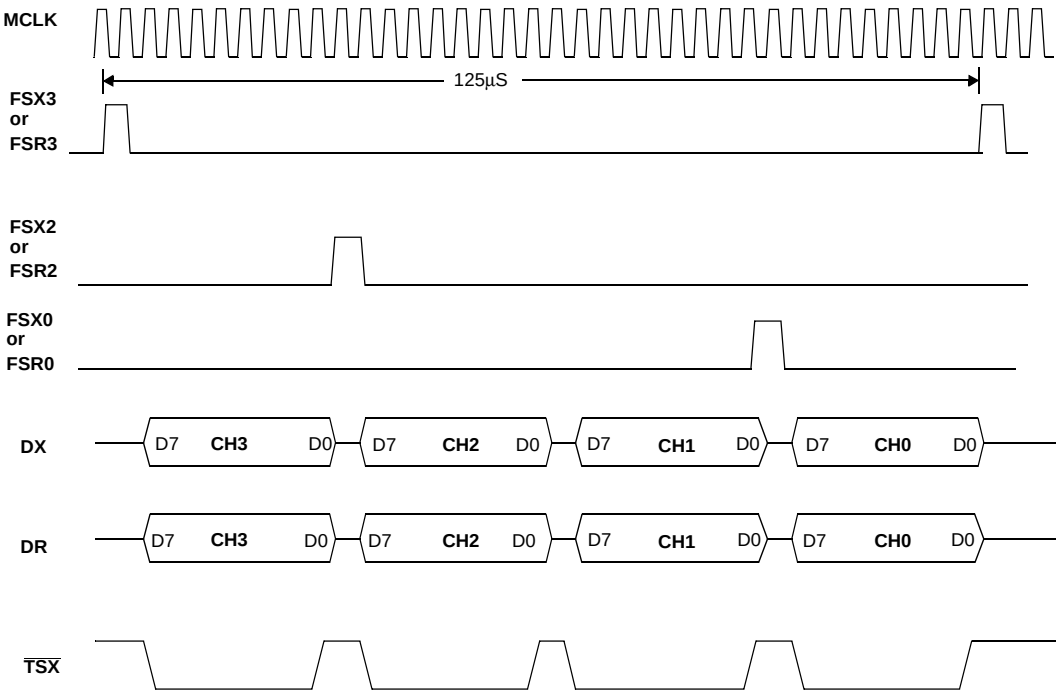


FIGURE 5. Timing diagram for PCM Interface, 8-bit mode (Short Frame Sync)

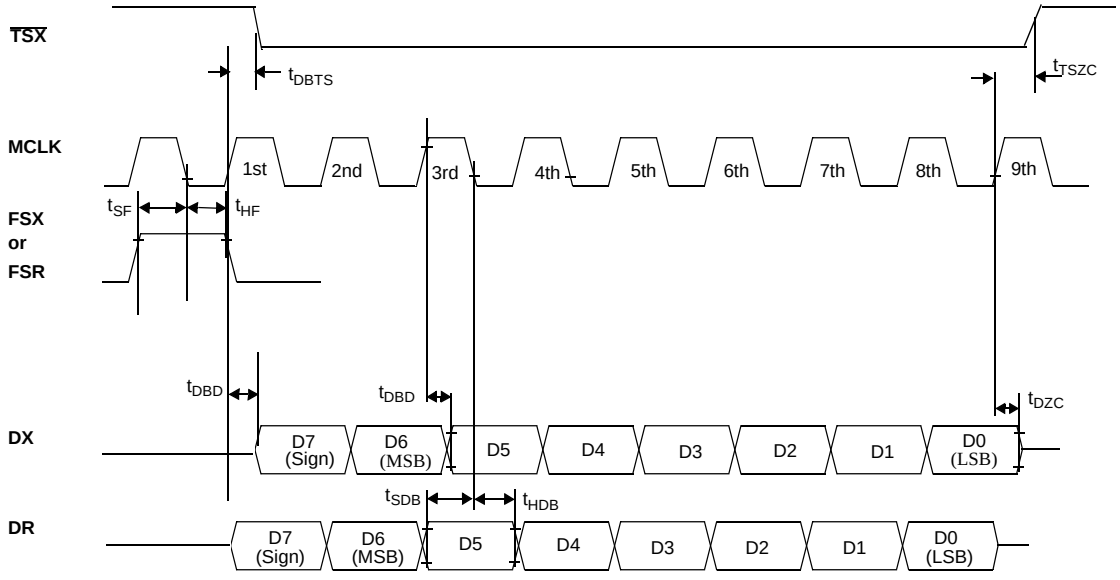


FIGURE 6. Timing diagram for PCM Interface, 8-bit mode (Short Frame Sync) for each channel

Timing Diagrams (continued)

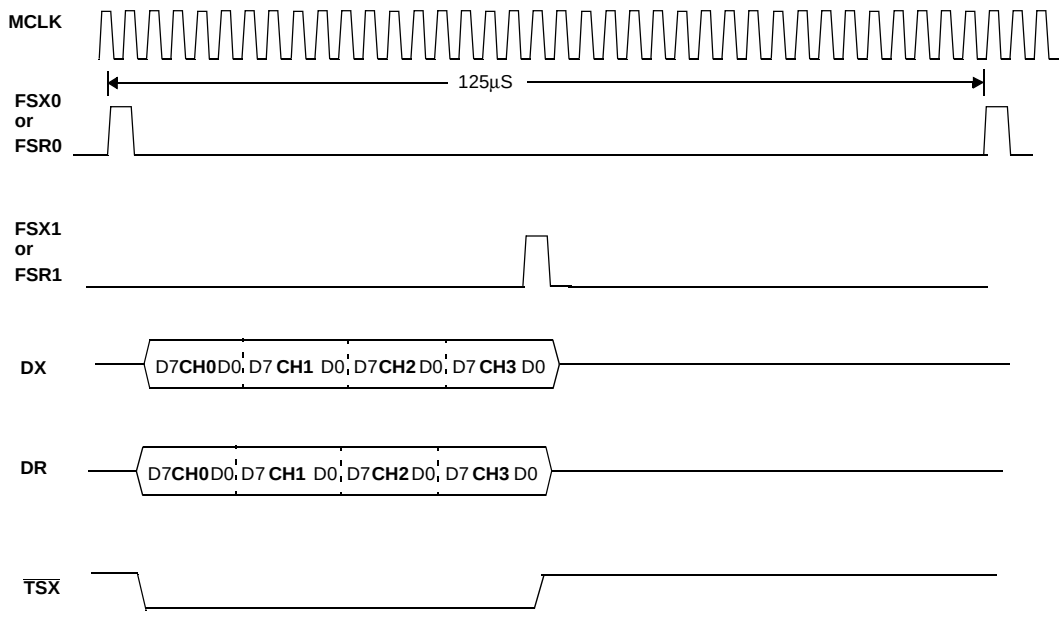


FIGURE 7. Timing diagram for PCM Interface, 32-bit mode

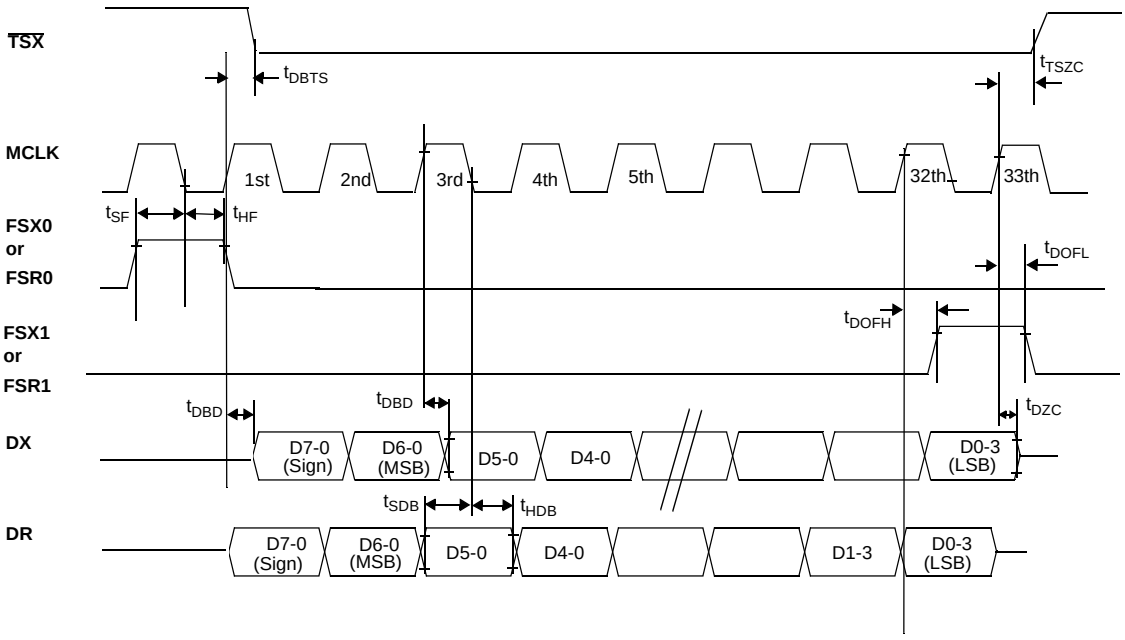


FIGURE 8. Timing diagram for PCM Interface, 32-bit mode

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to DGND	7V
Voltage at any digital inputs or outputs	V_{CC} +0.3V to DGND -0.3V
Voltage at any analog inputs or outputs	V_{CC} +0.3V to AGND-0.3V
Storage temperature range	-65^{o}C to +150^{o}C
Lead temperature(Soldering, 10 Sec)	260^{o}C
ESD (human body model)	2000 V
Latch-up immunity on any pin	200 mA

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC}(all supplies)=5.0V±5%, DGND=AGND=0V, T_A=-40°C to 85°C by correlation with 100% electrical testing at T_A=25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All digital signals are referenced to DGND, and all analog signals are referenced to AGND. Typical are specified at V_{CC}=+5V, T_A=25°C.

Digital Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input low voltage	All digital inputs			0.8	V
V_{IH}	Input high voltage	All digital inputs	2.2			V
V_{OL}	Output low voltage	IL=2mA			0.4	V
V_{OH}	Output high voltage	IL=-2mA IL=-100uA	2.4 3.5			V V
I_{IL}	Input low current	DGND<V_{IN}<V_{IL}, all digital inputs	-10		10	µA
I_{IH}	Input high current	V_{IH}<V_{IN}<V_{CC}, all digital inputs	-10		10	µA
I_{OZ}	Output current in high impedance state	DGND<V_O<V_{CC} (DX)	-10		10	µA
Ci	Input Capacitance				10	pF

Analog Interface

I_{XI}	Input leakage current	1V<V_{XI}<4V, all analog inputs in Power UP mode	-200		200	nA
R_{XI}	Input resistance	1V<V_{XI}<4V, all analog inputs	10			MΩ
C_{XI}	Input capacitance	1V<V_{XI}<4V, all analog inputs		10		pF
V_{CMXI}	Transmit input common mode voltage range		-10%	2.375	+10%	V
V_{CMXO}	Receive input common mode voltage range		-10%	2.375	+10%	V
R_{RO}	Output resistance	All analog outputs		5	10	Ω
R_{ROZ}	Output resistance in PDN		2000			Ω
RL_{RO}	Load resistance	0.7V<V_{RO}<4.1V, VROi	5000			Ω
CL_{RO}	Load capacitance	VRO			100	pF
A_VXA	Voltage Gain	VXI to GXO,RL on GXO>10kΩ	5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
RL_{GXO}	Load resistance	0.7V<V_{GX}<4.1V, GXOi	10000			Ω
CL_{GXO}	Load capacitance	GXO			50	pF
V_{RO}	RX output drive level	R_L=5000Ω	1.12			Vrms

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power Dissipation						
$I_{CC}0$	Power down current (all channels down)	Measured after having first achieved power-up state. MCLK=2.048MHz		0.9	1.5	mA
$I_{CC}1$	Power up active current (all channel active)	No load, MCLK=2.048MHz		35	50	mA
Amplitude Response						
	Absolute Levels	Nominal 0dBm0 level is 0dBm at the analog inputs/outputs		0.7746		V_{rms}
t_{max}	Virtual decision value defined per ITU G.711	Max overload level 3.17dBm0 (μ-law) 3.14dBm0 (A-law)			 1.116 1.112	 V_{rms} V_{rms}
G_{XA}	Transmit gain, absolute	T_A=25°C, V_{CC}=5V, Input at VXI=0dBm0 at 1015.625Hz	-0.15		0.15	dB
$G_{XAT/V}$	Cumulative Transmit gain Variation with supplies and temperature ranges	T_A=0°C to 70°C, V_{CC}=5V±5%, TA=-40°C to +85°C, V_{CC}=5V±5% Input at GXO=0dBm0 at 1015.625Hz	-0.2 -0.3		0.2 0.3	dB dB
G_{XR}	Transmit gain, relative to G_{XA}	f=16Hz f=50Hz f=60Hz f=200Hz f=300-3000Hz f=3300Hz f=3400Hz f=4000Hz f=4.6KHz and up (Note 2), measure response from 0 to 4000Hz	 -1.8 -0.15 -0.35 -0.7		-35 -30 -30 0 0.15 0.15 0 -14 -32	dB dB dB dB dB dB dB dB dB
G_{XAL}	Transmit gain variation with level	Sinusoidal test method, reference level = -10dBm0 at VXI GXO=-40dBm0 to +3dBm0 GXO=-50dBm0 to -40dBm0 GXO=-55dBm0 to -50dBm0	 -0.2 -0.4 -1.0		 0.2 0.4 1.0	 dB dB dB
G_{RA}	Receive gain, absolute	T_A=25°C, V_{CC}=5V±5% Input PCM level at DR=0dBm0 at 1015.625Hz	-0.15		0.15	dB
$G_{RAT/V}$	Cumulative Receive gain Variation with supplies and temperature ranges	T_A=0°C to 70°C, V_{CC}=5V±5%, T_A=-40°C to 85°C, V_{CC}=5V±5%, Input PCM level at DR=0dBm0 at 1015.625Hz	-0.2 -0.3		0.2 0.3	dB
G_{RR}	Receive gain, relative to G_{RA}	f=0-3000Hz f=3300Hz f=3400Hz f=4000Hz	-0.15 -0.35 -0.7		0.15 0.15 0 -14	dB dB dB dB

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G_{RAL}	Receive gain variation with level	Sinusoidal test method,				
		PCM level=-40dBm0 to +3dBm0	-0.2		0.2	dB
		PCM Level=-50dBm0 to -40dBm0	-0.4		0.4	dB
		PCM Level=-55dBm0 to -50dBm0	-1.0		1.0	dB

Note 2: Measure voiceband image signal, stimulus signal level is -25dBm0.

Distortion

STD_{XP}	Transmit signal to total distortion	Sinusoidal test method, A-law (psophometric filter), u-Law (C message filter), FSX=FSR,				
		f_{XI}=1015.625Hz	33			dB
		GXO=+3dBm0	36			dB
		GXO=0 to -30dBm0	29			dB
		GXO= -40dBm0	25			dB
		GXO= -45dBm0	20			dB
		GXO= -50dBm0	14			dB
		GXO= -55dBm0				
SFD_X	Transmit single frequency distortion	Sinusoidal test method, PCM code for all channels equals to positive zero, FSX=FSR, f_{XI}=1015.625Hz, GXO=0dBm			-46	dB
STD_{RP}	Receive signal to total distortion	Sinusoidal test method, A-law, (psophometric filter), u-Law (C message filter), FSX=FSR,				
		f=1015.625Hz,	33			
		PCM level=+3dBm0	36			dB
		PCM level=0 to -30dBm0	29			dB
		PCM level=-40dBm0	25			dB
		PCM level=-45dBm0	20			dB
		PCM level=-50dBm0	15			dB
		PCM level= -55dBm0				
SFD_R	Receive single frequency distortion	Sinusoidal test method, PCM code for all channels equals to 0dBm0, FSX=FSR, f=1015.625Hz, GXO=0Vrms			-46	dB
SOS_{RS}	Receive spurious out of band signals	Single frequency, PCM code for all channels equals 0 dBm0, 300Hz-3.4KHz, FSX=FSR, GXO=0Vrms				
		f=4.6KHz-7.6KHz			-30	dB
		f=7.6KHz-8.4KHz			-40	dB
		f=8.4KHz-100KHz			-30	dB

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Envelope delay distortion						
D_{XA}	Transmit delay, absolute	f=1400Hz,		275	330	µS
D_{XR}	Transmit delay, relative to D_{XA}	GXO=-10dBm0				
		f=500-600Hz		150	220	µs
		f=600-1000Hz		85	145	µs
		f=1000-2600Hz		50	100	µs
		f=2600-2800Hz		80	140	µs
D_{RA}	Receive delay, absolute	f=1400Hz,		112	220	µS
D_{RR}	Receive delay, relative to D_{RA}	PCM level=-10dBm0				
		f=500-600Hz	-40	-15		µs
		f=600-1000Hz	-40	-10		µs
		f=1000-2600Hz		75	90	µs
		f=2600-2800Hz		105	125	µs
		f=2800-3000Hz		145	175	µs
Noise						
N_{XP}	Transmit Idle channel noise, A-law	Psophometric weighted, PCM code for all channels equals to positive zero, FSX=FSR, GXO=0Vrms		-73	-69	dBm0p
N_{XC}	Transmit Idle channel noise, µ-law	C-message weighted, PCM code for all channels equals to alternating positive and negative zeros, FSX=FSR, GXO=0Vrms		12	16	dBrnC0
N_{RP}	Receive Idle channel noise, A-law	Psophometric weighted, PCM code for all channels equals to positive zero, FSX=FSR, GXO=0Vrms		-83	-79	dBm0p
N_{RC}	Receive Idle channel noise, µ-law	C-message weighted, PCM code for all channels equals to alternating positive and negative zeros, FSX=FSR, GXO=0Vrms		7	11	dBrnC0
N_{XR}	Analog to Analog Noise	DX connected to DR, f=0-100kHz FSX=FSR, GXO=0Vrms		-70	-53	dBm0
Power supply rejection						
$PPSR_X$	Positive power supply rejection, transmit	PCM code for all channels equals to positive zero, A-law, FSX=FSR, GXO=0Vrms, V_{CC}=5.0V+100mV_{rms}				
		f=0-4000Hz	40	45		dB
		f=4.6KHz-25KHz	40	45		dB
$PPSR_R$	Positive power supply rejection, receive	PCM code for all channels equals to positive zero, A-law, FSX=FSR, GXO=0Vrms, V_{CC}=5.0V+100mV_{rms}				
		f=0-4000Hz	40	45		dB
		f=4.6KHz-25KHz	40	45		dB

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Crosstalk						
CT_{R-X}	Receive to transmit crosstalk (Intra-channel Crosstalk)	PCM code for stimulated channel equals to 0dBm0, 300Hz-3.4KHz, PCM code for all other channels equals to positive zero, FSX=FSR, Measure PCM response.		-80	-75	dB
$CTFE_X$	Far end crosstalk with analog stimulus (Inter-channel crosstalk)	PCM code for all channels equals to positive zero, FSX=FSR, Stimulating signal GXO=0dBm0, f=750Hz All other channels GXO=$0V_{rms}$		-80	-73	dB
$CTNE_X$	Near end crosstalk with digital stimulus (Inter-channel crosstalk)	PCM code for stimulated channel equals to 0dBm0, f=750Hz, PCM code for all other channels equals to positive zero, FSX=FSR, All other channels GXO=$0V_{rms}$		-80	-73	dB
CT_{X-R}	Transmit to receive crosstalk (Intra-channel crosstalk)	PCM code for all channels equals to positive zero, FSX=FSR, Stimulating signal GXO=0dBm0, 300Hz-3.4KHz, all other channels GXO=$0V_{rms}$,		-80	-75	dB
$CTFE_R$	Far end crosstalk with digital stimulus (Inter-channel crosstalk)	PCM code for stimulated channel equals to 0dBm0, f=750Hz, PCM code for all other channels equals to positive zero, FSX=FSR, All other channels GXO=$0V_{rms}$		-80	-76	dB
$CTNE_X$	Near end crosstalk with analog stimulus (Inter-channel crosstalk)	PCM code for all channels equals to positive zero, FSX=FSR, Stimulating signal GXO=0dBm0, f=750Hz All other channels GXO=$0V_{rms}$		-80	-76	dB

Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Clock and Data Timing						
All timing parameters are measured at V_{OH}=2.0V and V_{OL}=0.7V						
$1/t_{PM}$	Frequency of MCLK			1.536 1.544 2.048 4.096 8.192		MHz MHz MHz MHz MHz
DC_{MCLK}	MCLK Duty Cycle		40		60	%
t_{RM}	Rise time of MCLK				10	ns
t_{FM}	Fall time of MCLK				10	ns
t_{SDB}	Setup time DR valid to MCLK low		20			ns
t_{HDB}	Hold time DR valid from MCLK low		20			ns
t_{DBD}	Delay from MCLK high to DX valid	C_L=100pF+2LSTTL loads	0		45	ns
t_{DZC}	Delay from MCLK high to DX disabled	C_L=100pF+2LSTTL loads			20	ns
t_{TSZC}	Delay from MCLK high to TSX disabled	C_L=100pF+2LSTTL loads			20	ns
t_{DBTS}	Delay time to $\overline{TS}_X$ low	C_L = 0pF to 150pF			50	ns
t_{PDN}	PDN persistence		$16xt_{PM}$			
t_{SF}	Set-up Time from FS to MCLK Low	Short Frame Sync Pulse	20			ns
t_{HF}	Hold Time from MCLK Low to FS Low	Short Frame Sync Pulse	20			ns

Long Frame Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HBFL}	Holding time from Clock to Frame Sync	Long Frame Only	10			ns
t_{SBF}	Set-up time from Frame Sync to Clock low	Long Frame Only	35			ns
t_{ZDF}	Delay time Valid Data from FS or MCLK, whichever comes later	C_L = 0pF to 150pF			50	ns

Note: when measuring signals going to TRI-STATE®, the timing delay is measured when the signal is 10% away from the starting level.

Applications Information

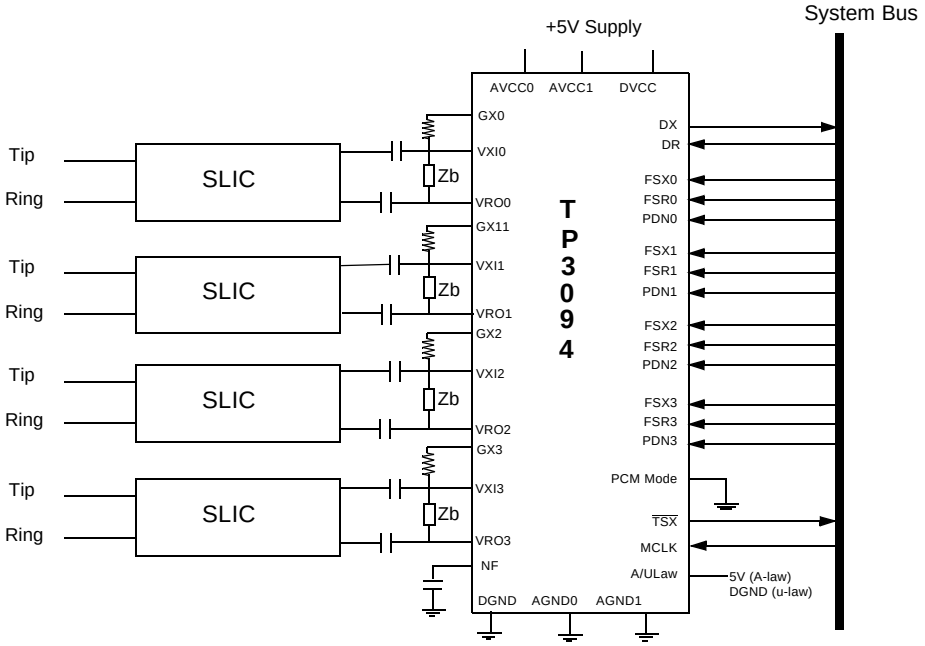


FIGURE 9. Typical application in a non cascaded mode

Applications Information

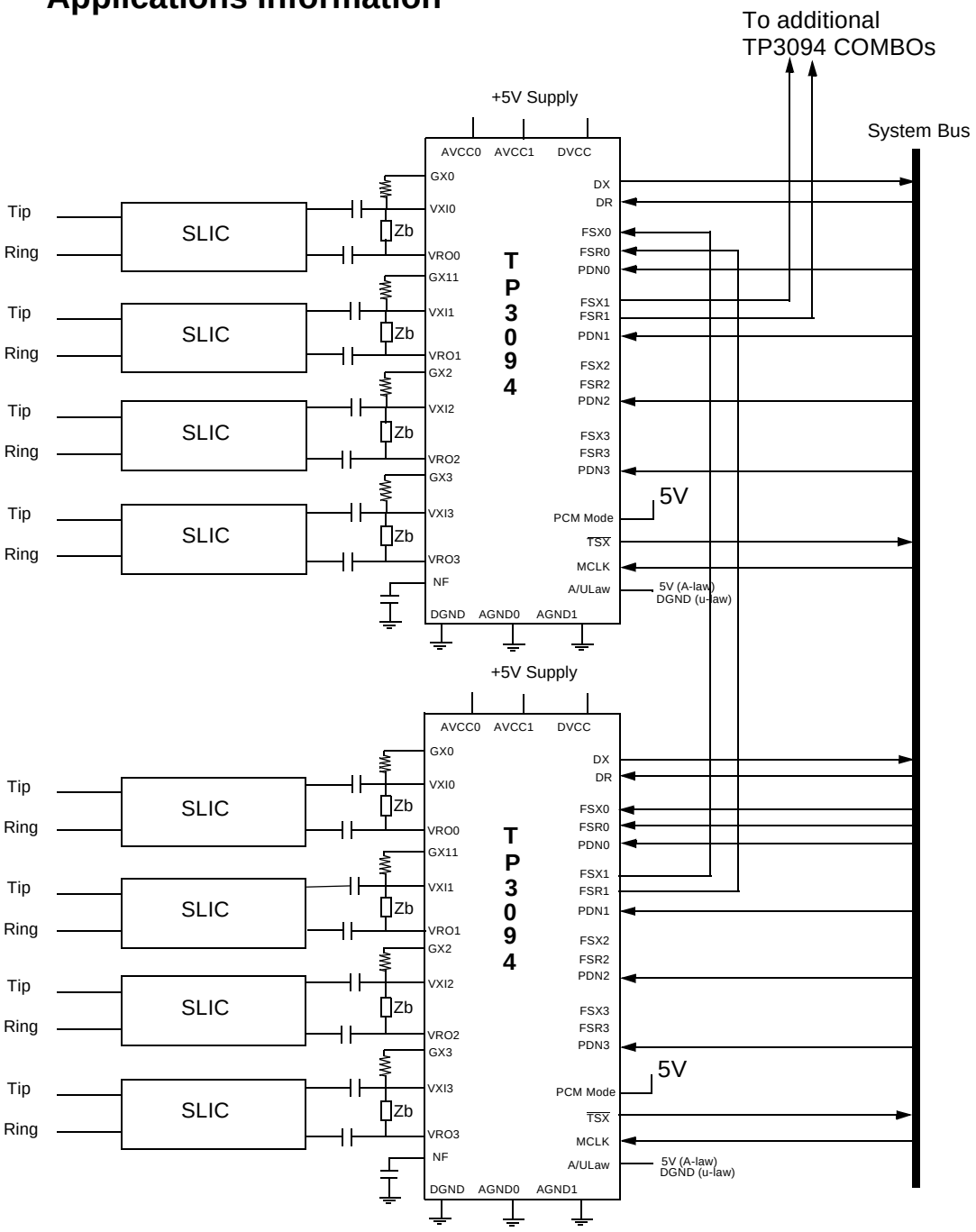
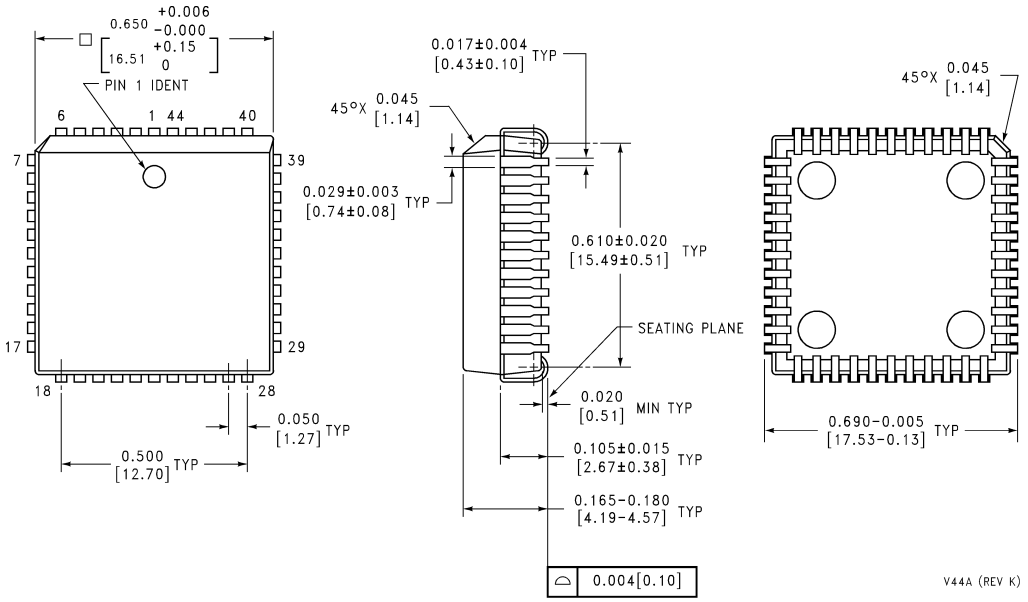


FIGURE 10. TP3094 in a cascade mode

Physical Dimensions inches (millimeters) unless otherwise noted



44-Lead Molded Plastic Chip Carrier (PLCC)

Order Number TP3094V

NS Package Number V44A

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