User's Guide
SPRUIC4C–July 2017–Revised January 2019

Piccolo F280049 controlCARD Information Guide

The Piccolo F280049 controlCARD from Texas Instruments (TI) is intended to provide a well-filtered robust design capable of working in most environments. This document describes the hardware details of the F280049 controlCARD and explains the functions, locations of jumpers, and connectors present on the board.

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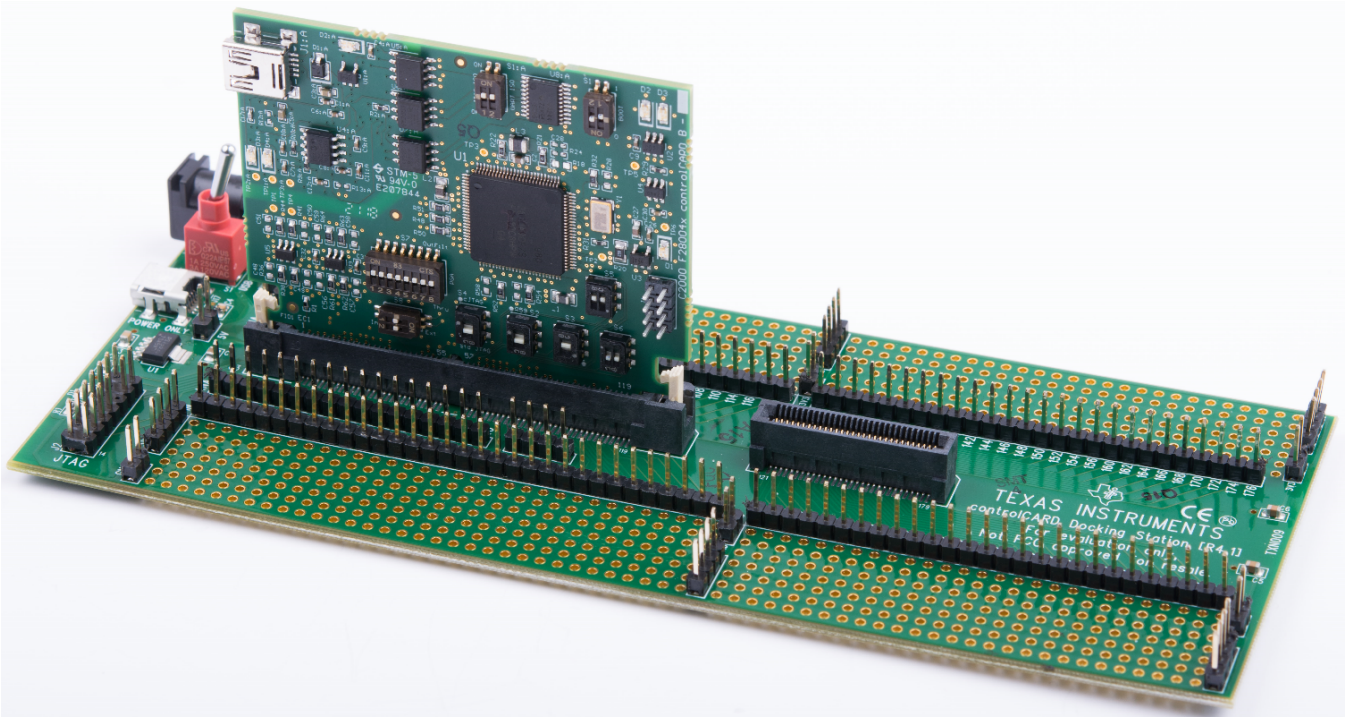


The Piccolo F280049 controlCARD from Texas Instruments (TI) provides a great way to learn and experiment with the F28004x device family within TI's C2000 family of microcontrollers (MCUs). This controlCARD uses the 120HSEC connector (compatible with the TMDSHSECDOCK docking station) and is intended to provide a well-filtered robust design capable of working in most environments. This document describes the hardware details of the F280049 controlCARD and explains the functions, locations of jumpers, and connectors present on the board.

The Hardware Developer's Kit, which is a full set of files necessary to evaluate and develop with the F280049 device, can be found in C2000Ware and includes:

- Schematics – designed in Altium
- Bill of materials (BOM)
- Layout PCB files – designed in Altium
- Gerber files

NOTE: This kit is designed to explore the functionality of the F28004x microcontroller family. The controlCARD can be treated as a good reference design, but it is not intended to be a complete customer design. Full compliance to safety, EMI/EMC, and other regulations are left to the designer of the final customer system.

This controlCARD can be obtained by ordering one of the products from Table 1.

Table 1. F280049 controlCARD Part Numbers

Part Number	Status	Description
TMDXDOCK280049M	Experimental	XF280049M controlCARD and HSEC docking station bundle
TMDSDOCK280049C	Qualified	F280049C controlCARD and HSEC docking station bundle
TMDSCNCD280049C	Qualified	F280049C controlCARD

2 Errata

Current revision of controlCARD as of June, 2018: PCB rev - B, ASSY rev - none.

2.1 Warnings, Notes, and Errata

Notes for all controlCARDs:

- The docking station is capable of drawing power through the included USB cable. However, when external components are added to the docking station for experimentation, the system may require more power than a standard USB port can provide (5-V and 500-mA). This is especially true when additional circuitry has been added to the docking station. In such cases, an external 5-VDC power supply (2.5-mm inner diameter × 5.5-mm outer diameter) plugged into J1 is recommended. A compatible supply could be the: Phihong PSAC05R-050(P)-R-C2 + Phihong RPBAG.
- The F28004x by default expects GPIO24 and GPIO32 to be the input pins responsible for determining the device boot mode at power up; the external pull directions for GPIO24 and GPIO32 are configured with S1 (see Table 4). If desired, the GPIO pins used for boot mode selection can be modified by programming the OTP in the device. Refer to the Boot ROM section of the specific device's Technical Reference Manual (TRM) for more information.
- The controlCARD included with TMDXDOCK280049M uses prototype silicon XF280049M. XF280049M is a prototype variant only, and is not offered in production. It has the same functionality and configuration as the qualified variant F280049C.

3 Getting Familiar With the controlCARD

3.1 F280049 controlCARD Features

- **Piccolo F280049 Microcontroller** – High performance C2000 microcontroller on the controlCARD.
- **120pin HSEC8 Edge Card Interface** – Allows for compatibility with all of C2000's 120- or 180-pin controlCARD-based application kits and TMDSHSECDOCK. Compatibility with 100-pin DIMM controlCARDs can be accomplished using the TMDSADAP180TO100 adapter card (sold separately).
- **Built-in Isolated JTAG Emulation** – An XDS100v2 emulator provides a convenient interface to Code Composer Studio without additional hardware. Flipping a switch allows an external JTAG emulator to be used. This external emulator may use standard 4-pin JTAG or 2-pin cJTAG.
- **Key Signal Breakout** – Most GPIO, ADC, and other key signals routed to hard gold connector fingers.
- **Robust Power Supply Filtering** – Single 5-VDC supply provides power to onboard 3.3-V LDO. All MCU inputs are then decoupled using LC filters near the device.
- **ADC Clamping** – ADC inputs are clamped by protection diodes.
- **Anti-Aliasing Filters** – Noise filters (small RC filters) can be easily added on several ADC input pins.

3.2 F28004x Device Description

For a complete description of the F28004x devices, see Section 1.3 of the *TMS320F28004x Piccolo™ Microcontrollers* data sheet (SPRS945).

3.3 Assumed Operating Conditions

This kit is assumed to run at standard room conditions. The EVM should run at approximately Standard Ambient Temperature and Pressure (SATP) with moderate-to-low humidity.

3.4 Using the controlCARD

For the controlCARD to work, the controlCARD MCU must be powered. This is usually done by inputting 5-VDC through the HSEC connector through an accompanying baseboard. For example, if using a docking station baseboard, 5-VDC should be input into the docking station's J1 or J17, then SW1 must be toggled to the appropriate position.

Based on the way that the controlCARD is used, additional hardware settings may be necessary, as shown in Table 2.

Table 2. Getting Started Reference

Component	Debug Using CCS and the on-card XDS100v2 Emulator	Debug Using CCS and an External Emulator Through the Baseboard	Standalone (Boot From FLASH or Other Boot Mode)
S1:A (controlCARD)	Left (Switch 1): Up (ON)	Left (Switch 1): Down (OFF)	Left (Switch 1): Down (OFF)
J1:A (controlCARD)	Connect a mini USB cable between J1:A and the computer. In CCS, use this target configuration: F280049 device with an XDS100v2 emulator.	—	—
S1 (controlCARD)	Left (Switch 2): Down (ON) Right (Switch 1): Up (OFF) Putting the C2000 device into Wait Mode can reduce the risk of connectivity issues.	Left (Switch 2): Down (ON) Right (Switch 1): Up (OFF) Putting the C2000 device into Wait Mode can reduce the risk of connectivity issues.	Set S1 as desired (See Table 4 for supported settings)
Baseboard's JTAG connector (J2 on the Docking Station baseboard)	—	Connect an external emulator and appropriately configure the CCS target configuration.	—

The F280049 controlCARD to docking station signal mapping can be found in the C2000Ware controlCARD product directory at \ti\c2000\C2000Ware_XXXX\boards\controlCARDs:

- **TMDSCNCD28004x_RevA_120cCARD_pinout.pdf** -- F280049 signal mapping on the default HSEC docking station
- **TMDSCNCD28004x_RevA_100DIM_map.pdf** -- F280049 signal mapping on the legacy DIM100 docking station if using TMDSADAP180TO100 adapter card

Hardware support files for the F280049 controlCARD and docking station can also be found in the C2000Ware product directories:

- F280049 controlCARD: \ti\c2000\C2000Ware_XXXX\boards\controlCARDs
- Docking station: \ti\c2000\C2000Ware_XXXX\boards\ExperimenterKits

3.5 Software Development

Code Composer Studio (CCS) is the recommended integrated development environment (IDE) for developing and debugging software for the C2000 series of MCUs. CCS is free to download and use with the controlCARD. Introductory videos for CCS are available at training.ti.com.

NOTE: For users of TMDXDOCK280049M

TMS320F280049M is a discontinued part number that is not supported on new installations of CCS. Use the functionally equivalent TMS320F280049C part number when creating a new target configuration for TMDXDOCK280049M on new installations of CCS.

C2000Ware contains a full suite of example software designed to work with the F280049 controlCARD. This software package includes many example projects which allow the user to experiment with the ADC, PWM, and other C2000 peripherals.

Support files for both register-level and driver-level programming are included with C2000Ware:

- Register programming examples are located at:
  \ti\c2000\C2000Ware_XXXX\device_support\f28004x\examples
- Driverlib programming examples are located at:
  \ti\c2000\C2000Ware_XXXX\driverlib\f28004x\examples

4 Special Notes

4.1 XDS100v2 Emulator and SCI/UART Connectivity

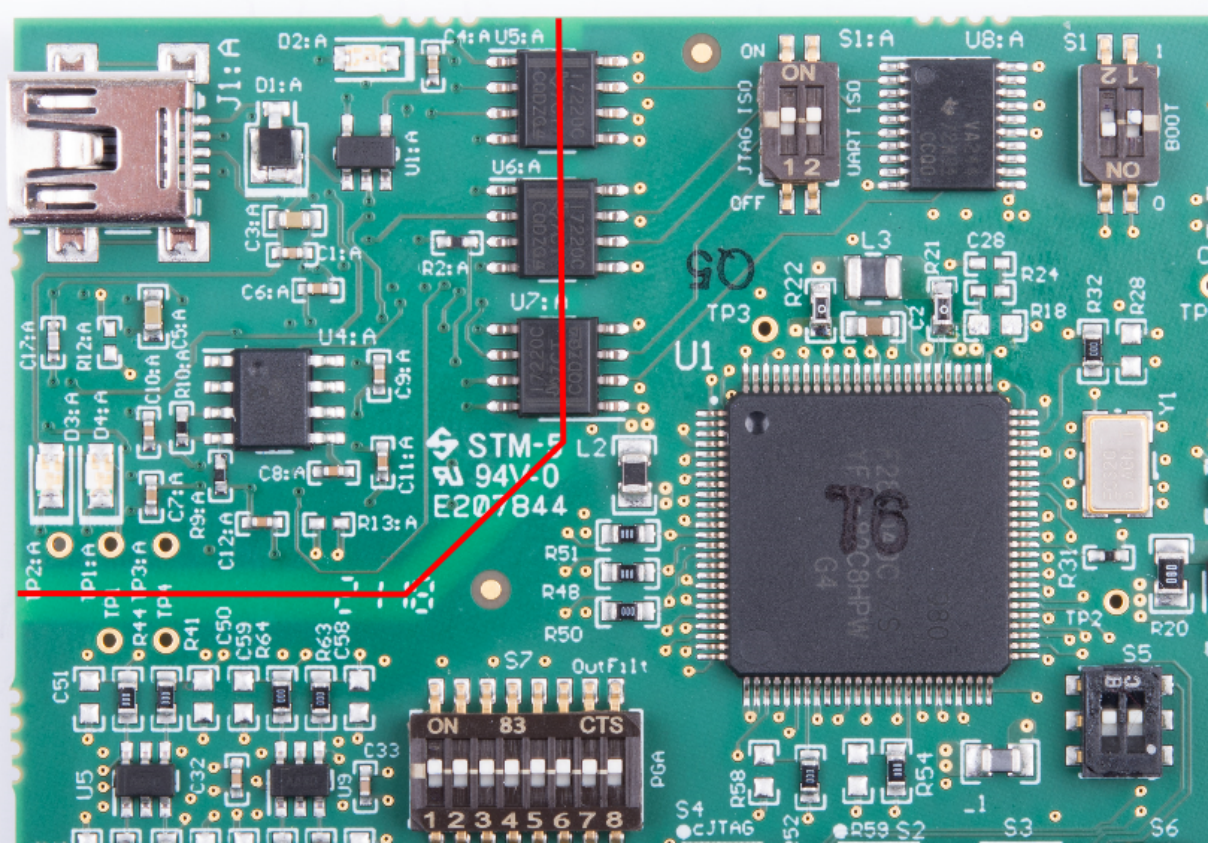
The F280049 controlCARD provides on-board emulation and USB-to-UART adapter functionality. This allows for a convenient method to debug and demo the F280049 MCU.

The FTDI chip, its support circuitry, and associated isolation components are placed in Macro A, the left section of the controlCARD. Each of these components contains an additional A within the component reference designator (that is R2:A for resistor 2 in Macro A).

Each F280049 controlCARD's XDS100v2 is programmed with a fixed serial number. If a debug session must involve two or more F280049 controlCARDs, each controlCARDs must have a unique serial number, and some must be reprogrammed. See: http://processors.wiki.ti.com/index.php/XDS100#Q:_Can_I_change_the_serial_number_on_my_XDS100v2.3F.

The configuration of the switches on S1:A (shown in Figure 2) determine whether the onboard emulator is active, whether an external emulator can be used, or whether the device will boot from FLASH/peripherals.

Figure 2. XDS100v2 Emulation Circuitry and Isolation Circuitry is Denoted by :A



4.2 cJTAG Usage

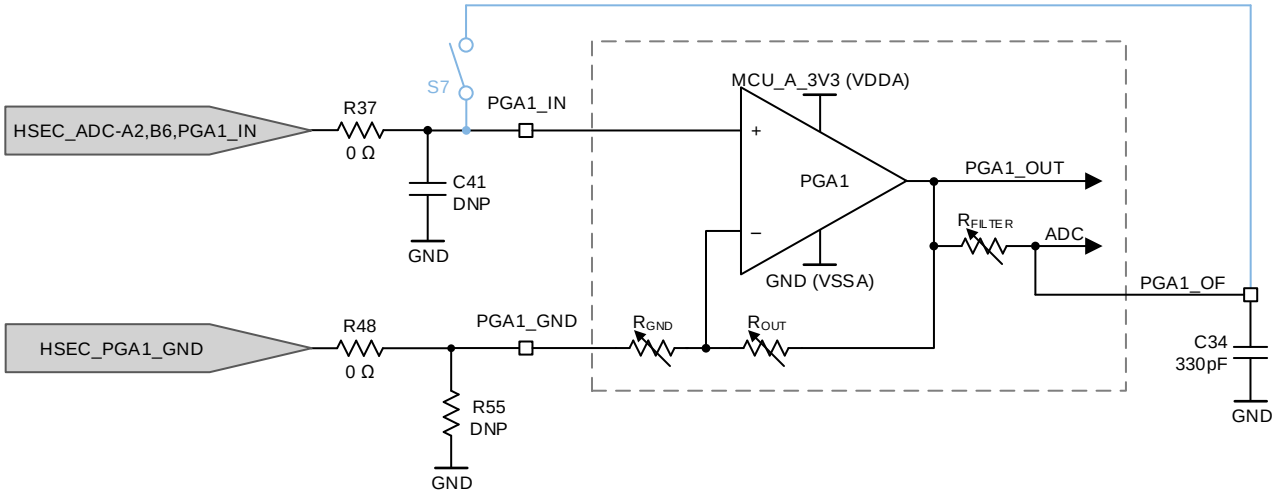
The F280049 MCU supports the cJTAG 2-pin debugging interface, but the onboard XDS100v2 emulator does not. To experiment with cJTAG, an external emulator must be connected through the baseboard. To enable cJTAG:

1. Connect an external emulator to the controlCARD's baseboard.
2. Change S4 to the cJTAG position (switch flipped up).
3. If cJTAG is used, the F280049 MCU will have two additional GPIOs which can be used by the application. Configure S2 and S3, as desired, to control which controlCARD fingers or pins the newly available GPIOs are connected to.

4.3 Evaluation of the Programmable Gain Amplifier (PGA)

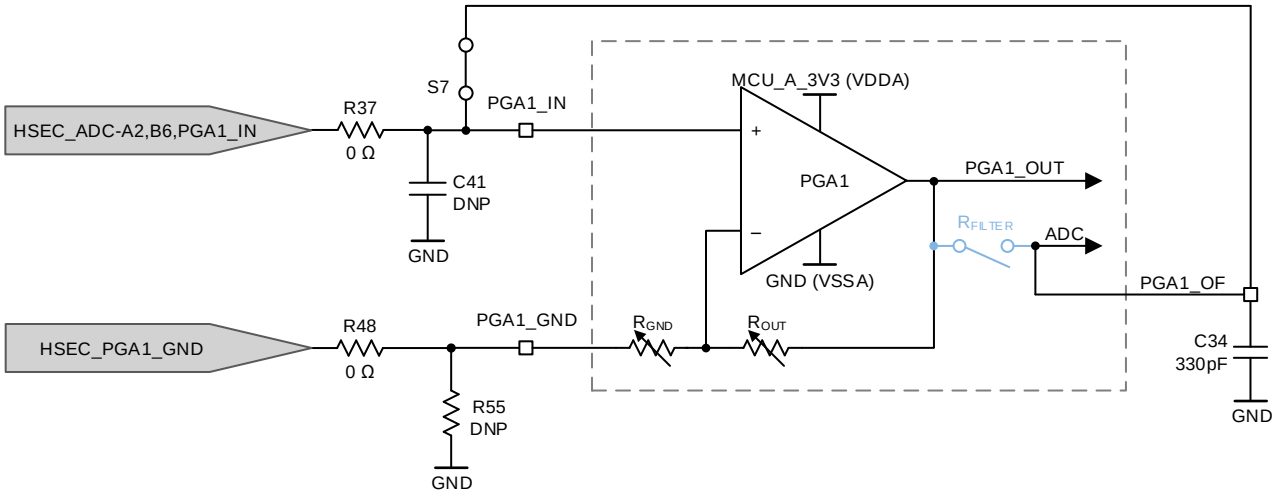
When evaluating the PGA, the PGA_GND pin must be driven to the ground reference of the PGA_IN signal. The PGA_GND signal may be provided using differential signaling through the HSEC fingers for improved noise immunity, or the PGA_GND pin may be tied to the GND reference of the controlCARD through a 0-Ω resistor (R55 in Figure 3) for simplicity.

Figure 3. PGA With S7 Open (Output Filter Usable)



The S7 switch bank provides the flexibility to either use the PGA output filter pin (PGAn_OF) for filtering (S7 open in Figure 3) or for sampling the PGA input voltage directly by bypassing the internal PGA (S7 closed in Figure 4).

Figure 4. PGA With S7 Closed (Output Filter Not Usable)



NOTE: The S7 closed implementation for PGA6 is different from the other PGAs. Instead of shorting PGA6_OF and PGA6_IN, the PGA6_OF signal may be accessed from the HSEC connector independently of the PGA6_IN signal.

NOTE: The PGA R_{FILTER} resistor should never be enabled while the S7 switch is closed. Prolonged exposure to contention between the PGA_IN and PGA_OF pins may result in permanent damage to the internal R_{FILTER} resistor.

4.4 Evaluation of the Analog to Digital Converters(ADCs)

When using the F280049 on-chip ADCs there are some useful guideline to follow to realize the performance numbers listed in the datasheet. This is especially true for the AC parameters such as: SNR, THD, and SINAD. Furthermore, it can also be shown that there is a direct correlation between the SNR of the ADC result and the spread of ADC codes seen for a DC input; as such these tips will improve the range and standard deviation of a DC input as well. Finally, while topics addressed will be with respect to the controlCARD, they are applicable to other implementations using the F280049 MCU as well.

On-board resistors and capacitors: By default (Figure 5) all inline resistors to the ADC pins are a simple 0-Ω shunt and all capacitors to the ground plane are not populated. While this circuit can be used to supply the ADC inputs with a voltage, likely both the resistor(R) and capacitor(C) will need to be populated based on the voltage source's characteristics. Referring to the ADC Input Model, the ADC input has its own RC network made up of the internal sample and hold capacitor, switch resistance, and parasitic capacitance. By changing the inline resistance and parallel capacitor we can optimize the input circuit to assist with settling time and/or filtering the input signal. Finally, it is recommended in general to use either NPO(Negative-Positive 0 PPM/°C) or COG(Ceramic On Glass) as these have better stability over temperature and across input frequencies than other types of capacitors.

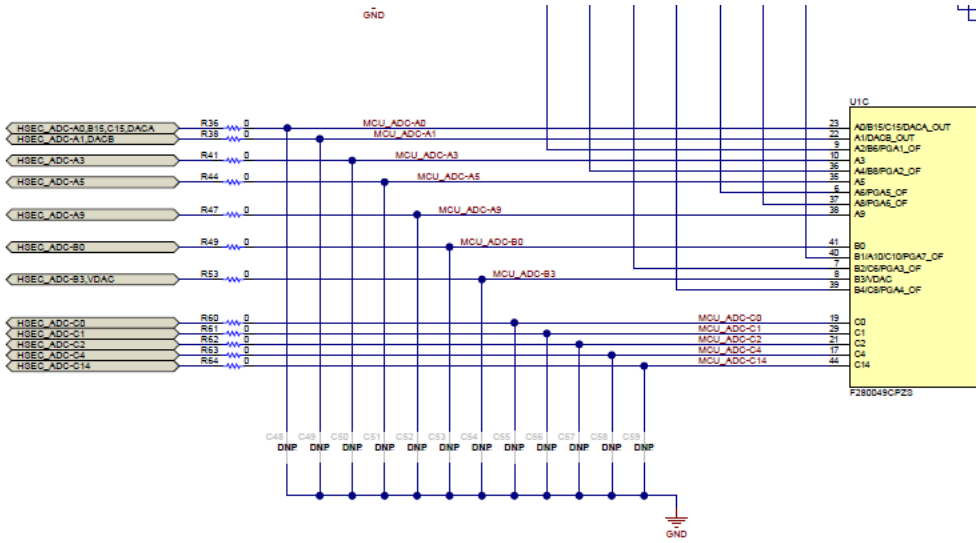


Figure 5. Partial Schematic Showing Default R and C values

Voltage source and drive circuitry: While the on-chip ADCs are 12-bit architecture (4096 distinct output codes when converting an analog signal to the digital domain); the translation will only be as precise as the input provided to the ADC. The typical rule of thumb when defining the source resolution to realize the full specification of an ADC is to have a 1-bit better source than the converter. In this case that would mean that ideally the analog input should be accurate to 13-bits.

Typically voltage supplies or regulators are not designed to be precise, but rather accommodate a wide range of current loads within a certain tolerance and for this reason are not ideal to show the performance of a higher bit ADC, like the one on the F280049. This does also not take into account that many times the supply in question is providing the main voltage to power the MCU itself; which also introduces noise and other artifacts into the signal.

In addition to the quality of the input signal there is also the aspect of the load presented to the ADC when it samples the input. Ideally an input to an ADC would have zero impedance so as not to impact the internal R/C network when the sampling event takes place. In many applications, however, the voltages that are sampled by the ADC are derived from a series of resistor networks, often large in value to decrease the active current consumption of the system. A solution to isolate the source impedance from the ADC sampling network is to place an operational amplifier in the signal path. Not only does this isolate the impedance of the signal from the ADC, it also shields the source itself from any effects the sampling network may have on the system.

Recommended source for evaluation: The Precision Signal Injector (PSI) EVM from TI was used to validate the ADC performance on the F280049C ControlCARD. This EVM supports both single ended as well as differential ended outputs using a 16-bit DAC as the signal source then passed through a high precision op-amp with post amplifier filtering. The EVM is powered and controlled through a standard USB connection from a host PC and includes a GUI to control its output. The outputs are routed through single or dual SMA type connectors; it is highly recommended to place an additional female SMA connector (Figure 6) on the controlCARD docking station to receive the signal via SMA for best noise immunity. For the local RC network 30-Ω resistors and 300pF capacitors were used. Using this setup the ADC parameters were observed to be consistent with the numbers in the datasheet.

Figure 6. Female SMA Connector

4.5 Evaluation of the Internal DC/DC Converter

The controlCARD, by default, assumes the F280049 internal VREG will be used to generate the 1.2-V power supply required by the MCU. The controlCARD enables the user to use the internal DC/DC converter capabilities, with some soldering.

To enable the internal DC/DC converter:

- R18 and R19 must be unpopulated.
- R21 and R22 must be populated with a 0-Ω resistor.
- C19 must be populated with a 2.2-µF X5R/X7R capacitor.
- C20 and C21 must each be populated with a 10-µF X5R/X7R capacitor.

Functionally, the F280049 powers up the 1.2-V power rail using the internal VREG, then requires software to change from the VREG to the DC/DC. See the F28004x Technical Reference Manual for more details.

5 Hardware References

Table 3 shows the various connections available on the board. Figure 7 illustrates the location of many of these components on the board.

Figure 7. Key Components on the controlCARD

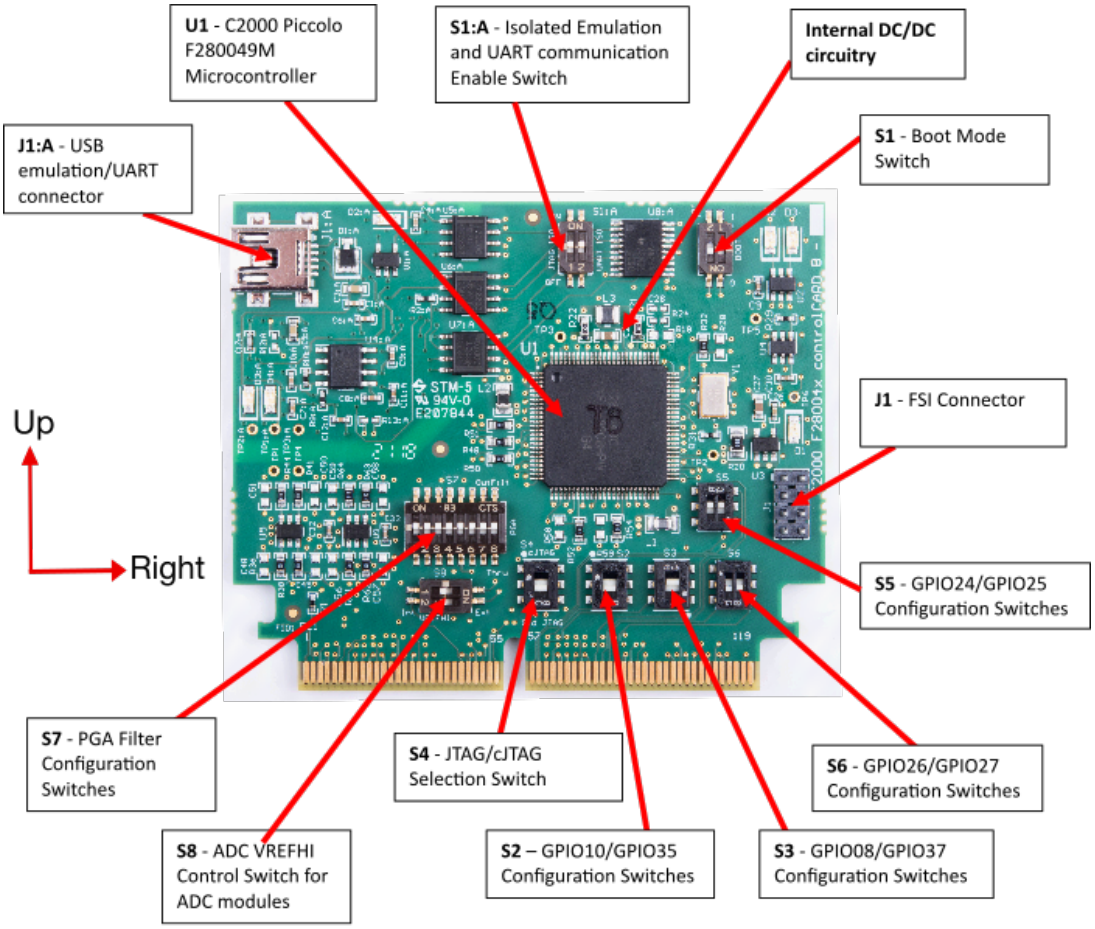


Table 3. Hardware References

Connectors	
J1:A	Emulation/UART connector - USB mini A connector used to provide XDS100v2 emulation and USB-to-UART(SCI) communication through FTDI logic. S1:A determines which connections are enabled to the MCU.
Jumpers	
J1	FSI Connector - Gives an ability to connect FSI signals from the F280049 to another board.
LEDs	
D1	Turns on when the controlCARD is powered ON (green)
D2	Controlled by GPIO-31 with negative logic (red)
D3	Controlled by GPIO-34 with negative logic (red)
D2:A	Turns on when ISO JTAG logic is powered on (green)
D3:A	JTAG/UART RX toggle indicator (blue)
D4:A	JTAG/UART TX toggle indicator (blue)
Resistors and Capacitors (default setting in BOLD)	
R18, R19, R21, R22	GPIO22/23 configuration resistors These resistors allow the user to choose whether GPIO22/23 is used as GPIO (and go to the baseboard) or whether they will be used in conjunction with the F280049 MCU's internal DC/DC capability: • **R18,R19 populated with 0-Ω resistors and R21,R22 unpopulated** – GPIO22 and GPIO23 are used as GPIO and go to the baseboard through EC1. The internal DC/DC cannot be used. • R18,R19 unpopulated and R21,R22 populated with 0-Ω resistors – Internal DC/DC can be used to generate the 1.2-V VDD power rail. GPIO22 and GPIO23 are used as VFBSW and VSW, respectively. The internal DC/DC can be used.
C19, C20, C21	These capacitors should be populated when the F280049's internal DC/DC capability is used. C19 should be populated with a 2.2-µF capacitor. C20 and C21 should each be populated with a 10-µF capacitor.
R24, C28	R24 and C28 create an optional snubber circuit, which can be used if the DC/DC is used.
R36-R47,R49,R53, R60-R64, C41-C47, and C48-C59	Optional RC input filter for all ADC/PGA inputs
C34-C40	PGA filter capacitor when PGA filtering is used
R55-R59	PGA-GND configuration resistors
R48,R50-R52,R54	These resistors control whether the negative input (PGAGND) for each PGA are grounded locally or whether they should be grounded through pins on the HSEC connector (for use in Kelvin grounding). By default, **resistors R55-R59 are not populated and R48, R50-R52, R54 are populated**. Because of this, all the PGAs are, by default, expected to be referenced to ground by the baseboard. If, for example, R55 was populated and R48 was unpopulated, then PGA1's PGAGND would be grounded on the controlCARD.
Switches (default position in BOLD)	
S1 (Installed with 180 degree rotation)	Boot Mode Selection Switch See Table 4 for a list of selectable boot modes. See the device datasheet and TRM for more information about device boot behavior. Left (Switch 2) – GPIO24 Configuration Switch: • **In the up position** – GPIO24 is pulled high • In the down position – GPIO24 is pulled low Right (Switch 1) – GPIO32 Configuration Switch: • **In the up position** – GPIO32 is pulled high • In the down position – GPIO32 is pulled low
S2	GPIO10/GPIO35 Configuration Switches • In the up position – GPIO10 goes to pin 60 of the HSEC connector. If S4's switch 1 is in the up position, GPIO35 goes to pin 85 of the HSEC connector. • **In the down position** – GPIO10 goes to pin 85 of the HSEC connector. If S4's switch 1 is in the up position, GPIO35 goes to pin 60 of the HSEC connector.

Table 3. Hardware References (continued)

S3 (Installed with 180 degree rotation)	GPIO08/GPIO37 Configuration Switches • **In the up position** – GPIO08 goes to pin 87 of the HSEC connector. If S4's switch 2 is in the up position, GPIO37 goes to pin 58 of the HSEC connector. • In the down position – GPIO08 goes to pin 58 of the HSEC connector. If S4's switch 2 is in the up position, GPIO37 goes to pin 87 of the HSEC connector.
S4	JTAG/cJTAG Selection Switch • In the up position – 2-pin cJTAG mode is expected to be used. GPIO35 and GPIO37 go to the baseboard based on the settings of S2 and S3, respectively. • **In the down position** – 4-pin standard JTAG is expected to be used. GPIO35 and GPIO37 are used to support JTAG functionality. The on-card XDS100v2 emulator requires 4-pin JTAG to be used.
S5 (Installed with 180 degree rotation)	GPIO24/GPIO25 Configuration Switches Left (Switch 2) – GPIO25 Configuration Switch: • **In the up position** – GPIO25 goes to pin 77 of the HSEC connector. • In the down position – GPIO25 goes to pin 102 of the HSEC connector. Right (Switch 1) – GPIO24 Configuration Switch: • **In the up position** – GPIO24 goes to pin 75 of the HSEC connector. • In the down position – GPIO24 goes to pin 100 of the HSEC connector.
S6	GPIO26/GPIO27 Configuration Switches Left (Switch 1) – GPIO26 Configuration Switch: • In the up position – GPIO26 goes to pin 107 of the HSEC connector. • **In the down position** – GPIO26 goes to pin 79 of the HSEC connector. Right (Switch 2) – GPIO27 Configuration Switch: • In the up position – GPIO27 goes to pin 109 of the HSEC connector. • **In the down position** – GPIO27 goes to pin 81 of the HSEC connector.
S7	PGA Filter Configuration Switches From the left, the switches control whether PGA1-PGA7's outputs, respectively, are filtered. The eighth switch of S7 is not used. Each switch: • **In the up position** – an HSEC pin is connected to the respective PGA+ input pin, and is now also tied to an additional ADC input pin. In software, PGA output filtering, for the respective PGA, functionality should NOT be used. • In the down position – an HSEC pin only goes to the PGA+ input pin. PGA output filtering, for the respective PGA, may be used. The up position for S7's switch 6 (PGA6) is implemented differently from the other PGAs. PGA6_OF may be accessed through the HSEC connector independently of PGA6_IN, whereas the other PGAs will have their respective PGAn_OF and PGAn_IN signals shorted together.
S8 (Installed with 90 degree rotation)	ADC VREFHI Control Switch for ADC modules Top (Switch 1) – VREFHI Control Switch for ADC module A: • **In the left position** – ADC-A should be configured to use the internal voltage reference. • In the right position – ADC-A is configured to use an external voltage reference, which should be connected to pin 45 of the HSEC connector. Bottom (Switch 2) – VREFHI Control Switch for ADC module B and module C: • **In the left position** – ADC-B and ADC-C should be configured to use the internal voltage reference. • In the right position – ADC-B and ADC-C are configured to use an external voltage reference, which should be connected to pin 45 of the HSEC connector.
S1:A	Isolated emulation and UART communication enable switches Left (Switch 1) – JTAG Enable: • **Up (on)** – All signals between the XDS100v2 emulation logic and the MCU are connected. This setting is valid when the MCU is being debugged or programmed through the on-card XDS100v2 emulator. • Down (off) – The XDS100v2 emulation logic will NOT be connected to the MCU. This setting is valid when the device boots from FLASH, boots from a peripheral directly, or when an external JTAG emulator is used. Right (Switch 2) – ISO UART communication enable: • **Up (on)** – The C2000 MCU's GPIO-28 (and pin76 of the 180pin controlCARD connector) are coupled to the FTDI's USB-to-Serial adapter. This allows UART communication to a computer through the FTDI chip. However, in this position, GPIO-28 is forced high by the FTDI chip. Functionality of pin76 on the connector is limited. • Down (off) – The C2000 MCU will NOT be connected to the FTDI USB-to-Serial adapter. Pin76 of the 180pin controlCARD connector is directly connected to GPIO-28.

Table 4. Boot Mode Switch (S1) Positions

Mode #	GPIO-24 (Left, Switch 2)	GPIO-32 (Right, Switch 1)	Boot from
00	0 (Down)	0 (Down)	Parallel I/O
01	0 (Down)	1 (Up)	Boot from SCI / Wait Mode
02	1 (Up)	0 (Down)	Boot from CAN
03	1 (Up)	1 (Up)	Boot from FLASH

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (July 2018) to C Revision **Page**

- Replaced Figure 1 showing control card with all protective stickers removed. 2
- Updated Figure 2 to highlight isolation boundary on the EVM. 6
- Added Evaluation of the Analog to Digital Converters(ADCs) section to show best practices to realize the datasheet performance numbers of the ADC. 8
- Updated Figure 7 to remove the protective film..... 10
- Fixed D1, D2, D3 description. 11

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