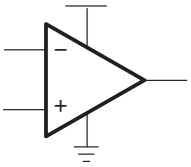
- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **Rail-To-Rail Input/Output**
- **Wide Bandwidth . . . 3 MHz**
- **High Slew Rate . . . 2.4 V/μs**
- **Supply Voltage Range . . . 2.7 V to 16 V**
- **Supply Current . . . 550 μA/Channel**
- **Input Noise Voltage . . . 39 nV/√Hz**

† Contact Texas Instruments for details. Q100 qualification data available on request.

- **Input Bias Current . . . 1 pA**
- **Specified Temperature Range −40°C to 125°C . . . Automotive Grade**
- **Ultrasmall Packaging**
  - **5 Pin SOT-23 (TLV2371)**
  - **8 Pin MSOP (TLV2372)**

Operational Amplifier



description

The TLV237x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV237x takes the minimum operating supply voltage down to 2.7 V over the extended automotive temperature range while adding the rail-to-rail output swing feature. The TLV237x also provides 3-MHz bandwidth from only 550 μA. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from (±8 V supplies down to ±1.35 V) a variety of rechargeable cells.

The CMOS inputs enable use in high-impedance sensor interfaces, with the lower voltage operation making an ideal alternative for the TLC227x in battery-powered applications. The rail-to-rail input stage further increases its versatility. The TLV237x is the seventh member of a rapidly growing number of RRIO products available from Texas Instruments and it is the first to allow operation up to 16-V rails with good ac performance.

The 2.7-V operation makes the TLV237x compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power microcontrollers available today including Texas Instruments' MSP430.

SELECTION OF SIGNAL AMPLIFIER PRODUCTS†

DEVICE	V_{DD} (V)	V_{IO} (μV)	Iq/Ch (μA)	I_{IB} (pA)	GBW (MHz)	SR (V/μs)	SHUTDOWN	RAIL-TO-RAIL	SINGLES/DUALS/QUADS
TLV237x	2.7−16	500	550	1	3	2.4	Yes	I/O	S/D/Q
TLC227x	4−16	300	1100	1	2.2	3.6	—	O	D/Q
TLV27x	2.7−16	500	550	1	3	2.4	—	O	S/D/Q
TLC27x	3−16	1100	675	1	1.7	3.6	—	—	S/D/Q
TLV246x	2.7−6	150	550	1300	6.4	1.6	Yes	I/O	S/D/Q
TLV247x	2.7−6	250	600	2	2.8	1.5	Yes	I/O	S/D/Q
TLV244x	2.7−10	300	725	1	1.8	1.4	—	O	D/Q

† Typical values measured at 5 V, 25°C

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES				UNIVERSAL EVM BOARD
		SOIC	SOT-23	TSSOP	MSOP	
TLV2371	1	8	5	—	—	See the EVM Selection Guide (SLOU060)
TLV2372	2	8	—	—	8	
TLV2374	4	14	—	14	—	

TLV2371 AVAILABLE OPTIONS

T_A	V_{IO}MAX AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	SOT-23	
			(DBV)	SYMBOL
−40°C to 125°C	4.5 mV	TLV2371QDRQ1	TLV2371QDBVRQ1†	

† Product Preview

TLV2372 AVAILABLE OPTIONS

T_A	V_{IO}MAX AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	MSOP	
			(DGK)	SYMBOL
−40°C to 125°C	4.5 mV	TLV2372QDRQ1	TLV2372QDGKRQ1†	

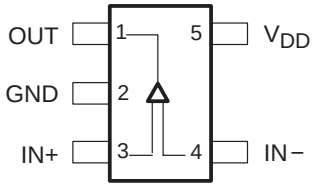
† Product Preview

TLV2374 AVAILABLE OPTIONS

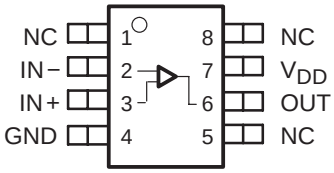
T_A	V_{IO}MAX AT 25°C	PACKAGED DEVICES	
		SMALL OUTLINE (D)	TSSOP (PW)
−40°C to 125°C	4.5 mV	TLV2374QDRQ1	TLV2374QPWRQ1

TLV237x PACKAGE PINOUTS(1)

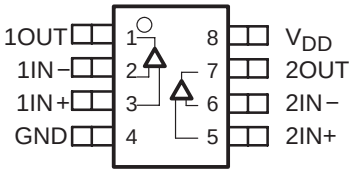
TLV2371
DBV PACKAGE
(TOP VIEW)



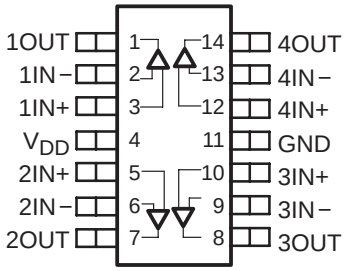
TLV2371
D PACKAGE
(TOP VIEW)



TLV2372
D OR DGK PACKAGE
(TOP VIEW)

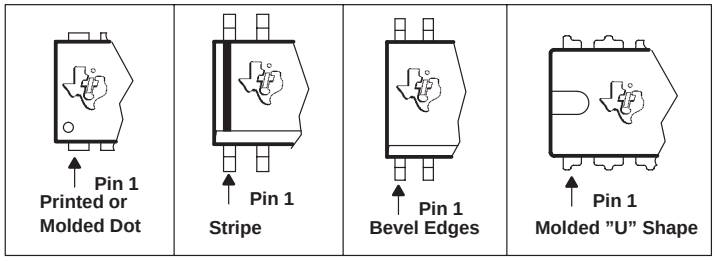


TLV2374
D OR PW PACKAGE
(TOP VIEW)



NC − No internal connection
(1) SOT−23 may or may not be indicated

TYPICAL PIN 1 INDICATORS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 16.5 V
Differential input voltage, V_{ID} . . . . . $\pm V_{DD}$
Input voltage range, V_I (see Note 1) . . . . . −0.2 V to V_{DD} + 0.2 V
Input current range, I_I . . . . . ±10 mA
Output current range, I_O . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D (8-pin) package . . . . . 176°C/W
D (14-pin) package . . . . . 122.3°C/W
D (16-pin) package . . . . . 114.7°C/W
DBV (5-pin) package . . . . . 324.1°C/W
DGK (8-pin) package . . . . . 259.96°C/W
PW (14-pin) package . . . . . 173.6°C/W
Operating free-air temperature range, T_A: Q suffix . . . . . −40°C to 125°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	16	V
	Split supply	±1.35	±8	
Common-mode input voltage range, V_{ICR}		0	V_{DD}	V
Turnon voltage level, $V_{(ON)}$, relative to GND pin voltage			2	V
Turnoff voltage level, $V_{(OFF)}$, relative to GND pin voltage		0.8		V
Operating free-air temperature, T_A	Q-suffix	−40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$		25°C		2	4.5	mV
				Full range			6	
α_{VIO}	Offset voltage drift			25°C		2		μV/°C
CMRR	Common-mode rejection ratio	V_{IC} = 0 to V_{DD}, $R_S = 50\ \Omega$	V_{DD} = 2.7 V	25°C	50	68		dB
				Full range	49			
		V_{IC} = 0 to V_{DD}–1.35 V, $R_S = 50\ \Omega$		25°C	53	70		
				Full range	54			
		V_{IC} = 0 to V_{DD}, $R_S = 50\ \Omega$,	V_{DD} = 5 V	25°C	55	72		
				Full range	54			
		V_{IC} = 0 to V_{DD}–1.35 V, $R_S = 50\ \Omega$,		25°C	58	80		
				Full range	57			
		V_{IC} = 0 to V_{DD}, $R_S = 50\ \Omega$,	V_{DD} = 15 V	25°C	64	82		
				Full range	63			
		V_{IC} = 0 to V_{DD}–1.35 V, $R_S = 50\ \Omega$,		25°C	67	84		
				Full range	66			
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)} = V_{DD}/2$, $R_L = 10\ k\Omega$	V_{DD} = 2.7 V	25°C	95	106		dB
				Full range	76			
			V_{DD} = 5 V	25°C	80	110		
				Full range	82			
			V_{DD} = 15 V	25°C	77	83		
				Full range	79			

input characteristics

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{IO}	Input offset current	V_{DD} = 15 V, $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$	25°C		1	60	pA
			125°C			500	
I_{IB}	Input bias current		25°C		1	60	pA
			125°C			500	
$r_{i(d)}$	Differential input resistance		25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 21 kHz	25°C		8		pF

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{IC} = V_{DD}/2$, $I_{OH} = -1$ mA, $V_{ID} = 1$ V	V_{DD} = 2.7 V	25°C	2.55	2.58		V
				Full range	2.48			
			V_{DD} = 5 V	25°C	4.9	4.93		
				Full range	4.85			
			V_{DD} = 15 V	25°C	14.92	14.96		
				Full range	14.9			
		$V_{IC} = V_{DD}/2$, $I_{OH} = -5$ mA, $V_{ID} = 1$ V	V_{DD} = 2.7 V	25°C	1.88	2		
				Full range	1.42			
			V_{DD} = 5 V	25°C	4.58	4.68		
				Full range	4.44			
			V_{DD} = 15 V	25°C	14.7	14.8		
				Full range	14.6			
V_{OL}	Low-level output voltage	$V_{IC} = V_{DD}/2$, I_{OL} = 1 mA, $V_{ID} = 1$ V	V_{DD} = 2.7 V	25°C		0.1	0.15	V
				Full range			0.22	
			V_{DD} = 5 V	25°C		0.05	0.1	
				Full range			0.15	
			V_{DD} = 15 V	25°C		0.05	0.08	
				Full range			0.1	
		$V_{IC} = V_{DD}/2$, I_{OL} = 5 mA, $V_{ID} = 1$ V	V_{DD} = 2.7 V	25°C		0.52	0.7	
				Full range			1.15	
			V_{DD} = 5 V	25°C		0.28	0.4	
				Full range			0.54	
			V_{DD} = 15 V	25°C		0.19	0.3	
				Full range			0.35	

power supply

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
I_{DD}	Supply current (per channel)	$V_O = V_{DD}/2$,	V_{DD} = 2.7 V	25°C		470	560	μA
			V_{DD} = 5 V	25°C		550	660	
			V_{DD} = 15 V	25°C		750	900	
				Full range			1200	
PSRR	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 15 V, No load	$V_{IC} = V_{DD}/2$,	25°C	70	80		dB
				Full range	65			

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	R_L = 2 kΩ, C_L = 10 pF	V_{DD} = 2.7 V	25°C		2.4		MHz
			V_{DD} = 5 V to 15 V	25°C		3		
SR	Slew rate at unity gain	$V_{O(PP)} = V_{DD}/2$, C_L = 50 pF, R_L = 10 kΩ	V_{DD} = 2.7 V	25°C	1.4	2		V/μs
				Full range	1			
			V_{DD} = 5 V	25°C	1.4	2.4		V/μs
				Full range	1.2			
			V_{DD} = 15 V	25°C	1.9	2.1		V/μs
				Full range	1.4			
ϕ_m	Phase margin	R_L = 2 kΩ,	C_L = 100 pF	25°C		65°		
	Gain margin	R_L = 2 kΩ,	C_L = 10 pF	25°C		18		dB
t_s	Settling time	V_{DD} = 2.7 V, $V_{(STEP)PP}$ = 1 V, A_V = −1, C_L = 10 pF, R_L = 2 kΩ	0.1%	25°C		2.9		μs
		V_{DD} = 5 V, 15 V, $V_{(STEP)PP}$ = 1 V, A_V = −1, C_L = 47 pF, R_L = 2 kΩ	0.1%			2		

noise/distortion performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	V_{DD} = 2.7 V, $V_{O(PP)} = V_{DD}/2$ V, R_L = 2 kΩ, f = 10 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.05%		
			A_V = 100			0.18%		
		V_{DD} = 5 V, 5 V, $V_{O(PP)} = V_{DD}/2$ V, R_L = 2 kΩ, f = 10 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.09%		
			A_V = 100			0.5%		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		39		nV/√Hz
		f = 10 kHz				35		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2, 3
CMRR	Common-mode rejection ratio	vs Frequency	4
	Input bias and offset current	vs Free-air temperature	5
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8, 10
V_{OH}	High-level output voltage	vs High-level output current	7, 9, 11
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	12
I_{DD}	Supply current	vs Supply voltage	13
PSRR	Power supply rejection ratio	vs Frequency	14
A_{VD}	Differential voltage gain & phase	vs Frequency	15
	Gain-bandwidth product	vs Free-air temperature	16
SR	Slew rate	vs Supply voltage	17
		vs Free-air temperature	18
ϕ_m	Phase margin	vs Capacitive load	19
V_n	Equivalent input noise voltage	vs Frequency	20
	Voltage-follower large-signal pulse response		21, 22
	Voltage-follower small-signal pulse response		23
	Inverting large-signal response		24, 25
	Inverting small-signal response		26
	Crosstalk	vs Frequency	27

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

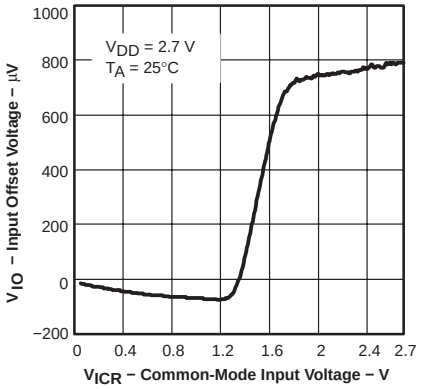


Figure 1

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

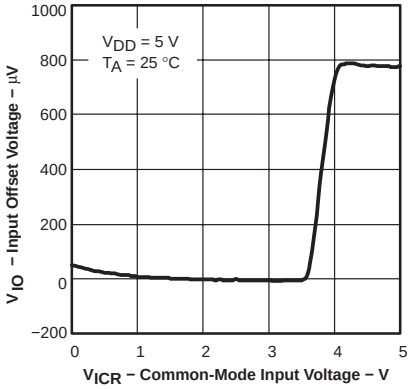


Figure 2

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

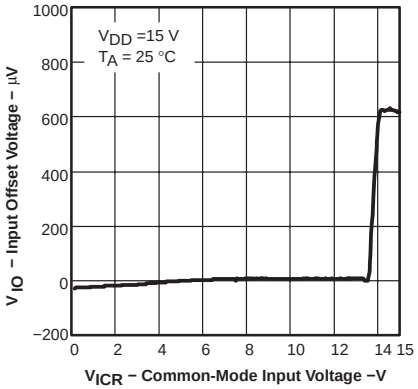


Figure 3

COMMON-MODE REJECTION RATIO vs FREQUENCY

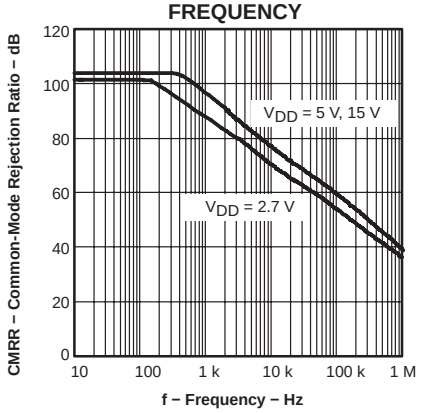


Figure 4

INPUT BIAS/OFFSET CURRENT vs FREE-AIR TEMPERATURE

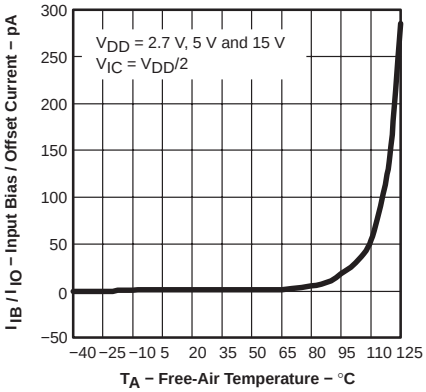


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

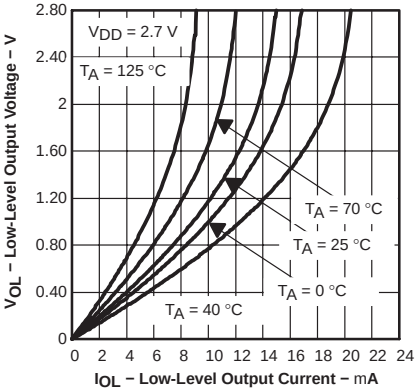


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

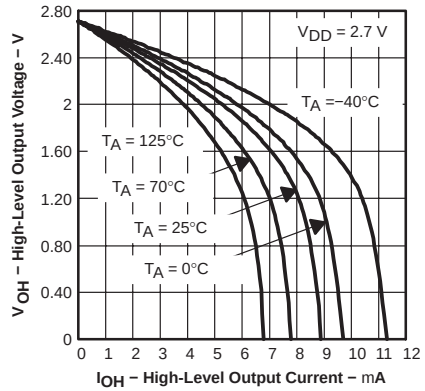


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

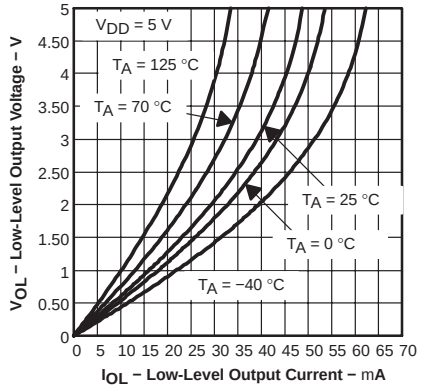


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

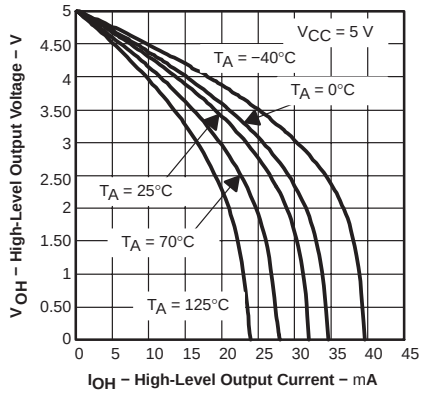


Figure 9

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

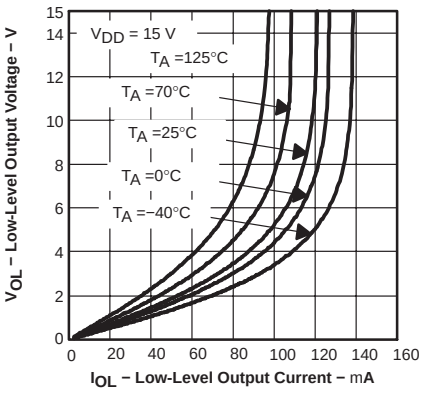


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

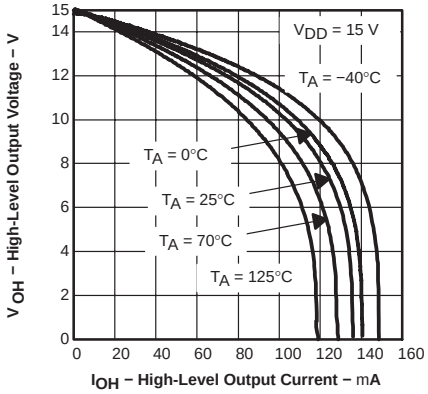


Figure 11

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

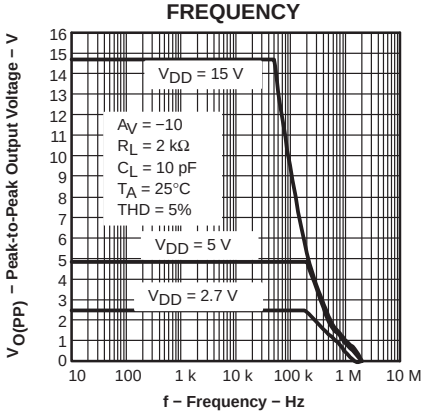


Figure 12

SUPPLY CURRENT vs SUPPLY VOLTAGE

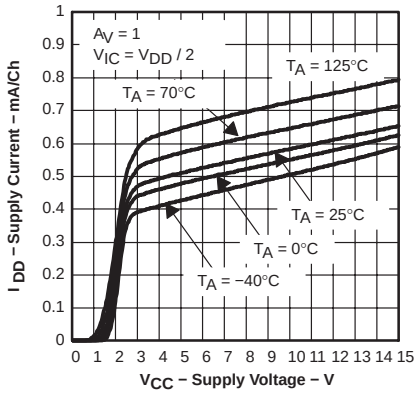


Figure 13

POWER SUPPLY REJECTION RATIO vs FREQUENCY

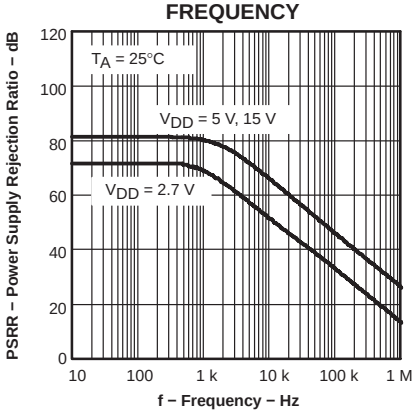


Figure 14

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

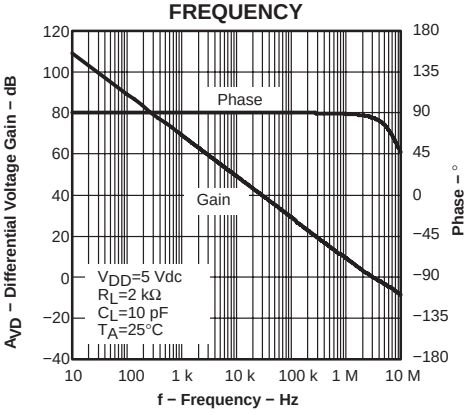


Figure 15

GAIN BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

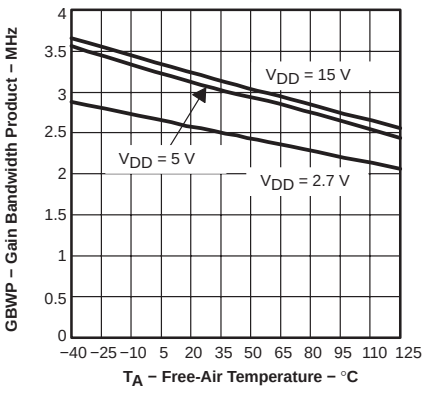


Figure 16

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

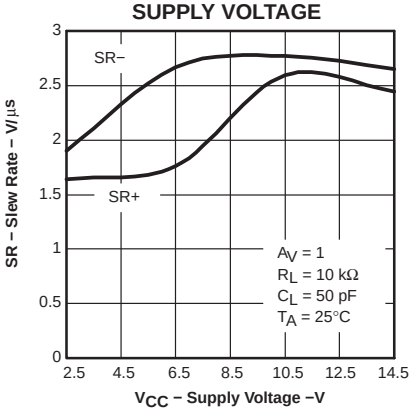


Figure 17

SLEW RATE vs FREE-AIR TEMPERATURE

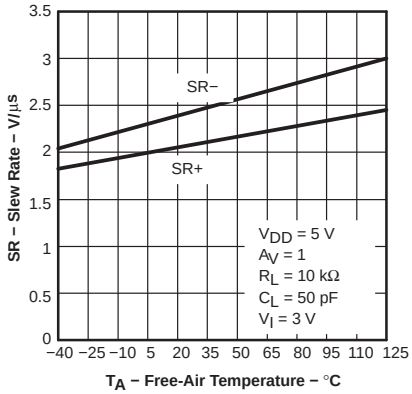


Figure 18

PHASE MARGIN vs CAPACITIVE LOAD

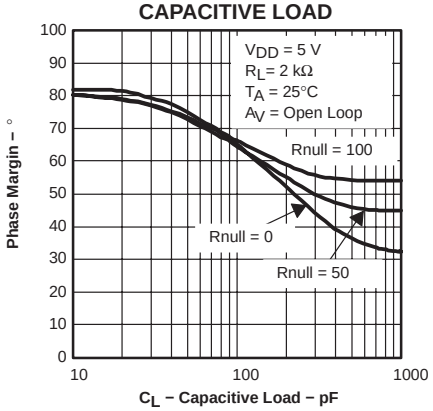


Figure 19

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

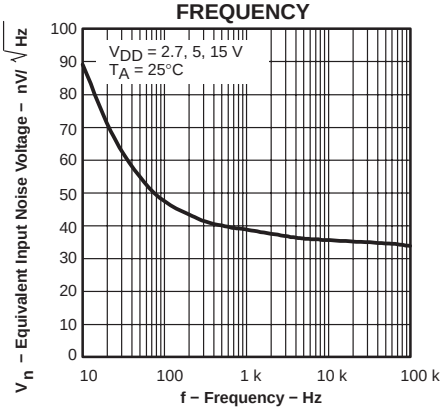


Figure 20

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

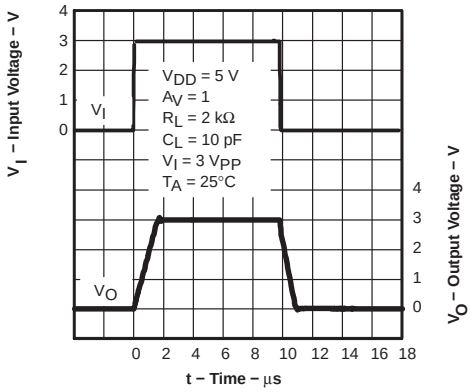


Figure 21

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

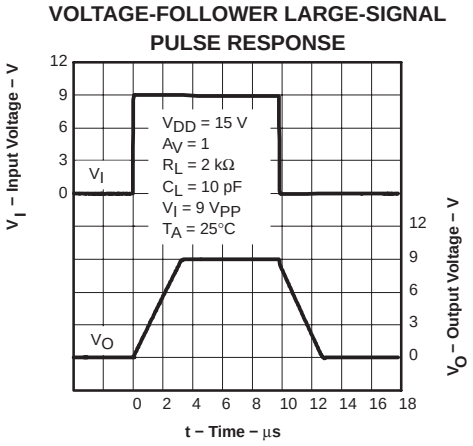


Figure 22

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

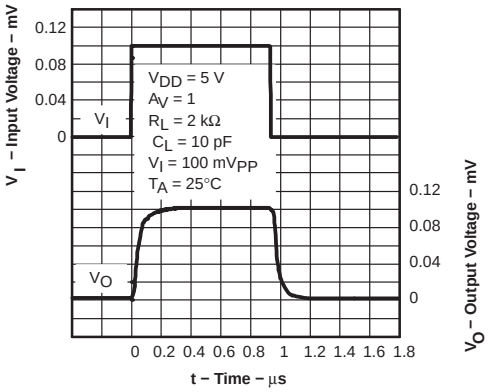


Figure 23

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL RESPONSE

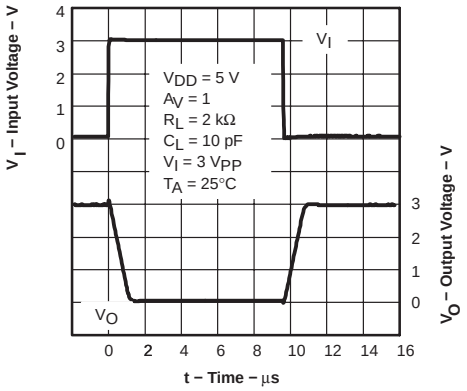


Figure 24

INVERTING LARGE-SIGNAL RESPONSE

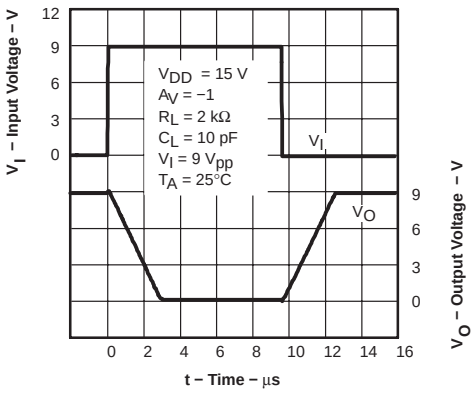


Figure 25

INVERTING SMALL-SIGNAL RESPONSE

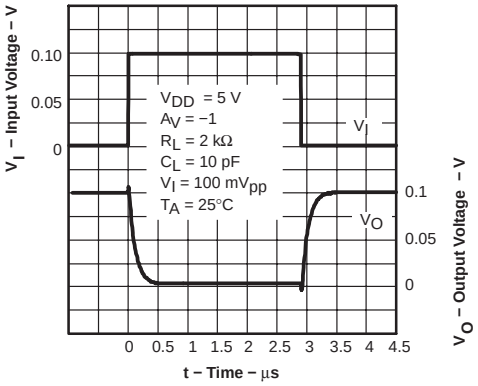


Figure 26

CROSSTALK vs FREQUENCY

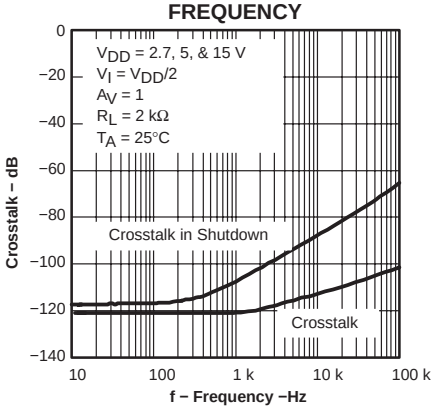


Figure 27

APPLICATION INFORMATION

rail-to-rail input operation

The TLV237x input stage consists of two differential transistor pairs, NMOS and PMOS, that operate together to achieve rail-to-rail input operation. The transition point between these two pairs can be seen in Figure 1 through Figure 3 for a 2.7-V, 5-V, and 15-V supply. As the common-mode input voltage approaches the positive supply rail, the input pair switches from the PMOS differential pair to the NMOS differential pair. This transition occurs approximately 1.35 V from the positive rail and results in a change in offset voltage due to different device characteristics between the NMOS and PMOS pairs. If the input signal to the device is large enough to swing between both rails, this transition results in a reduction in common-mode rejection ratio (CMRR). If the input signal does not swing between both rails, it is best to bias the signal in the region where only one input pair is active. This is the region in Figure 1 through Figure 3 where the offset voltage varies slightly across the input range and optimal CMRR can be achieved. This has the greatest impact when operating from a 2.7-V supply voltage.

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin, leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 28. A minimum value of 20 Ω should work well for most applications.

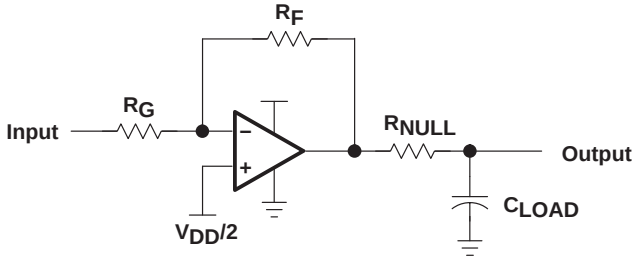
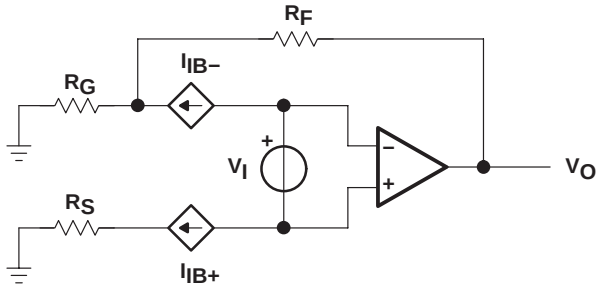


Figure 28. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The schematic and formula in Figure 29 can be used to calculate the output offset voltage.



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 29. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 30).

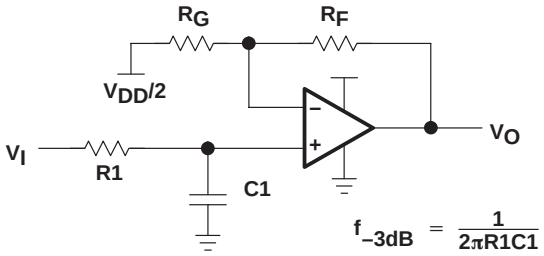


Figure 30. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

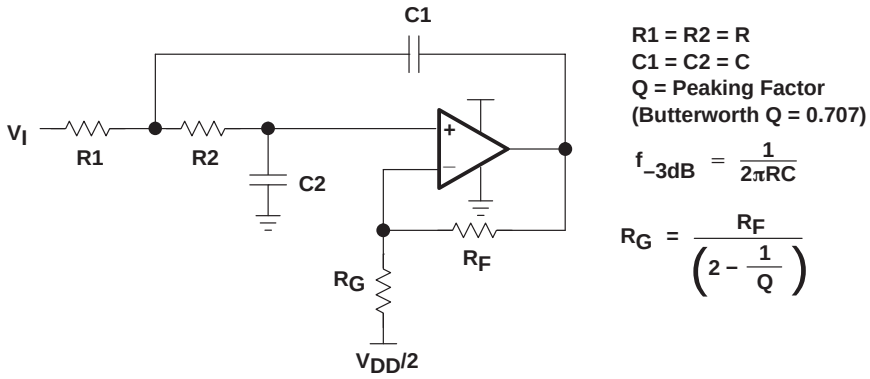


Figure 31. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV237x, follow proper printed-circuit board design techniques. The following is a general set of guidelines.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum capacitor among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

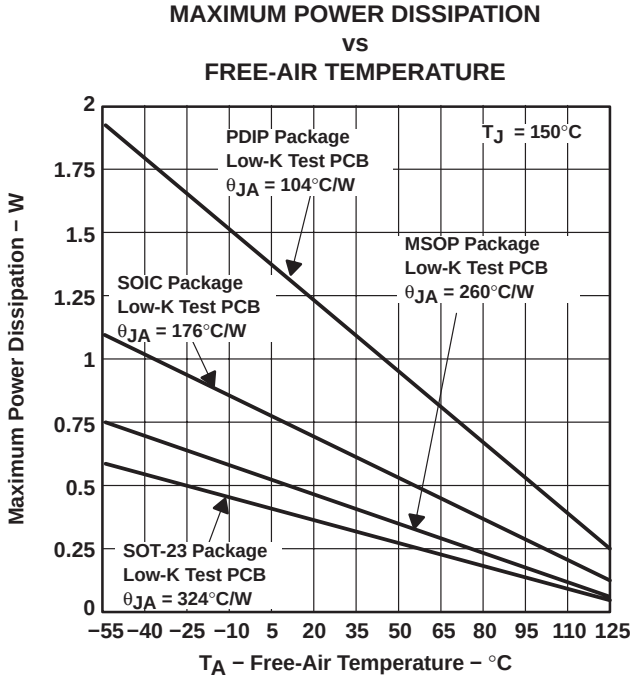
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 32 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV237x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 32.

PACKAGING INFORMATION

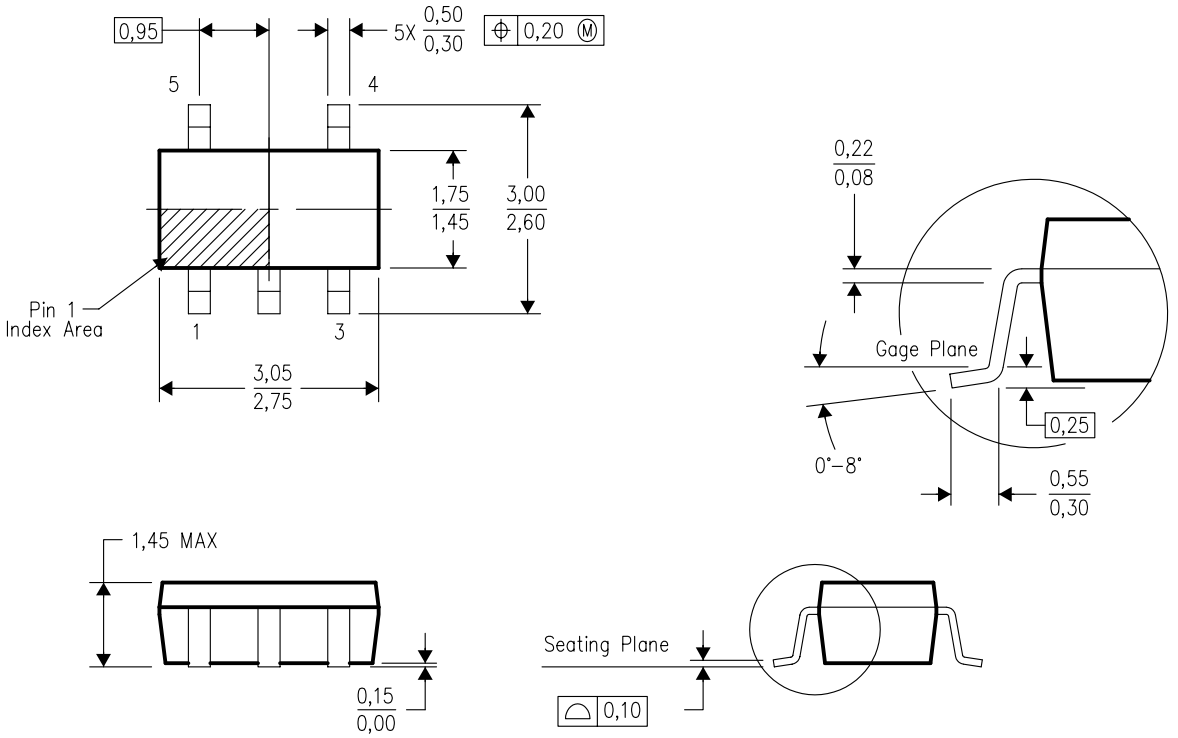
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV2371QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2371QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2372QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2372QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2374QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2374QDRQ1	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2374QPWRQ1	ACTIVE	TSSOP	PW	14	2000	TBD	CU NIPDAU	Level-1-250C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

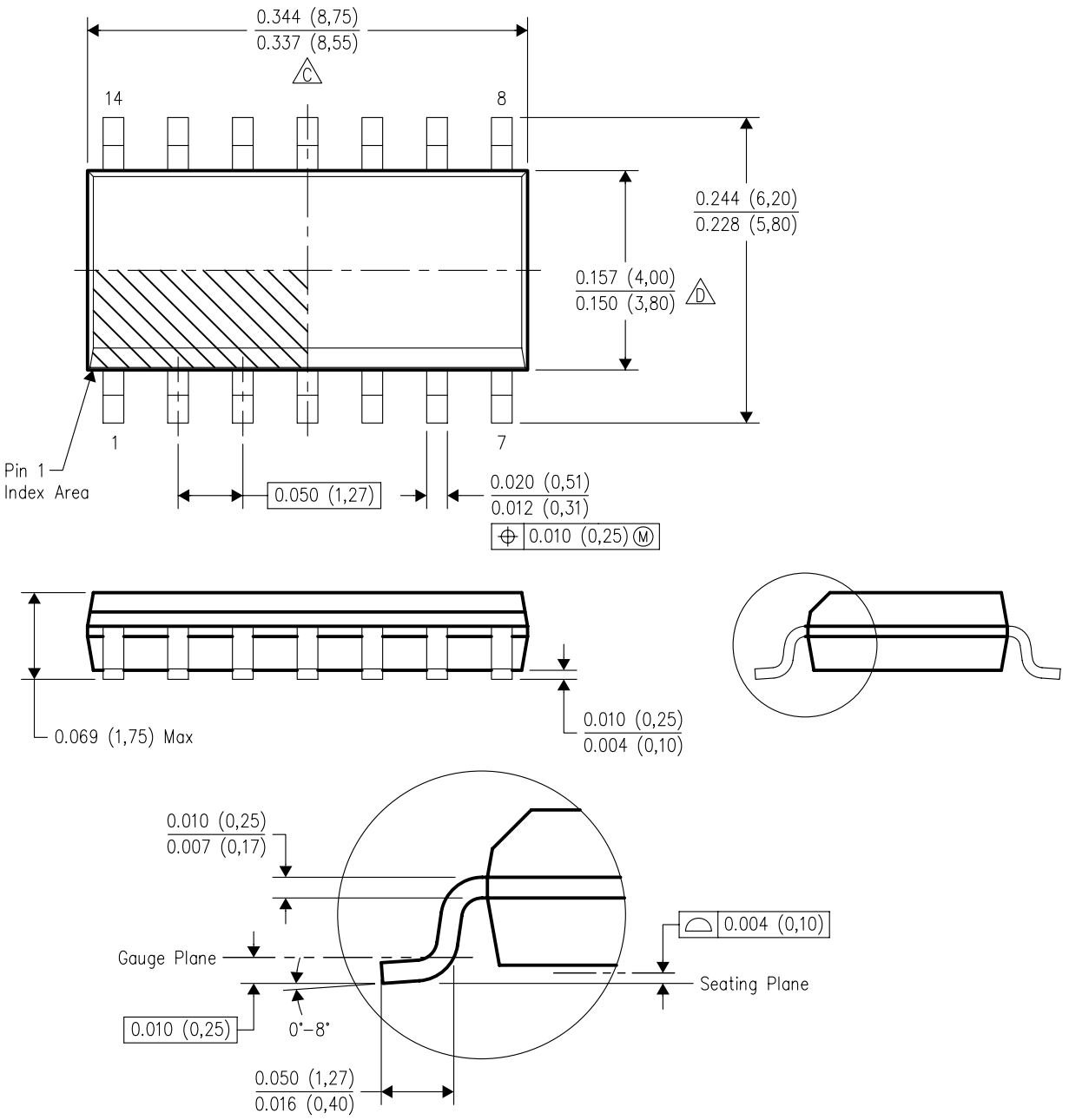
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

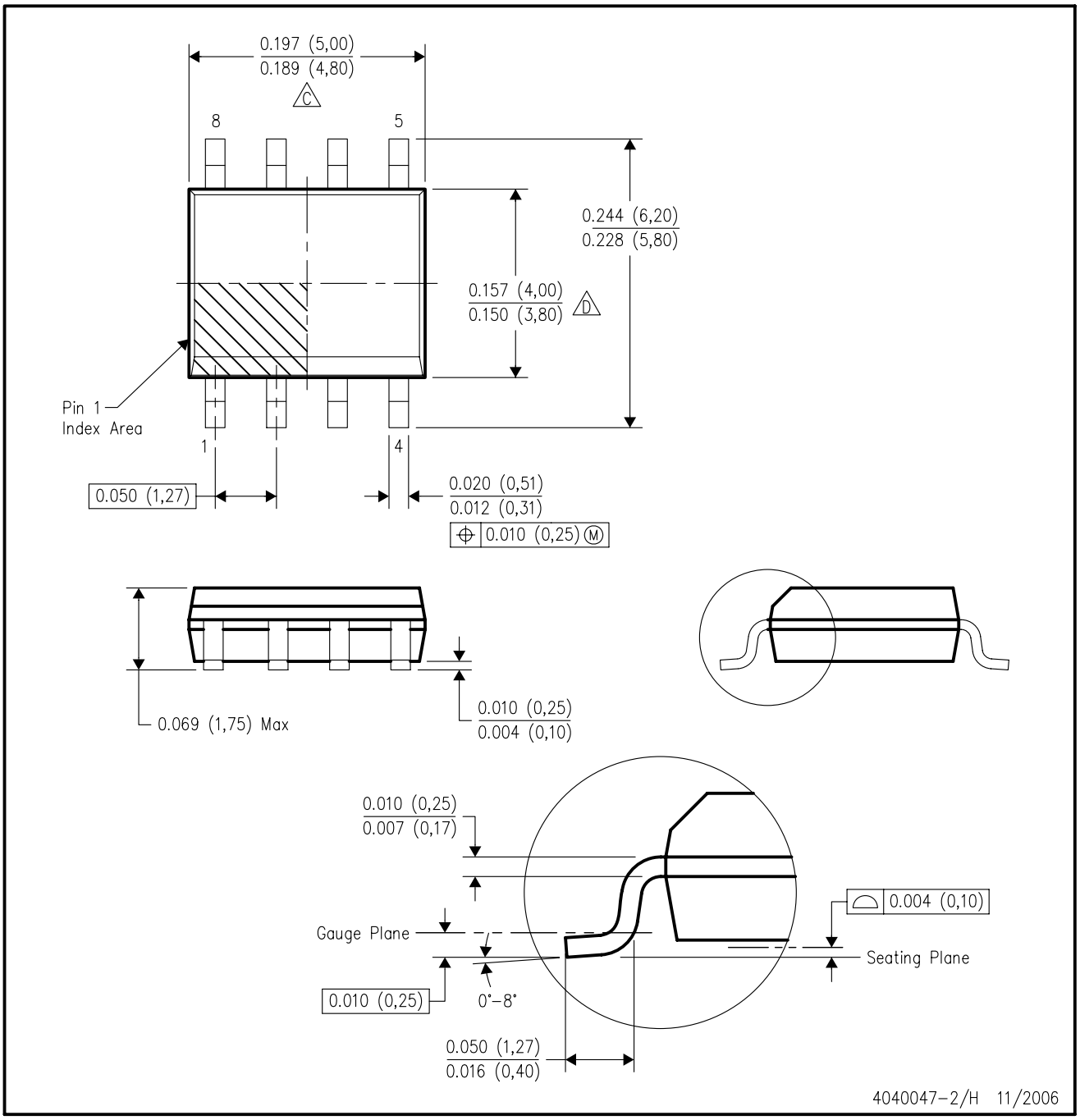
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

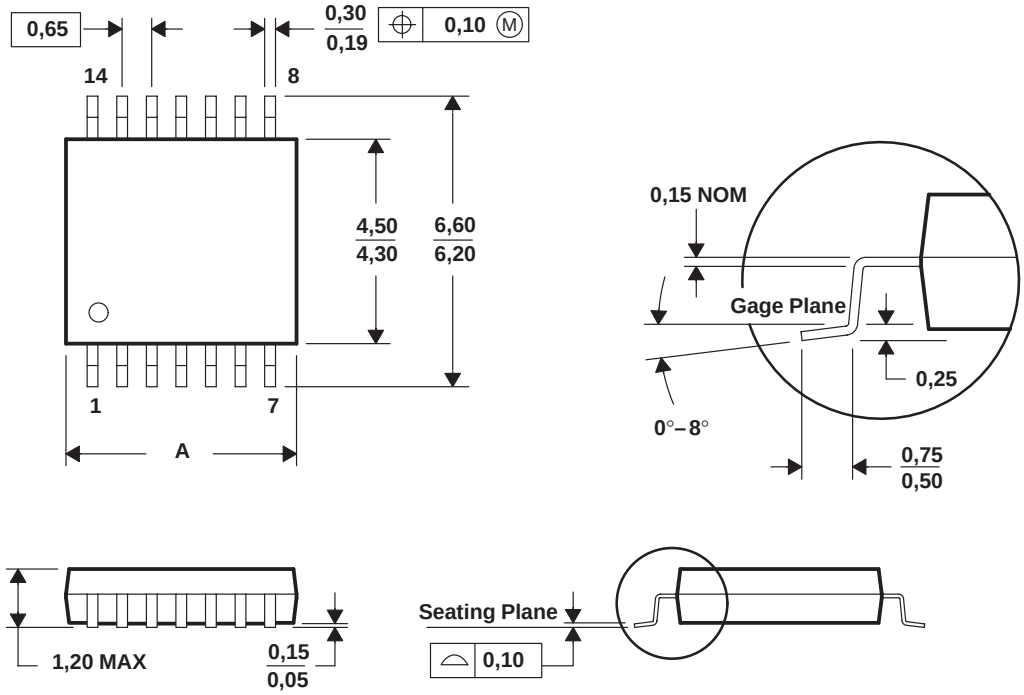
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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