

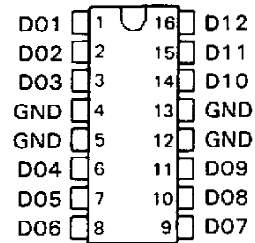
# SN74S1050

## 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

SDLS015A D3228, JULY 1989—REVISED MARCH 1990

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current . . . 200 mA
- 12-Bit Array Structure Suited for Bus-Oriented Systems
- ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

D OR N PACKAGE  
(TOP VIEW)

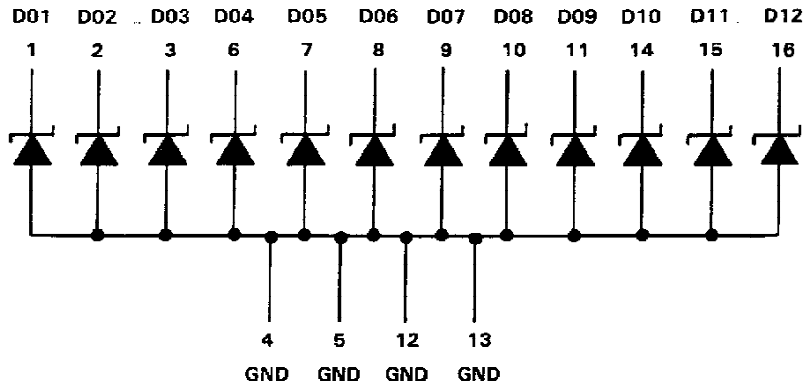


### description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1050 is characterized for operation from 0°C to 70°C.

### schematic diagram



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# SN74S1050

## 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3228, JULY 1989—REVISED MARCH 1990

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Steady-state reverse voltage, $V_R$ .....	7 V
Continuous forward current, $I_F$ : any D terminal from GND .....	50 mA
total through all GND terminals .....	170 mA
Repetitive peak forward current, <sup>‡</sup> $I_{FRM}$ : any D terminal from GND .....	200 mA
total through all GND terminals .....	1 A
Continuous total power dissipation at (or below) 25°C free-air temperature .....	625 mW
Operating free-air temperature range .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

<sup>†</sup>Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>‡</sup>These values apply for  $t_W \leq 100 \mu s$ , duty cycle  $\leq 20\%$ .

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

#### single-diode operation (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>§</sup>	MAX	UNIT
$I_R$ Static reverse current	$V_R = 7 V$			5	$\mu A$
$V_F$ Static forward voltage	$I_F = 18 mA$	0.75	0.95		V
	$I_F = 50 mA$	0.95	1.2		
$V_{FM}$ Peak forward voltage	$I_F = 200 mA$	1.45			V
$C_T$ Total capacitance	$V_R = 0, f = 1 MHz$		5	10	pF
	$V_R = 2 V, f = 1 MHz$		4	8	

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

#### multiple-diode operation

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>§</sup>	MAX	UNIT
$I_X$ Internal crosstalk current	Total $I_F = 1 A$ , See Note 2		0.6	2	mA
	Total $I_F = 198 mA$ , See Note 2		0.02	0.2	

<sup>§</sup>All typical values are at  $T_A = 25^\circ C$ .

NOTE 2.  $I_X$  is measured under the following conditions with one diode static and all others switching:

Switching diodes:  $t_W = 100 \mu s$ , duty cycle = 20%; static diode:  $V_R = 5 V$ .

The static diode's input current is the internal crosstalk current  $I_X$ .

#### switching characteristics at 25°C free-air temperature (see Figures 1 and 2)

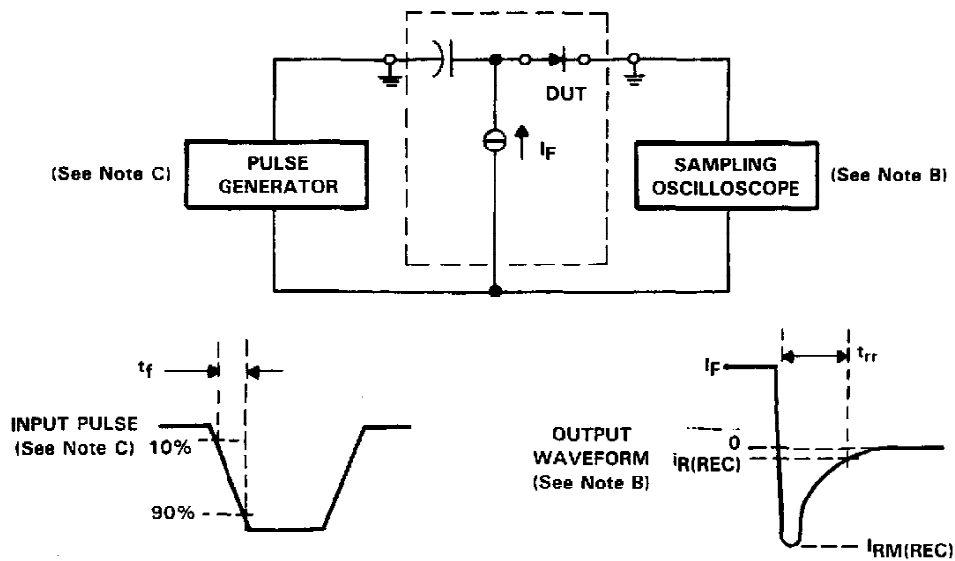
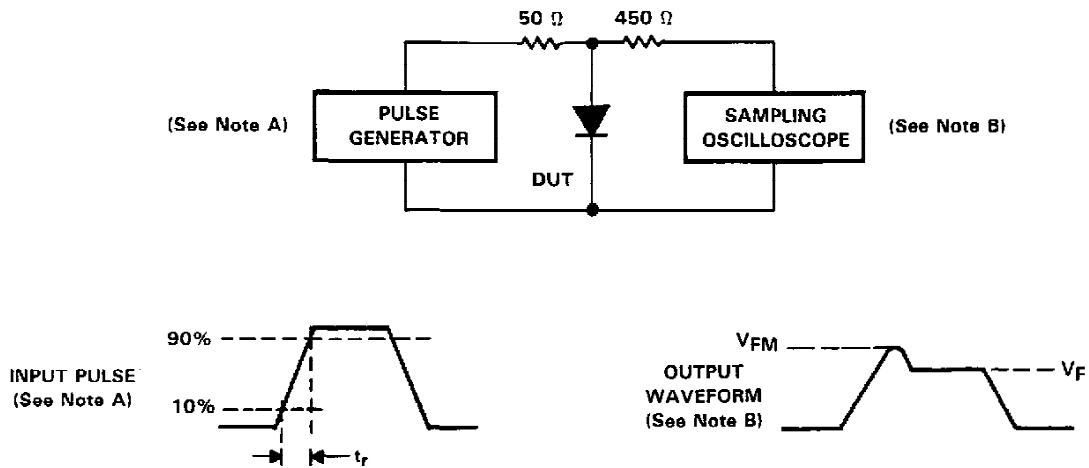
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr}$ Reverse recovery time	$I_F = 10 mA, I_{RM(REC)} = 10 mA, I_{R(REC)} = 1 mA, R_L = 100 \Omega$		8	16	ns

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**SN74S1050**  
**12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY**

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics:  $t_r = 20$  ns,  $Z_{out} = 50$   $\Omega$ ,  $f = 500$  Hz, duty cycle = 0.01.
- B. The output waveform is monitored by an oscilloscope having the following characteristics:  $t_r \leq 350$  ps,  $R_{in} = 50$   $\Omega$ ,  $C_{in} = \leq 5$  pF.
- C. The input pulse is supplied by a pulse generator having the following characteristics:  $t_f = 0.5$  ns,  $Z_{out} = 50$   $\Omega$ ,  $t_w = \geq 50$  ns, duty cycle  $\leq 0.01$ .

# SN74S1050 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

## APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1052 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1052 is shown in Figure 3.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 4 was evaluated. The resulting waveforms with and without the diode are shown in Figure 5.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

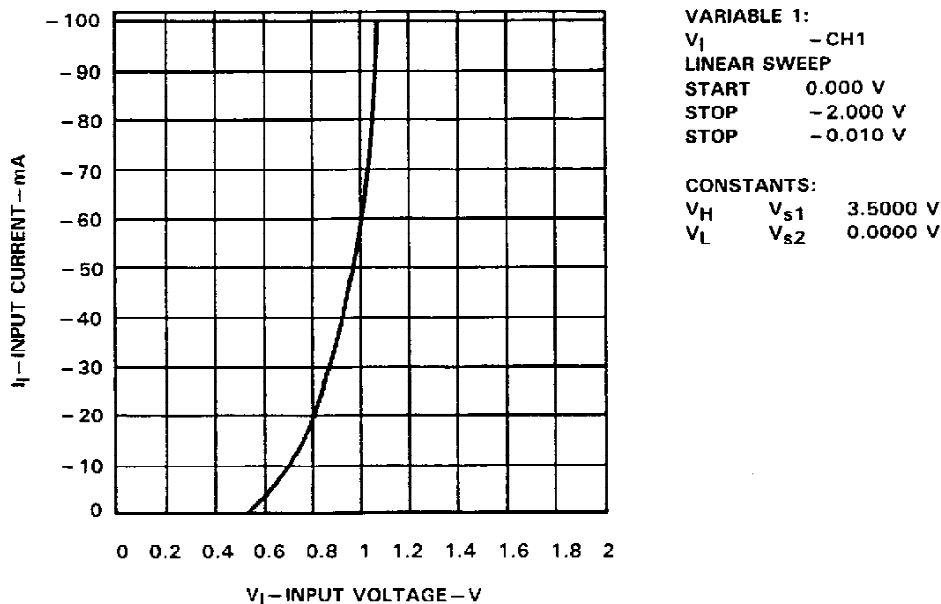


FIGURE 3. TYPICAL CURRENT-VOLTAGE CURVE

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74S1050D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1050DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1050DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1050DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1050DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1050DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1050N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S1050NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



**TAPE AND REEL INFORMATION**

**PACKAGING INFORMATION**

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SN74S1050DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
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SN74S1050N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S1050NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74S1050DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74S1050DR	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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