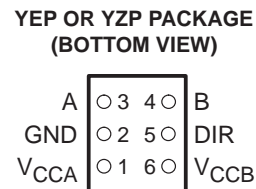
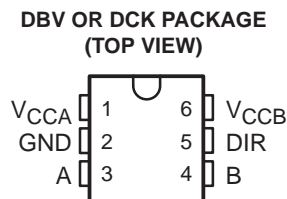


SN74LVC1T45

SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 4-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Max Data Rates
 - 420 Mbps (3.3-V to 5-V Translation)
 - 210 Mbps (Translate to 3.3 V)
 - 140 Mbps (Translate to 2.5 V)
 - 75 Mbps (Translate to 1.8 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



description/ordering information

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC1T45 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

ORDERING INFORMATION

T _A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡	
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74LVC1T45YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1T45YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1T45DBVR	CT1_
		Reel of 250	SN74LVC1T45DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1T45DCKR	TA_
		Reel of 250	SN74LVC1T45DCKT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description/ordering information (continued)

The SN74LVC1T45 is designed so that the DIR input circuit is supplied by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

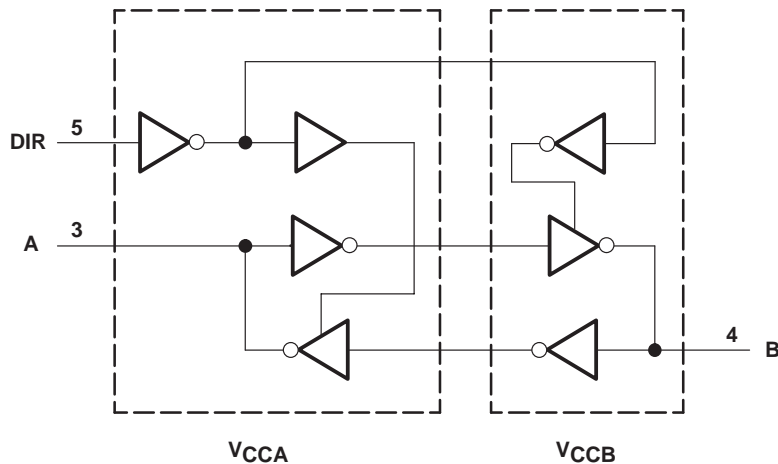
The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

FUNCTION TABLE

INPUT	OPERATION
DIR	
L	B data to A bus
H	A data to B bus

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB}	-0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2): A port	-0.5 V to $V_{CCA} + 0.5V$
B port	-0.5 V to $V_{CCB} + 0.5V$
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3): DBV package	165°C/W
DCK package	259°C/W
YEP/YZP package	123°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Notes 4 through 8)

		V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage			1.65	5.5	V
V _{CCB}				1.65	5.5	
V _{IH}	High-level input voltage	Data inputs (see Note 7)	1.65 V to 1.95 V		V _{CCI} × 0.65	V
			2.3 V to 2.7 V		1.7	
			3 V to 3.6 V		2	
			4.5 V to 5.5 V		V _{CCI} × 0.7	
V _{IL}	Low-level input voltage	Data inputs (see Note 7)	1.65 V to 1.95 V		V _{CCI} × 0.35	V
			2.3 V to 2.7 V		0.7	
			3 V to 3.6 V		0.8	
			4.5 V to 5.5 V		V _{CCI} × 0.3	
V _{IH}	High-level input voltage	DIR (Referenced to V _{CCA}) (see Note 8)	1.65 V to 1.95 V		V _{CCA} × 0.65	V
			2.3 V to 2.7 V		1.7	
			3 V to 3.6 V		2	
			4.5 V to 5.5 V		V _{CCA} × 0.7	
V _{IL}	Low-level input voltage	DIR (Referenced to V _{CCA}) (see Note 8)	1.65 V to 1.95 V		V _{CCA} × 0.35	V
			2.3 V to 2.7 V		0.7	
			3 V to 3.6 V		0.8	
			4.5 V to 5.5 V		V _{CCA} × 0.3	
V _I	Input voltage			0	5.5	V
V _O	Output voltage			0	V _{CCO}	V
I _{OH}	High-level output current		1.65 V to 1.95 V		-4	mA
			2.3 V to 2.7 V		-8	
			3 V to 3.6 V		-24	
			4.5 V to 5.5 V		-32	
I _{OL}	Low-level output current		1.65 V to 1.95 V		4	mA
			2.3 V to 2.7 V		8	
			3 V to 3.6 V		24	
			4.5 V to 5.5 V		32	
Δt/Δv	Input transition rise or fall rate	Data input	1.65 V to 1.95 V		20	ns/V
			2.3 V to 2.7 V		20	
			3 V to 3.6 V		10	
			4.5 V to 5.5 V		5	
		Control input	1.65 V to 5.5 V		5	
T _A	Operating free-air temperature			-40	85	°C

- NOTES:
- V_{CCI} is the V_{CC} associated with the data input port.
 - V_{CCO} is the V_{CC} associated with the output port.
 - All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
 - For V_{CCI} values not specified in the data sheet, V_{IH(min)} = V_{CCI} × 0.7 V, V_{IL(max)} = V_{CCI} × 0.3 V.
 - For V_{CCI} values not specified in the data sheet, V_{IH(min)} = V_{CCA} × 0.7 V, V_{IL(max)} = V_{CCA} × 0.3 V.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			-40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -100 μA, V _I = V _{IH}	1.65 V to 4.5 V	1.65 V to 4.5 V				V _{CCO} -0.1		V
	I _{OH} = -4 mA, V _I = V _{IH}	1.65 V	1.65 V				1.2		
	I _{OH} = -8 mA, V _I = V _{IH}	2.3 V	2.3 V				1.9		
	I _{OH} = -24 mA, V _I = V _{IH}	3 V	3 V				2.4		
	I _{OH} = -32 mA, V _I = V _{IH}	4.5 V	4.5 V				3.8		
V _{OL}	I _{OL} = 100 μA, V _I = V _{IL}	1.65 V to 4.5 V	1.65 V to 4.5 V				0.1		V
	I _{OL} = 4 mA, V _I = V _{IL}	1.65 V	1.65 V				0.45		
	I _{OL} = 8 mA, V _I = V _{IL}	2.3 V	2.3 V				0.3		
	I _{OL} = 24 mA, V _I = V _{IL}	3 V	3 V				0.55		
	I _{OL} = 32 mA, V _I = V _{IL}	4.5 V	4.5 V				0.55		
I _I	DIR input	V _I = V _{CCA} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±1	±2	μA
I _{off}	A port	V _I or V _O = 0 to 5.5 V	0 V	0 to 5.5 V			±1	±2	μA
	B port		0 to 5.5 V	0 V			±1	±2	
I _{OZ}	A or B ports	V _O = V _{CCO} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±1	±2	μA
I _{CCA}	V _I = V _{CCI} or GND	I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				3	μA
			5.5 V	0 V				2	
			0 V	5.5 V				0	
I _{CCB}	V _I = V _{CCI} or GND	I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				3	μA
			5.5 V	0 V				0	
			0 V	5.5 V				2	
I _{CCA} + I _{CCB}	V _I = V _{CCI} or GND	I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				4	μA
ΔI _{CCA}	A port	A port at V _{CCA} - 0.6 V, DIR at V _{CCA} , B port = OPEN	3 V to 5.5 V	3 V to 5.5 V				50	μA
	DIR	DIR at V _{CCA} - 0.6 V, B port = OPEN, A port at V _{CCA} or GND						50	
ΔI _{CCB}	B port	B port at V _{CCB} - 0.6 V, DIR at GND, A port = OPEN	3 V to 5.5 V	3 V to 5.5 V				50	μA
C _i	DIR input	V _I = V _{CCA} or GND	3.3 V	3.3 V			2.5		pF
C _{io}	A or B ports	V _O = V _{CCA/B} or GND	3.3 V	3.3 V			6		pF

NOTES: 9. V_{CCO} is the V_{CC} associated with the output port.
10. V_{CCI} is the V_{CC} associated with the input port.



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switching characteristics over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	17.7	2.2	10.3	1.7	8.3	1.4	7.2	ns
t_{PHL}			2.8	14.3	2.2	8.5	1.8	7.1	1.7	7	
t_{PLH}	B	A	3	17.7	2.3	16	2.1	15.5	1.9	15.1	ns
t_{PHL}			2.8	14.3	2.1	12.9	2	12.6	1.8	12.2	
t_{PHZ}	DIR	A	5.2	19.4	4.8	18.5	4.7	18.4	5.1	17.1	ns
t_{PLZ}			2.3	10.5	2.1	10.5	2.4	10.7	3.1	10.9	
t_{PHZ}	DIR	B	7.4	21.9	4.9	11.5	4.6	10.3	2.8	8.2	ns
t_{PLZ}			4.2	16	3.7	9.2	3.3	8.4	2.4	6.4	
t_{PZH}^{\dagger}	DIR	A	33.7		25.2		23.9		21.5		ns
t_{PZL}^{\dagger}			36.2		24.4		22.9		20.4		
t_{PZH}^{\dagger}	DIR	B	28.2		20.8		19		18.1		ns
t_{PZL}^{\dagger}			33.7		27		25.5		24.1		

† The enable time is a calculated value, derived using the formula shown in the section entitled *enable times* on page 16.

switching characteristics over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	16	1.5	8.5	1.3	6.4	1.1	5.1	ns
t_{PHL}			2.1	12.9	1.4	7.5	1.3	5.4	0.9	4.6	
t_{PLH}	B	A	2.2	10.3	1.5	8.5	1.4	8	1	7.5	ns
t_{PHL}			2.2	8.5	1.4	7.5	1.3	7	0.9	6.2	
t_{PHZ}	DIR	A	3	8.1	3.1	8.1	2.8	8.1	3.2	8.1	ns
t_{PLZ}			1.3	5.9	1.3	5.9	1.3	5.9	1	5.8	
t_{PHZ}	DIR	B	6.5	23.7	4.1	11.4	3.9	10.2	2.4	7.1	ns
t_{PLZ}			3.9	18.9	3.2	9.6	2.8	8.4	1.8	5.3	
t_{PZH}^{\dagger}	DIR	A	29.2		18.1		16.4		12.8		ns
t_{PZL}^{\dagger}			32.2		18.9		17.2		13.3		
t_{PZH}^{\dagger}	DIR	B	21.9		14.4		12.3		10.9		ns
t_{PZL}^{\dagger}			21		15.6		13.5		12.7		

† The enable time is a calculated value, derived using the formula shown in the section entitled *enable times* on page 16.



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switching characteristics over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	15.5	1.4	8	0.7	5.8	0.7	4.4	ns
t_{PHL}			2	12.6	1.3	7	0.8	5	0.7	4	
t_{PLH}	B	A	1.7	8.3	1.3	6.4	0.7	5.8	0.6	5.4	ns
t_{PHL}			1.8	7.1	1.3	5.4	0.8	5	0.7	4.5	
t_{PHZ}	DIR	A	2.9	7.3	3	7.3	2.8	7.3	3.4	7.3	ns
t_{PLZ}			1.8	5.6	1.6	5.6	2.2	5.7	2.2	5.7	
t_{PHZ}	DIR	B	5.4	20.5	3.9	10.1	2.9	8.8	2.4	6.8	ns
t_{PLZ}			3.3	14.5	2.9	7.8	2.4	7.1	1.7	4.9	
t_{PZH}^{\dagger}	DIR	A	22.8		14.2		12.9		10.3		ns
t_{PZL}^{\dagger}			27.6		15.5		13.8		11.3		
t_{PZH}^{\dagger}	DIR	B	21.1		13.6		11.5		10.1		ns
t_{PZL}^{\dagger}			19.9		14.3		12.3		11.3		

\dagger The enable time is a calculated value, derived using the formula shown in the section entitled *enable times* on page 16.

switching characteristics over recommended operating free-air temperature range, $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	15.1	1	7.5	0.6	5.4	0.5	3.9	ns
t_{PHL}			1.8	12.2	0.9	6.2	0.7	4.5	0.5	3.5	
t_{PLH}	B	A	1.4	7.2	1	5.1	0.7	4.4	0.5	3.9	ns
t_{PHL}			1.7	7	0.9	4.6	0.7	4	0.5	3.5	
t_{PHZ}	DIR	A	2.1	5.4	2.2	5.4	2.2	5.5	2.2	5.4	ns
t_{PLZ}			0.9	3.8	1	3.8	1	3.7	0.9	3.7	
t_{PHZ}	DIR	B	4.8	20.2	2.5	9.8	1	8.5	2.5	6.5	ns
t_{PLZ}			4.2	14.8	2.5	7.4	2.5	7	1.6	4.5	
t_{PZH}^{\dagger}	DIR	A	22		12.5		11.4		8.4		ns
t_{PZL}^{\dagger}			27.2		14.4		12.5		10		
t_{PZH}^{\dagger}	DIR	B	18.9		11.3		9.1		7.6		ns
t_{PZL}^{\dagger}			17.6		11.6		10		8.9		

\dagger The enable time is a calculated value, derived using the formula shown in the section entitled *enable times* on page 16.



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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.8\text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3\text{ V}$	$V_{CCA} =$ $V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA}^\dagger	A port input, B port output	$C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$	3	4	4	4	pF
	B port input, A port output		18	19	20	21	
C_{pdB}^\dagger	A port input, B port output		18	19	20	21	
	B port input, A port output		3	4	4	4	

† Power-dissipation capacitance per transceiver



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power-up considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. Take the following precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA} .
3. V_{CCB} can be ramped up along with or after V_{CCA} .

typical total static power consumption ($I_{CCA} + I_{CCB}$)

Table 1

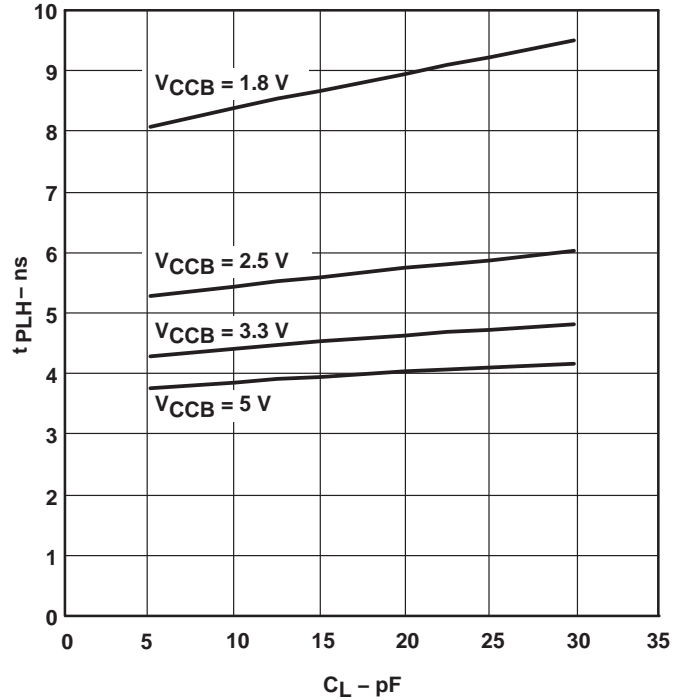
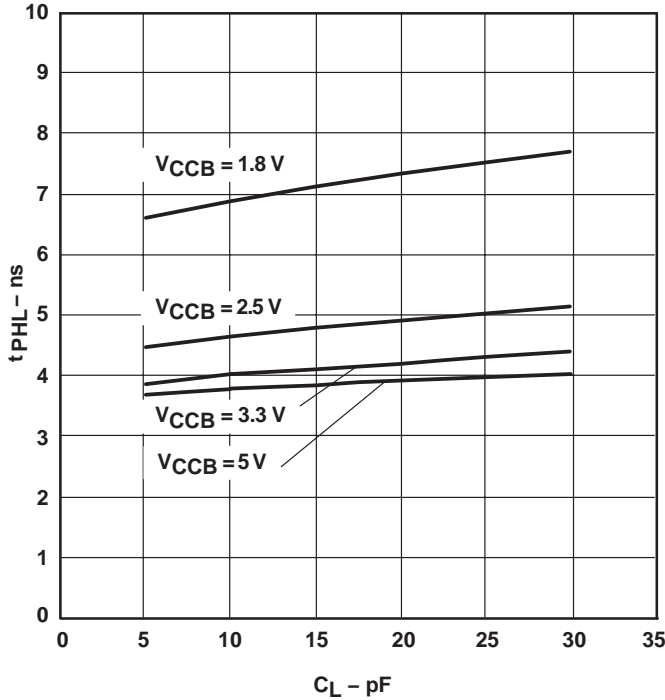
V_{CCB}	V_{CCA}					UNIT
	0 V	1.8 V	2.5 V	3.3 V	5 V	
0 V	0	<1	<1	<1	<1	μA
1.8 V	<1	<2	<2	<2	2	
2.5 V	<1	<2	<2	<2	<2	
3.3 V	<1	<2	<2	<2	<2	
5 V	<1	2	<2	<2	<2	

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WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

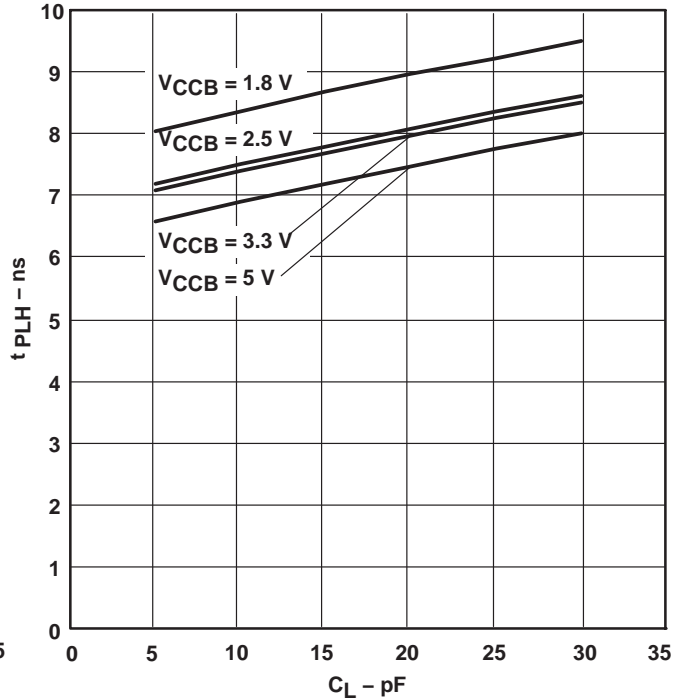
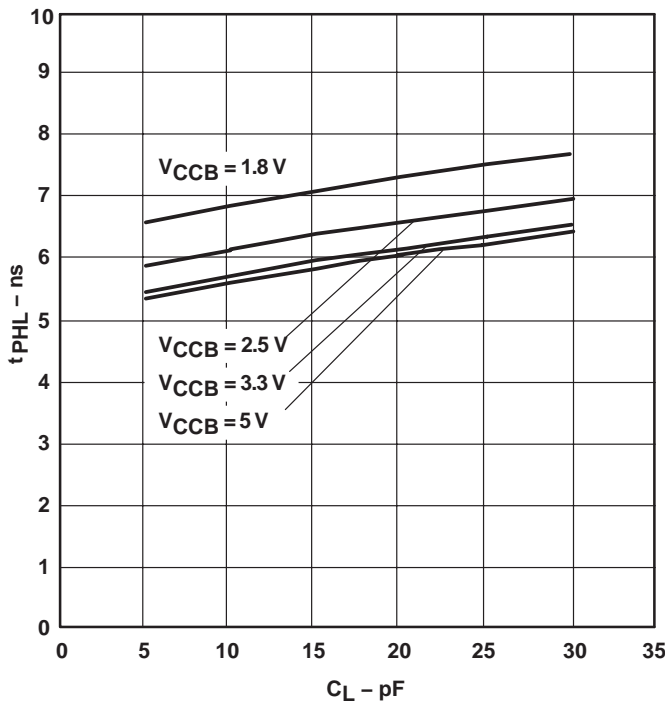
SCES515E – DECEMBER 2003 – REVISED MAY 2004

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$



TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

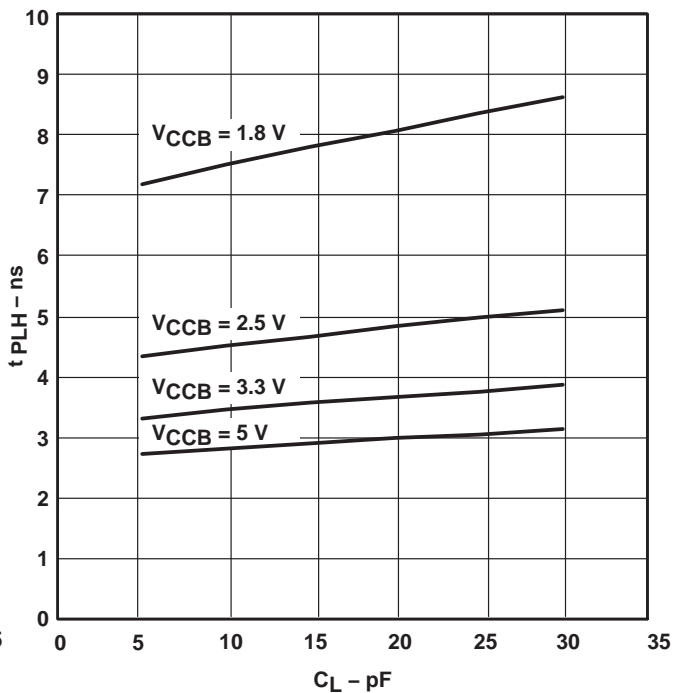
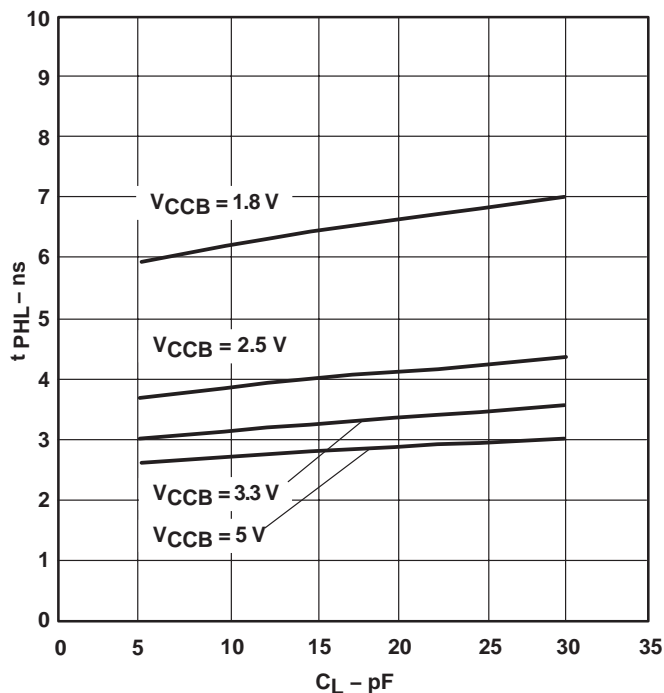


SN74LVC1T45
SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

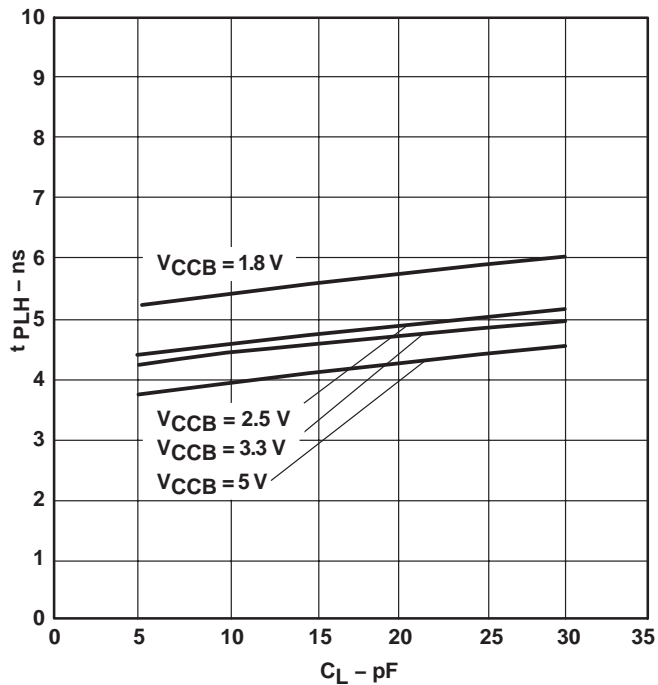
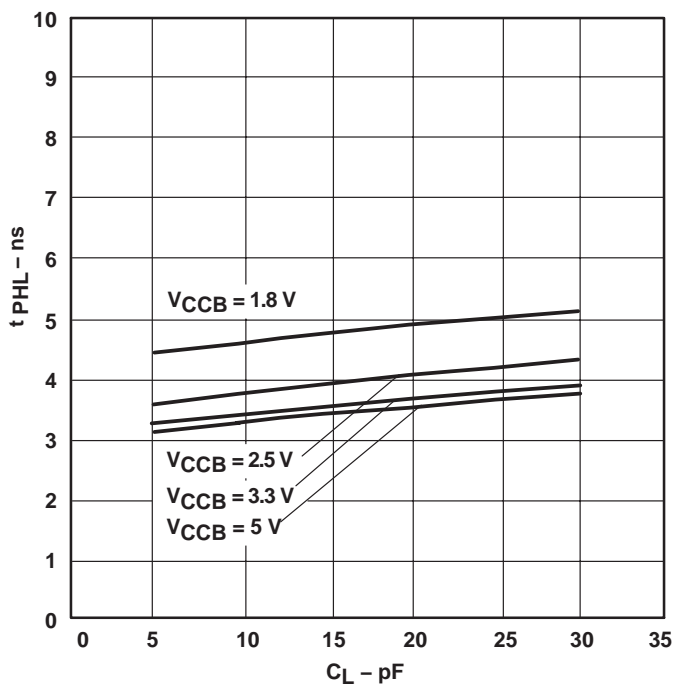
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TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$



TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

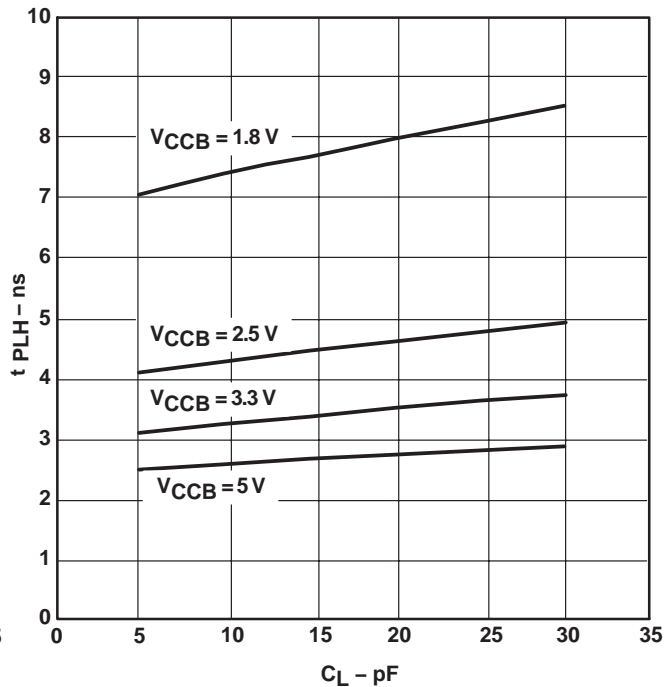
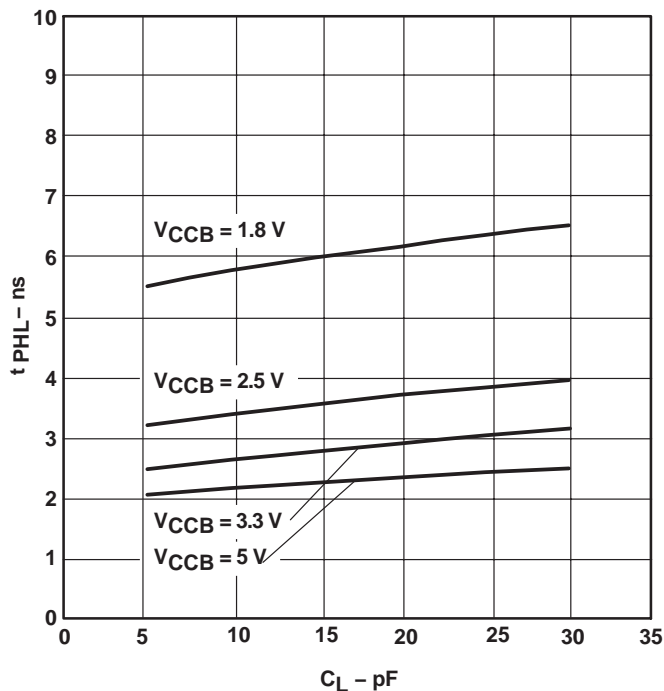


SN74LVC1T45
SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

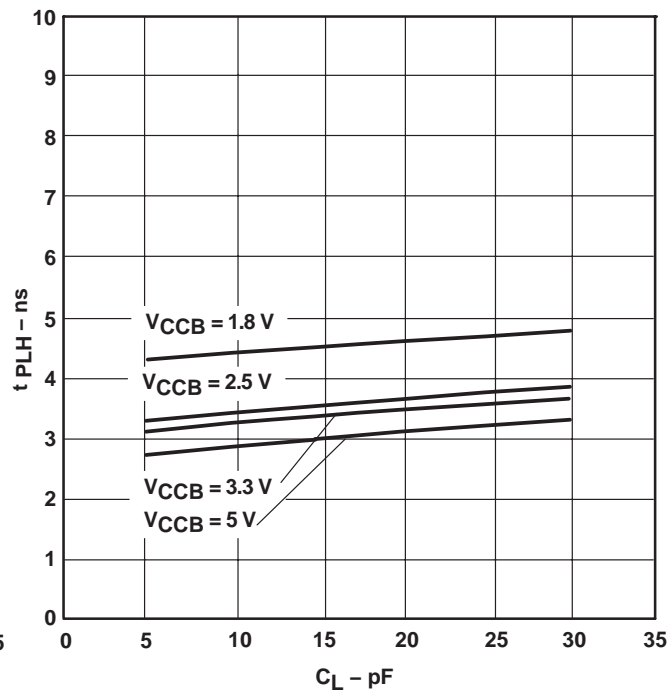
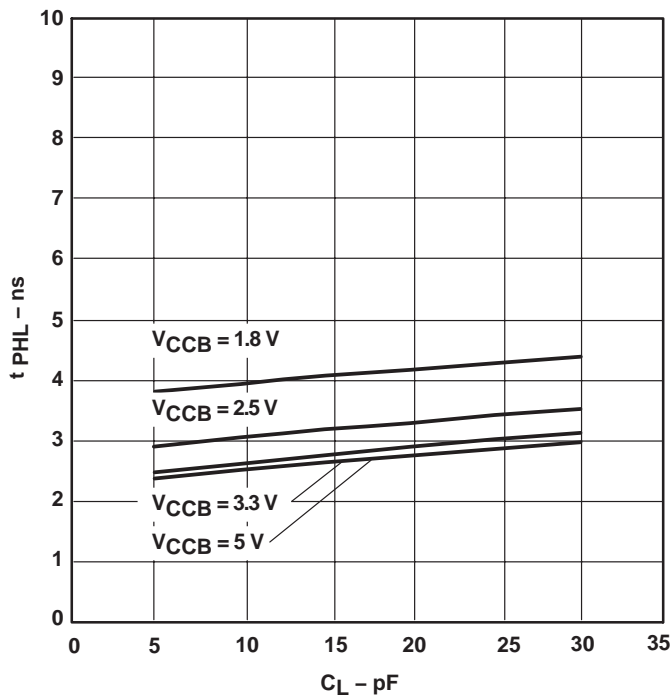
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TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$



TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

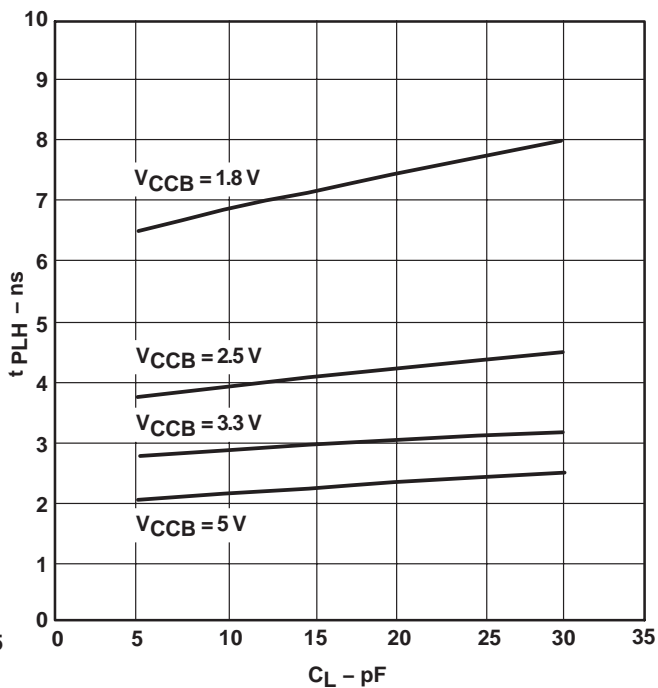
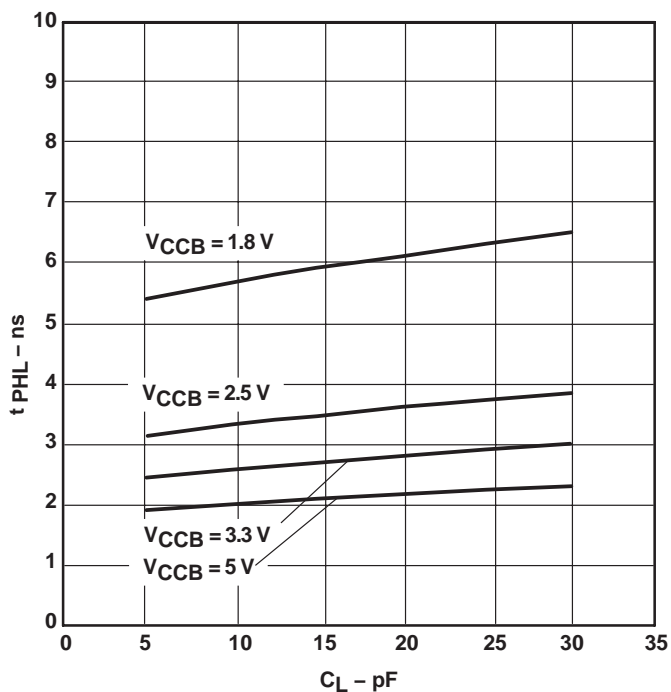


SN74LVC1T45
SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

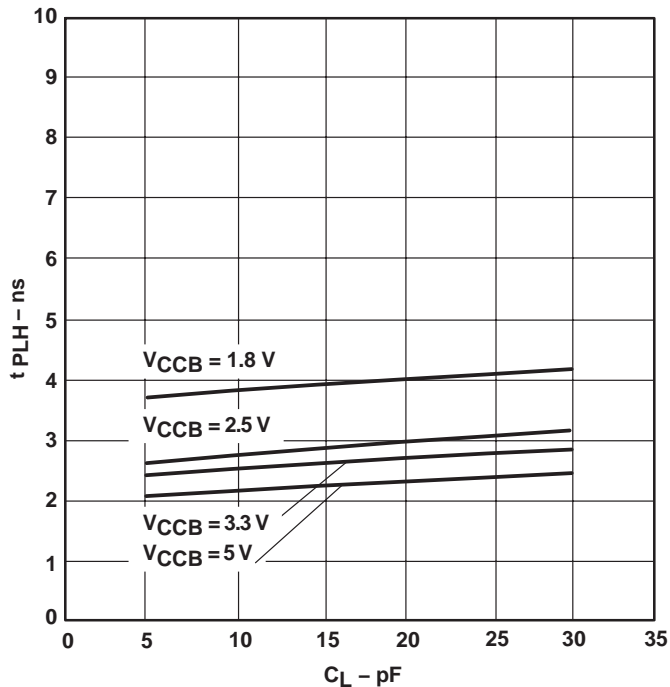
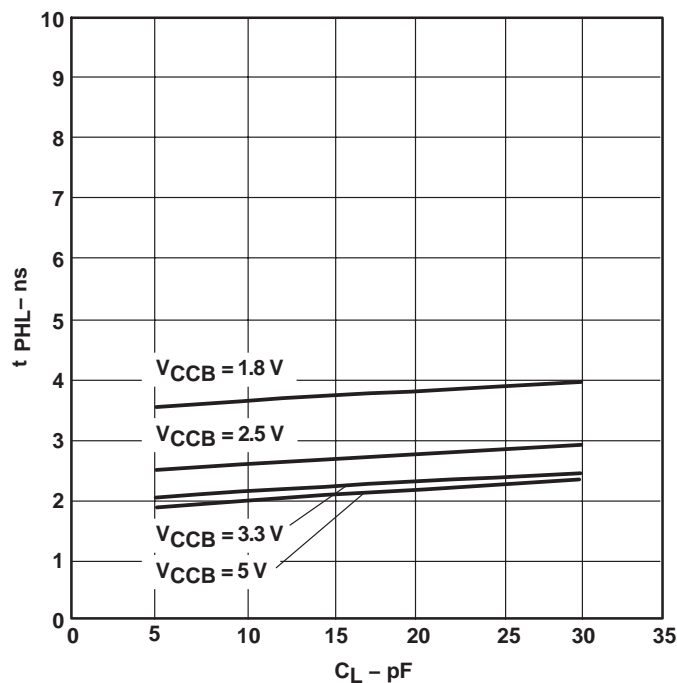
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TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$



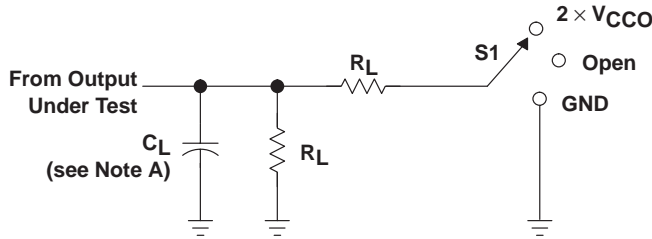
TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$



SN74LVC1T45 SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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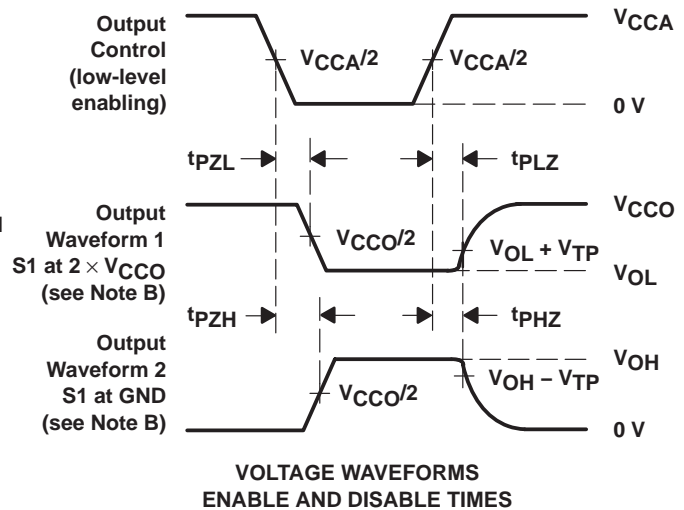
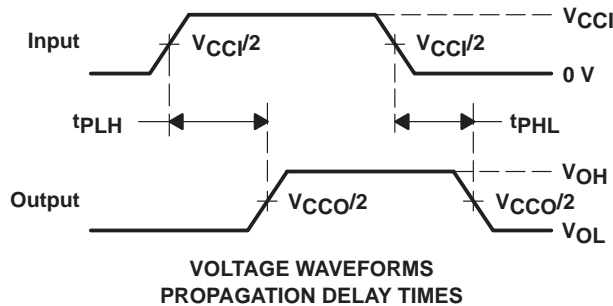
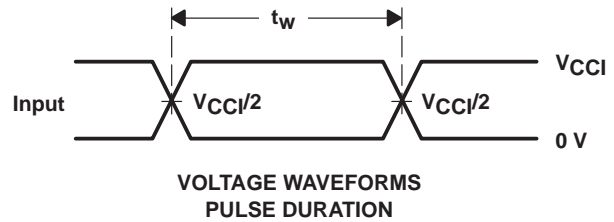
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
$1.8 \text{ V} \pm 0.15 \text{ V}$	15 pF	2 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	15 pF	2 k Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	15 pF	2 k Ω	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	15 pF	2 k Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $dv/dt \geq 1 \text{ V/ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CCI} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.
 - All parameters and waveforms are not applicable to all devices.

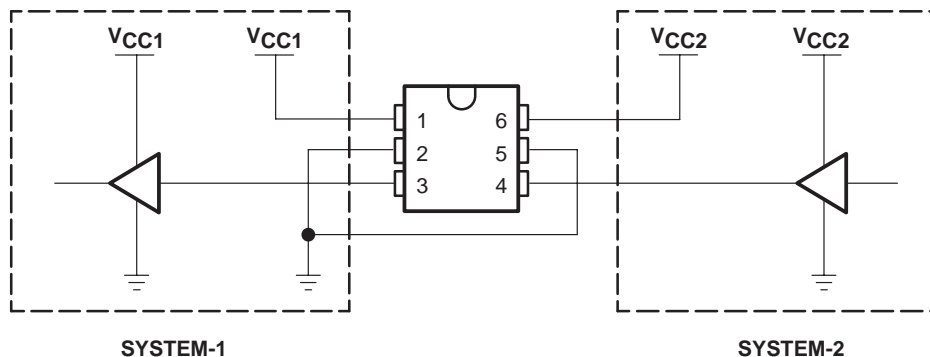
Figure 2. Load Circuit and Voltage Waveforms

SN74LVC1T45
SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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APPLICATION INFORMATION

The following circuit is an example of the SN74LVC1T45 being used in a unidirectional logic level-shifting application.



PIN	NAME	FUNCTION	DESCRIPTION
1	V _{CCA}	V _{CC1}	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V _{CC1} voltage.
4	B	IN	Input threshold value depends on V _{CC2} voltage.
5	DIR	DIR	The GND (low level) determines B port to A port direction.
6	V _{CCB}	V _{CC2}	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

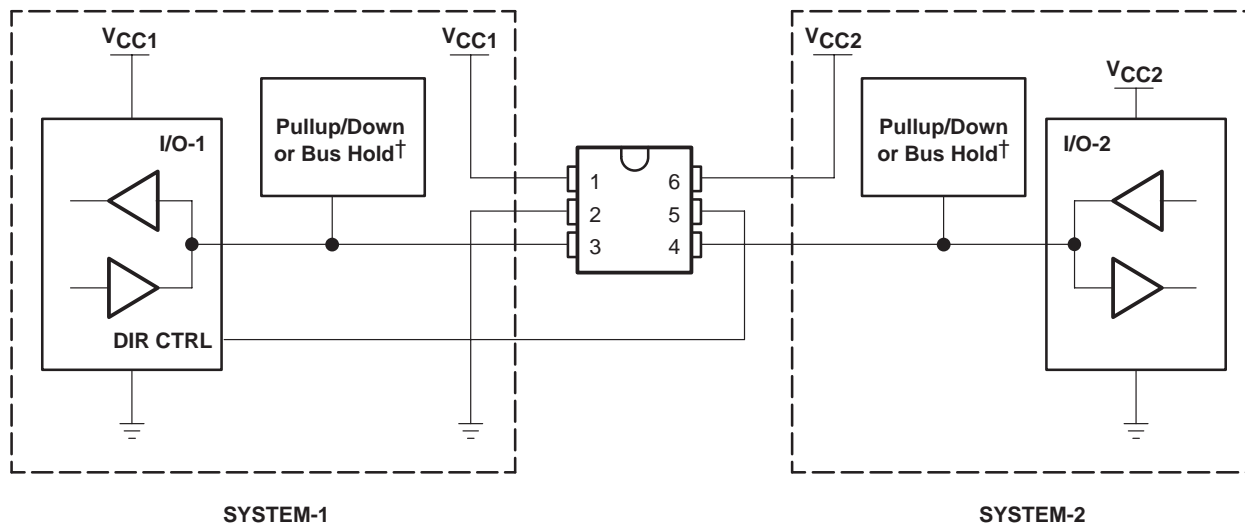
Figure 3. Unidirectional Logic Level-Shifting Application

SN74LVC1T45 SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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APPLICATION INFORMATION

Figure 4 shows the SN74LVC1T45 being used in a bidirectional logic level-shifting application. Since the SN74LVC1T45 does not have an output enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



Following is a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O 1	I/O 2	DESCRIPTION
1	H	OUT	IN	SYSTEM-1 data to SYSTEM-2
2	H	HI-Z	HI-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.†
3	L	HI-Z	HI-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.†
4	L	OUT	IN	SYSTEM-2 data to SYSTEM-1

† SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

Figure 4. Bidirectional Logic Level-Shifting Application

enable times

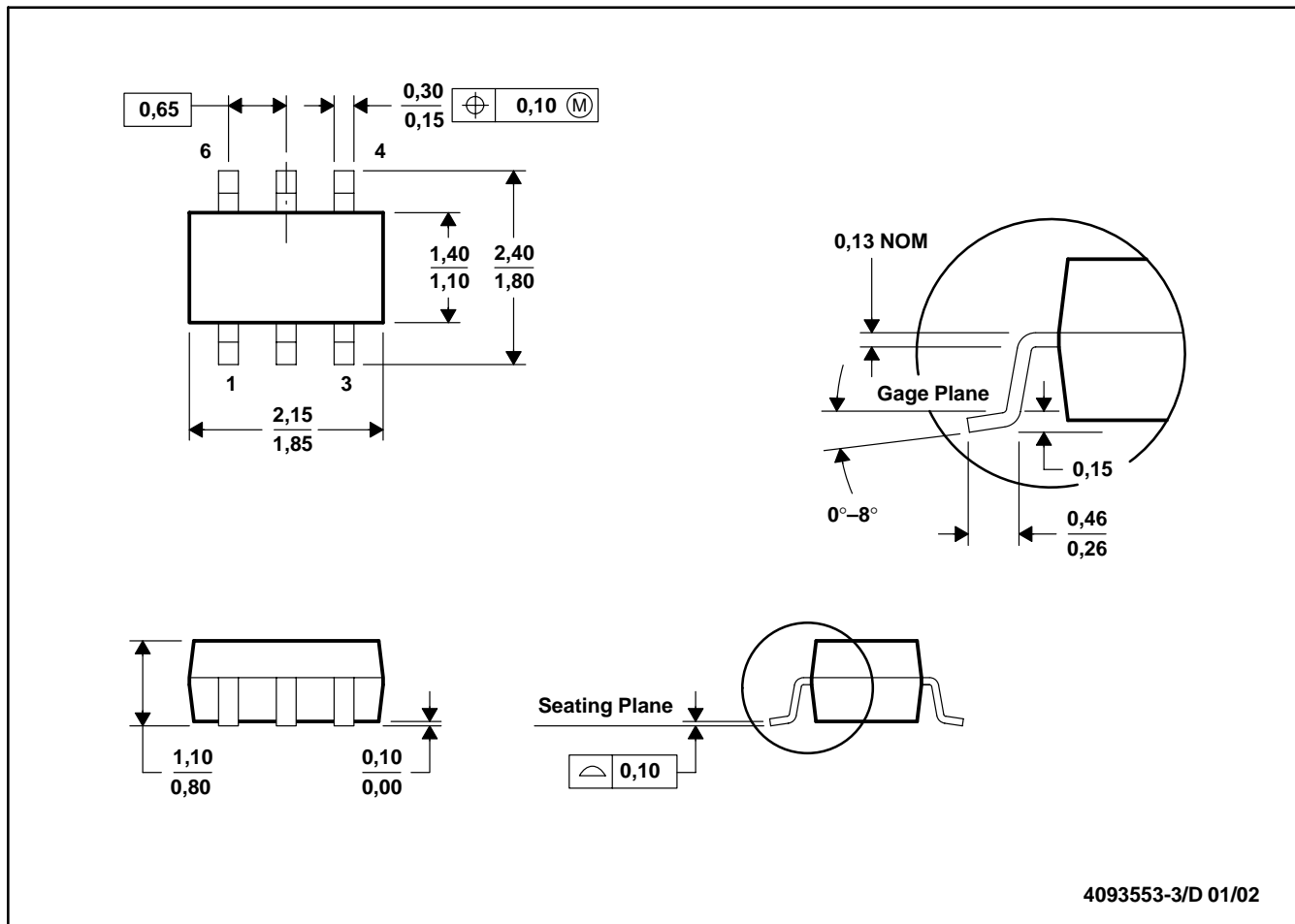
Calculate the enable times for the SN74LVC1T45 using the following formulas:

- $t_{PZH}(\text{DIR to A}) = t_{PLZ}(\text{DIR to B}) + t_{PLH}(\text{B to A})$
- $t_{PZL}(\text{DIR to A}) = t_{PHZ}(\text{DIR to B}) + t_{PHL}(\text{B to A})$
- $t_{PZH}(\text{DIR to B}) = t_{PLZ}(\text{DIR to A}) + t_{PLH}(\text{A to B})$
- $t_{PZL}(\text{DIR to B}) = t_{PHZ}(\text{DIR to A}) + t_{PHL}(\text{A to B})$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

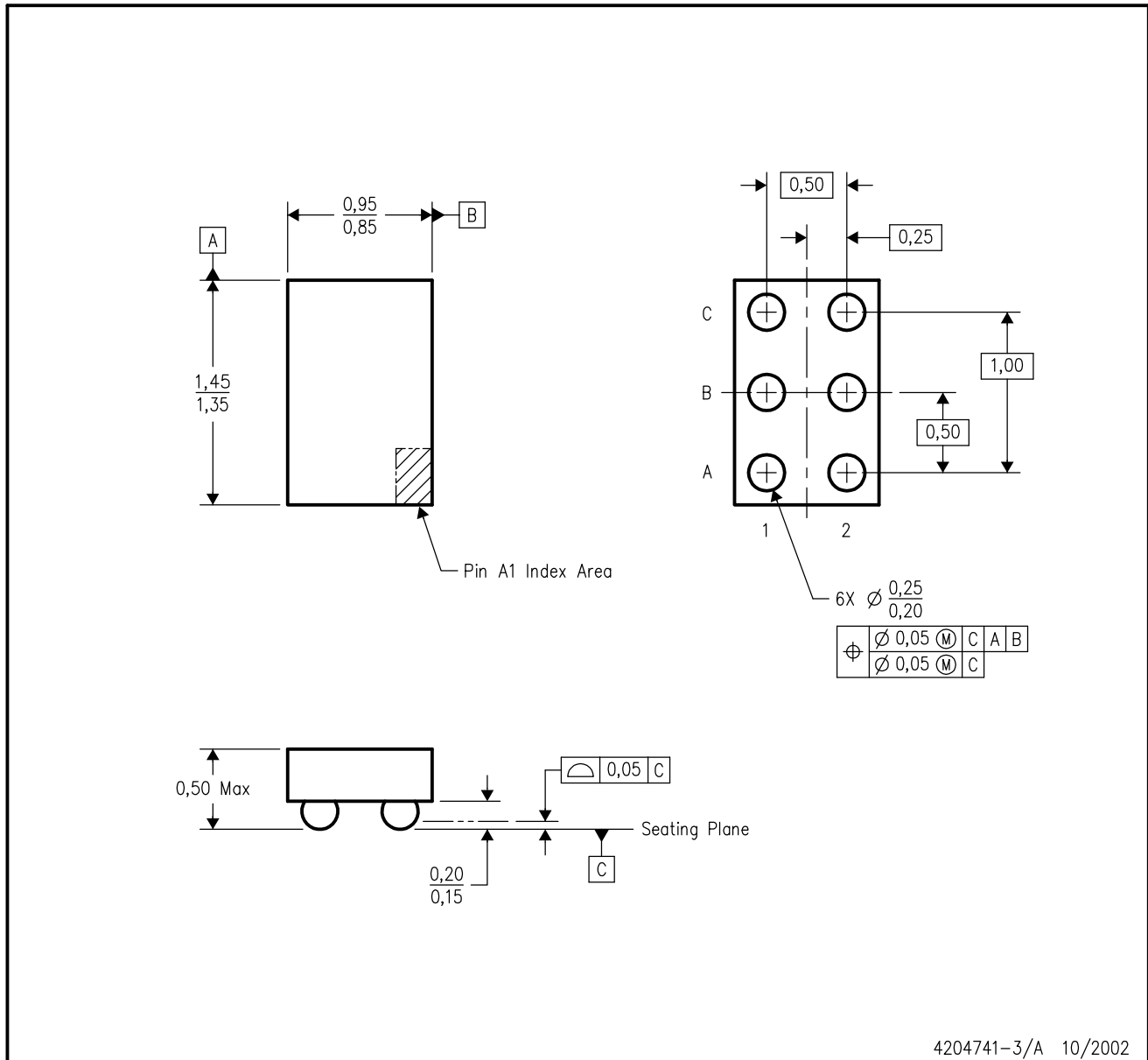


4093553-3/D 01/02

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-203

YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY

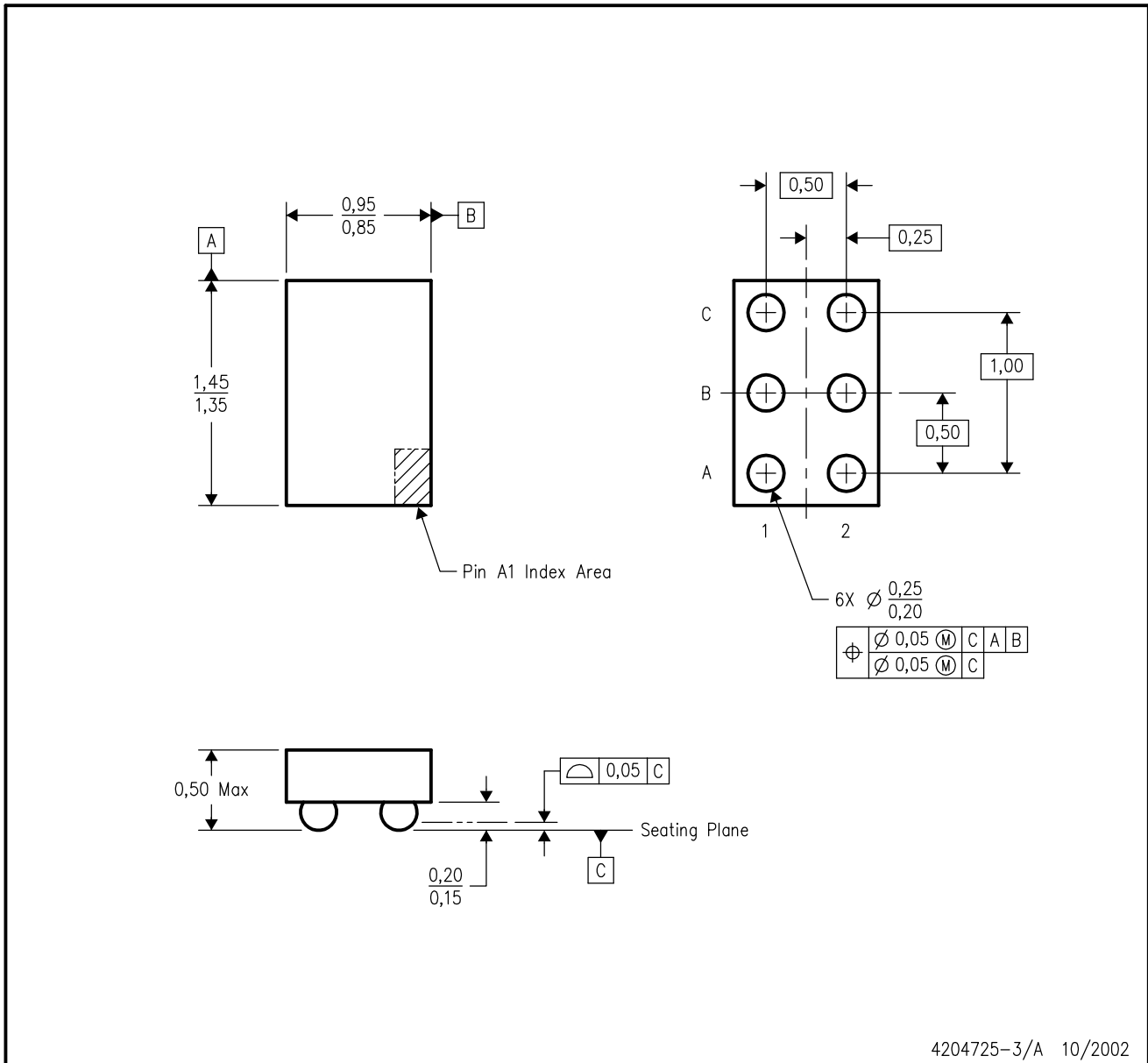


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4204725-3/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead-free.

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