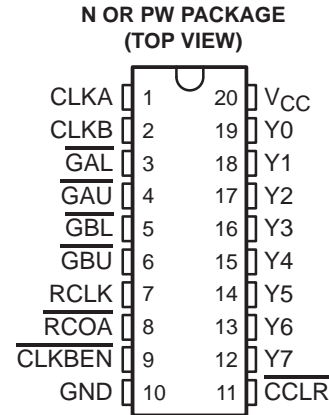


# SN74LV8154 DUAL 16-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS589 – AUGUST 2004

- Can Be Used as Two 16-Bit Counters or a Single 32-Bit Counter
- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 25 ns at 5 V (RCLK to Y)
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.7 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >4.4 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



## description/ordering information

The SN74LV8154 is a dual 16-bit binary counter with 3-state output registers, designed for 2-V to 5.5-V  $V_{CC}$  operation.

This 16-bit counter (A or B) feeds a 16-bit storage register, and each storage register is further divided into an upper byte and lower byte. The  $\overline{\text{GAL}}$ ,  $\overline{\text{GAU}}$ ,  $\overline{\text{GBL}}$ ,  $\overline{\text{GBU}}$  inputs are used to select the byte that needs to be output at Y0–Y7. CLKA is the clock for A counter, and CLKB is the clock for B counter. RCLK is the clock for the A and B storage registers. All three clock signals are positive-edge triggered.

A 32-bit counter can be realized by connecting CLKA and CLKB together and by connecting  $\overline{\text{RCOA}}$  to  $\overline{\text{CLKBEN}}$ .

To ensure the high-impedance state during power up or power down,  $\overline{\text{GAL}}$ ,  $\overline{\text{GAU}}$ ,  $\overline{\text{GBL}}$ , and  $\overline{\text{GBU}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74LV8154N	SN74LV8154N
	TSSOP – PW	Tube	SN74LV8154PW	LV8154
		Tape and reel	SN74LV8154PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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# SN74LV8154 DUAL 16-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

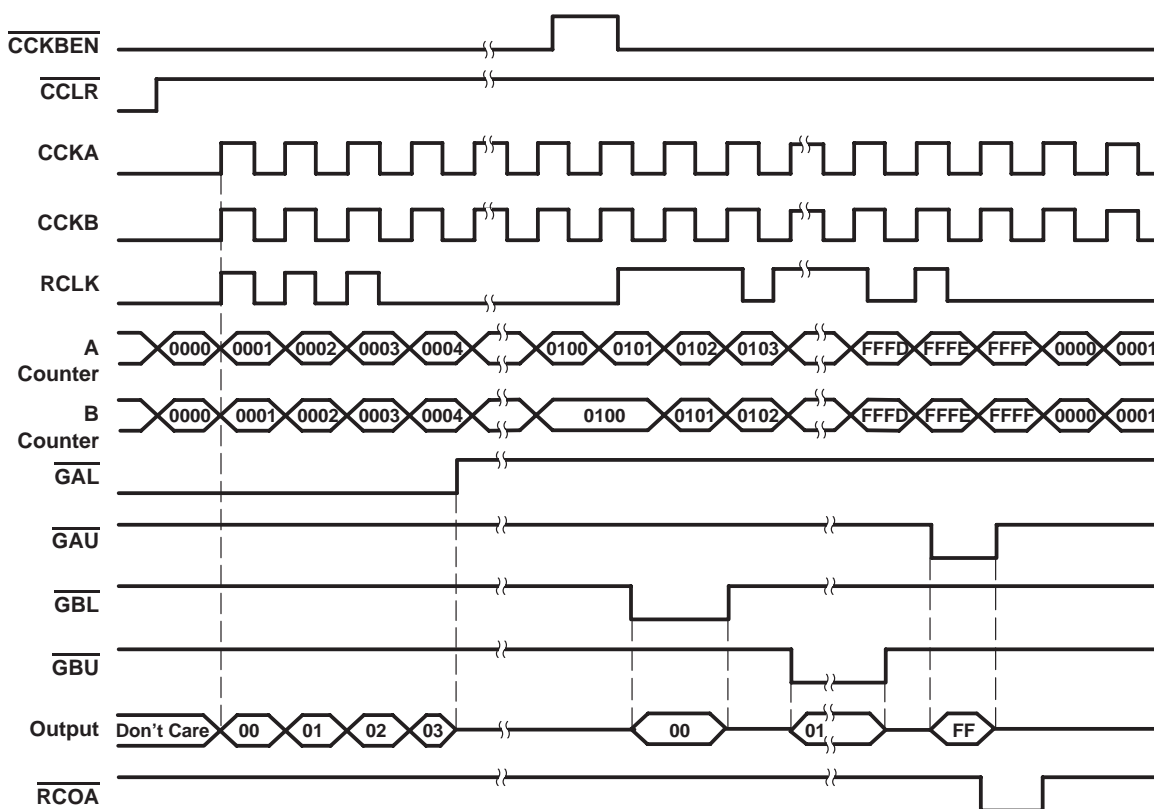
SCLS589 – AUGUST 2004

FUNCTION TABLE  
(each buffer)

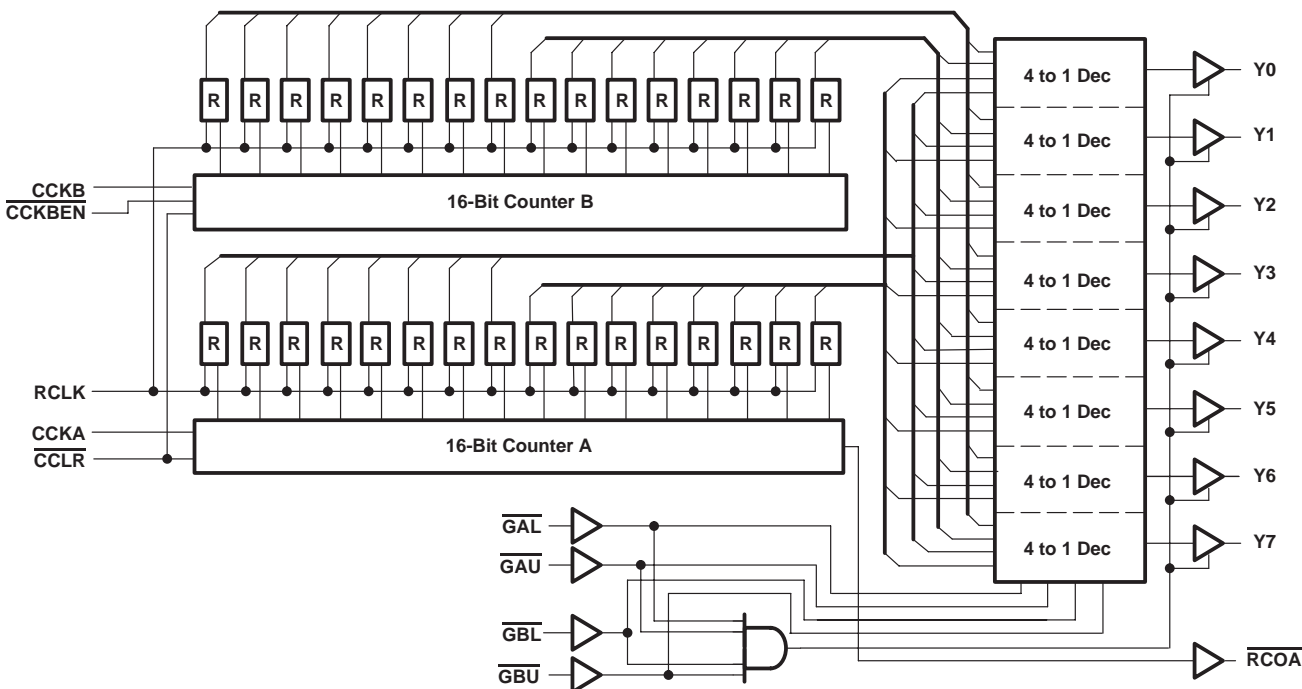
INPUTS				OUTPUT Y <sub>n</sub>
$\overline{\text{GAL}}$	$\overline{\text{GAU}}$	$\overline{\text{GBL}}$	$\overline{\text{GBU}}$	
L	H	H	H	Lower byte in A register
H	L	H	H	Upper byte in A register
H	H	L	H	Lower byte in B register
H	H	H	L	Upper byte in B register
H	H	H	H	Z

Combinations of  $\overline{\text{GAL}}$ ,  $\overline{\text{GAU}}$ ,  $\overline{\text{GBL}}$ ,  $\overline{\text{GBU}}$ , other than those shown above, are prohibited. If more than one input is L at the same time, the output data (Y0–Y7) may be invalid.

## timing diagram



**block diagram**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): N package .....	69°C/W
..... PW package .....	83°C/W
Storage temperature range, $T_{Stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

**SN74LV8154**  
**DUAL 16-BIT BINARY COUNTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

SCLS589 – AUGUST 2004

**recommended operating conditions (see Note 4)**

		V <sub>CC</sub>	MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage		2	5.5	V	
V <sub>IH</sub>	High-level input voltage	2 V	1.5		V	
		3 V to 3.6 V	V <sub>CC</sub> × 0.7			
		4.5 V to 5.5 V	V <sub>CC</sub> × 0.7			
V <sub>IL</sub>	Low-level input voltage	2 V	0.5		V	
		3 V to 3.6 V	V <sub>CC</sub> × 0.3			
		4.5 V to 5.5 V	V <sub>CC</sub> × 0.3			
V <sub>I</sub>	Input voltage		0	5.5	V	
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V	
		3-state	0	5.5		
I <sub>OH</sub>	High-level output current	Y <sub>n</sub> outputs	2 V	-50		μA
			3 V to 3.6 V	-6		mA
			4.5 V to 5.5 V	-12		
	RCOA		2 V	-50		μA
			3 V to 3.6 V	-6		mA
			4.5 V to 5.5 V	-12		
I <sub>OL</sub>	Low-level output current	Y <sub>n</sub> outputs	2 V	50		μA
			3 V to 3.6 V	6		mA
			4.5 V to 5.5 V	12		
	RCOA		2 V	50		μA
			3 V to 3.6 V	6		mA
			4.5 V to 5.5 V	12		
Δt/Δv	Input transition rise or fall rate	3 V to 3.6 V	100		ns/V	
		4.5 V to 5.5 V	20			
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN74LV8154**  
**DUAL 16-BIT BINARY COUNTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

SCLS589 – AUGUST 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	Y <sub>n</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9			V
		I <sub>OH</sub> = -6 mA	3 V	2.48			
		I <sub>OH</sub> = -12 mA	4.5 V	3.8			
	RCOA	I <sub>OH</sub> = -50 μA	2 V	1.9			
		I <sub>OH</sub> = -6 mA	3 V	2.48			
		I <sub>OH</sub> = -12 mA	4.5 V	3.8			
V <sub>OL</sub>	Y <sub>n</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	V
		I <sub>OL</sub> = 6 mA	3 V			0.44	
		I <sub>OL</sub> = 12 mA	4.5 V			0.55	
	RCOA	I <sub>OL</sub> = 50 μA	2 V			0.1	
		I <sub>OL</sub> = 6 mA	3 V			0.44	
		I <sub>OL</sub> = 12 mA	4.5 V			0.55	
I <sub>I</sub>		V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1	μA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			5	μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3		pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		5		pF

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t <sub>w</sub>	Pulse duration	CLKA, CLKB, RCLK high or low	10		ns
		CCLR low	22		
t <sub>su</sub>	Setup time	CLKBEN low before CLKB↑	13		ns
		CCLR high (inactive) before CLKA↑ or CLKB↑	13		
		CLKA↑ or CLKB↑ before RCLK↑	13		
		RCLK↑ before GAL or GAU or GBL or GBU low	13		
		GAL or GAU or GBL or GBU high (inactive) before RCLK↑	13		
t <sub>h</sub>	Hold time	CLKBEN low after CLKB↑	0		ns
		CLKA or CLKB after RCLK	0		
t <sub>z</sub> <sup>†</sup>	Z-period	GAL, GAU, GBL, GBU all high before one of them switches low	200		ns

<sup>†</sup> t<sub>z</sub> condition: C<sub>L</sub> = 50 pF, R<sub>L</sub> = 1 kΩ



# SN74LV8154 DUAL 16-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS589 – AUGUST 2004

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

		MIN	MAX	UNIT
$t_w$	Pulse duration	CLKA, CLKB, RCLK high or low	10	ns
		$\overline{\text{CCLR}}$ low	20	
$t_{su}$	Setup time	$\overline{\text{CLKBEN}}$ low before $\text{CLKB}\uparrow$	10	ns
		$\overline{\text{CCLR}}$ high (inactive) before $\text{CLKA}\uparrow$ or $\text{CLKB}\uparrow$	10	
		$\text{CLKA}\uparrow$ or $\text{CLKB}\uparrow$ before $\text{RCLK}\uparrow$	10	
		$\text{RCLK}\uparrow$ before $\overline{\text{GAL}}$ or $\overline{\text{GAU}}$ or $\overline{\text{GBL}}$ or $\overline{\text{GBU}}$ low	10	
$t_h$	Hold time	$\overline{\text{CLKBEN}}$ low after $\text{CLKB}\uparrow$	0	ns
		CLKA or CLKB after RCLK	0	
$t_z^\dagger$	Z-period	$\overline{\text{GAL}}$ , $\overline{\text{GAU}}$ , $\overline{\text{GBL}}$ , $\overline{\text{GBU}}$ all high before one of them switches low	200	ns

$^\dagger t_z$  condition:  $C_L = 50\text{ pF}$ ,  $R_L = 1\text{ k}\Omega$

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{MAX}$			$C_L = 15\text{ pF}$				40		MHz
			$C_L = 50\text{ pF}$				25		
$t_{pd}$	RCLK	Y	$C_L = 15\text{ pF}$				22	1 38	ns
	CLKA	$\overline{\text{RCOA}}$					26	1 44	
$t_{PLH}$	$\overline{\text{CCLR}}$	$\overline{\text{RCOA}}$					18	1 32	ns
$t_{en}$	$\overline{\text{GAL}}$ , $\overline{\text{GAU}}$ , $\overline{\text{GBL}}$ , $\overline{\text{GBU}}$	Y					27	1 46	ns
$t_{dis}$	$\overline{\text{GAL}}$ , $\overline{\text{GAU}}$ , $\overline{\text{GBL}}$ , $\overline{\text{GBU}}$	Y					12	1 21	ns
$t_{pd}$	RCLK	Y		$C_L = 50\text{ pF}$				25	1 42
	CLKA	$\overline{\text{RCOA}}$				28	1 46		
$t_{PLH}$	$\overline{\text{CCLR}}$	$\overline{\text{RCOA}}$				20	1 35	ns	
$t_{en}$	$\overline{\text{GAL}}$ , $\overline{\text{GAU}}$ , $\overline{\text{GBL}}$ , $\overline{\text{GBU}}$	Y				30	1 50	ns	
$t_{dis}$	$\overline{\text{GAL}}$ , $\overline{\text{GAU}}$ , $\overline{\text{GBL}}$ , $\overline{\text{GBU}}$	Y				14	1 24	ns	



**SN74LV8154**  
**DUAL 16-BIT BINARY COUNTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

SCLS589 – AUGUST 2004

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT	
				MIN	TYP	MAX				
$f_{\text{MAX}}$			$C_L = 15\text{ pF}$				40		MHz	
			$C_L = 50\text{ pF}$				25			
$t_{\text{pd}}$	RCLK	Y	$C_L = 15\text{ pF}$	14			1	25	ns	
	CLKA	$\overline{\text{RCOA}}$		16			1	27		
$t_{\text{PLH}}$	$\overline{\text{CCLR}}$	$\overline{\text{RCOA}}$		12			1	20	ns	
$t_{\text{en}}$	$\overline{\text{GAL}}, \overline{\text{GAU}}, \overline{\text{GBL}}, \overline{\text{GBU}}$	Y		16			1	28	ns	
$t_{\text{dis}}$	$\overline{\text{GAL}}, \overline{\text{GAU}}, \overline{\text{GBL}}, \overline{\text{GBU}}$	Y		8			1	15	ns	
$t_{\text{pd}}$	RCLK	Y		$C_L = 50\text{ pF}$	16			1	27	ns
	CLKA	$\overline{\text{RCOA}}$			17			1	28	
$t_{\text{PLH}}$	$\overline{\text{CCLR}}$	$\overline{\text{RCOA}}$			13			1	21	ns
$t_{\text{en}}$	$\overline{\text{GAL}}, \overline{\text{GAU}}, \overline{\text{GBL}}, \overline{\text{GBU}}$	Y			18			1	30	ns
$t_{\text{dis}}$	$\overline{\text{GAL}}, \overline{\text{GAU}}, \overline{\text{GBL}}, \overline{\text{GBU}}$	Y			9			1	16	ns

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$

PARAMETER		$T_A = 25^\circ\text{C}$			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic $V_{\text{OL}}$	0.7			V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic $V_{\text{OL}}$	-0.75			V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic $V_{\text{OH}}$	4.4			V

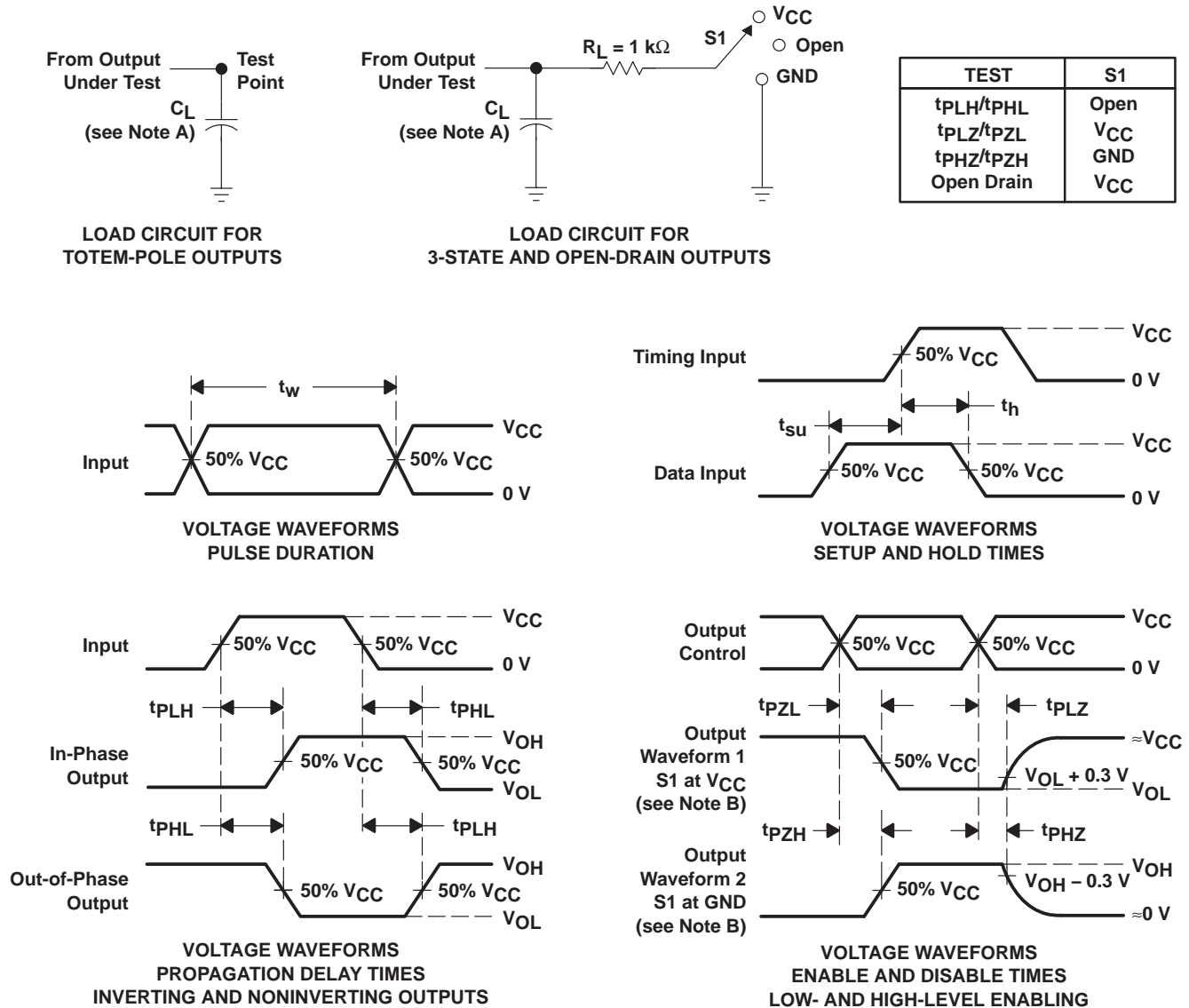
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = \text{No load}$ , $\text{CCLK} = 10\text{ MHz}$ , $\text{RCLK} = 1\text{ MHz}$	56	pF

# SN74LV8154 DUAL 16-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS589 – AUGUST 2004

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV8154N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV8154NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV8154PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8154PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8154PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8154PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8154PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8154PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

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