

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645 OCTAL BUS TRANSCEIVERS

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- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

| DEVICE | OUTPUT | LOGIC |
|--------|----------------|--------------------|
| 'LS640 | 3-State | Inverting |
| 'LS641 | Open-Collector | True |
| 'LS642 | Open-Collector | Inverting |
| 'LS644 | Open-Collector | True and inverting |
| 'LS645 | 3-State | True |

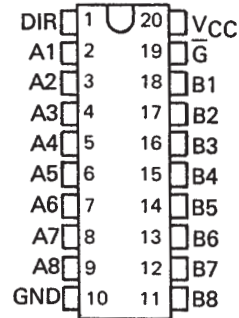
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so the buses are effectively isolated.

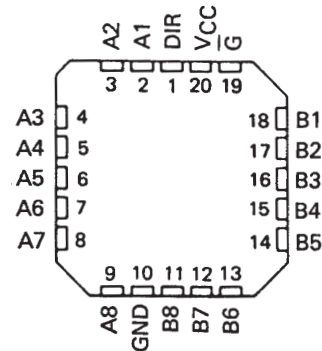
The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C .

SN54LS' . . . J PACKAGE
SN74LS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS' . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

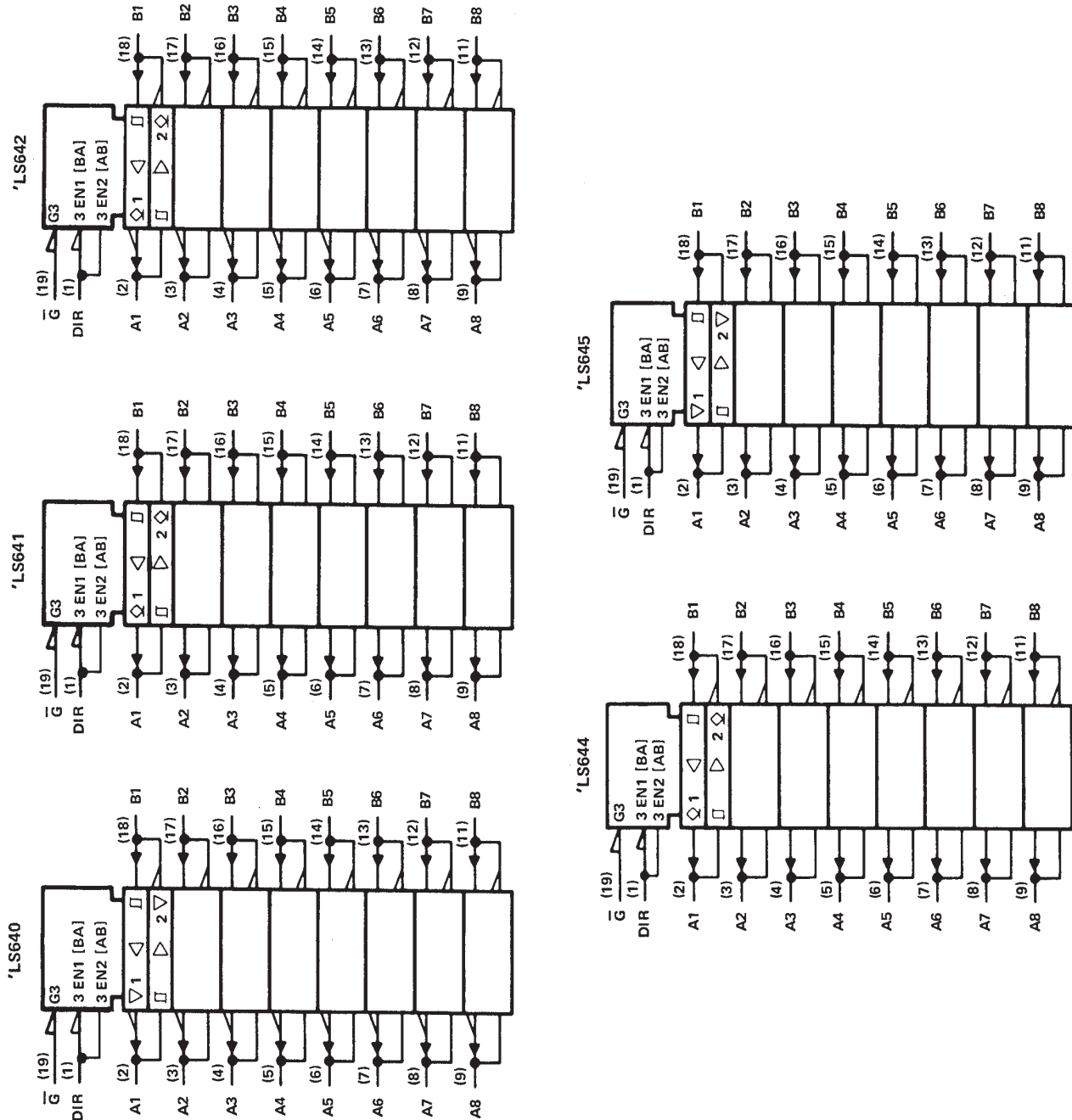
| CONTROL INPUTS | | OPERATION | | |
|----------------|-----|------------------|------------------|-------------------------|
| \bar{G} | DIR | 'LS640 'LS642 | 'LS641 'LS645 | 'LS644 |
| L | L | B data to A bus | B data to A bus | B data to A bus |
| L | H | A data to B bus | A data to B bus | \bar{A} data to B bus |
| H | X | Isolation | Isolation | Isolation |

H = high level, L = low level, X = irrelevant

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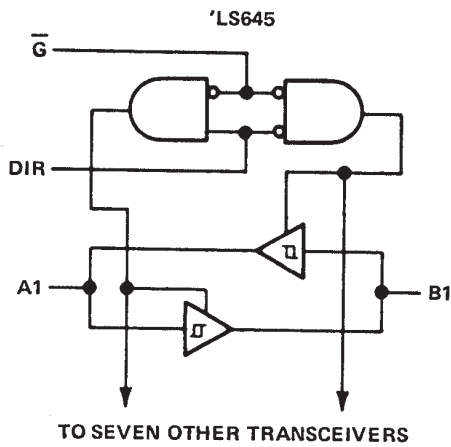
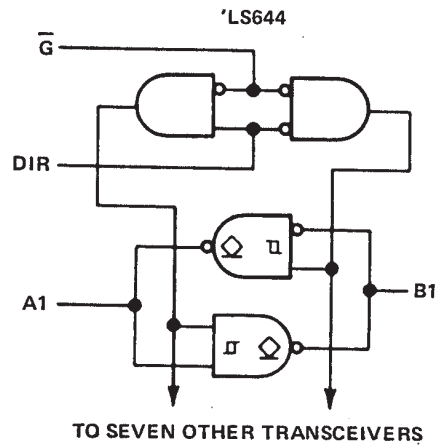
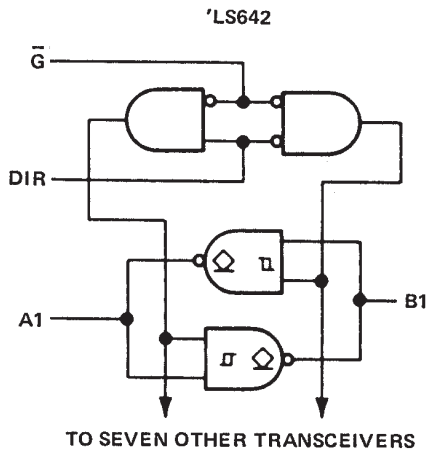
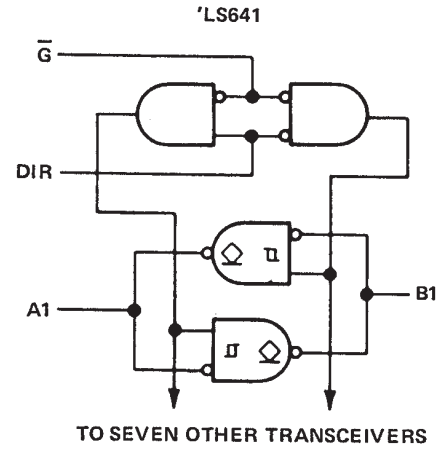
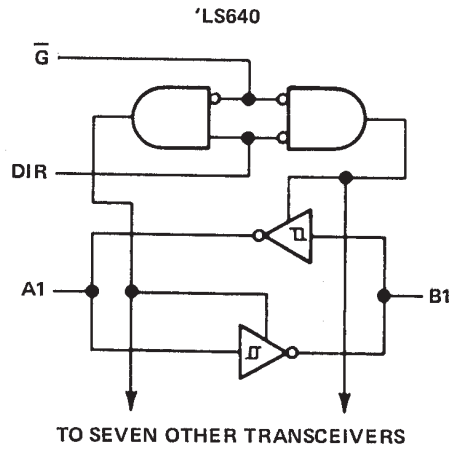
logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645
 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645
OCTAL BUS TRANSCEIVERS
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logic diagrams (positive logic)



SN54LS640, SN54LS645 SN74LS640, SN74LS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|------------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: All inputs | 7 V |
| I/O ports | 5.5 V |
| Operating free-air temperature range: SN54LS640, SN54LS645 | -55 °C to 125 °C |
| SN74LS640, SN74LS645 | 0 °C to 70 °C |
| Storage temperature range | -65 °C to 150 °C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| PARAMETER | SN54LS640 SN54LS645 | | | SN74LS640 SN74LS645 | | | UNIT |
|--------------------------------------|------------------------|-----|-----|------------------------|-----|-----------------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.5 | | | 0.6 | V |
| I_{OH} High-level output current | | | -12 | | | -15 | mA |
| I_{OL} Low-level output current | | | 12 | | | 24 | mA |
| | | | | | | 48 [†] | |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

[†]The 48-mA limit applies for the SN74LS640-1 and SN74LS645-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS [†] | SN54LS640 SN54LS645 | | | SN74LS640 SN74LS645 | | | UNIT | |
|-------------------------------------|---|---|-----------------------|------|------------------------|------------------|------|------|----|
| | | MIN | TYP [§] | MAX | MIN | TYP [§] | MAX | | |
| V_{IK} | $V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$ | | | -1.5 | | | -1.5 | V | |
| Hysteresis ($V_{T+} - V_{T-}$) | $V_{CC} = \text{MIN}$, A or B input | 0.1 | 0.4 | | 0.2 | 0.4 | | V | |
| V_{OH} | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$ | $I_{OH} = -3 \text{ mA}$ | 2.4 | 3.4 | 2.4 | 3.4 | | | |
| | | $I_{OH} = \text{MAX}$ | 2 | | 2 | | | | |
| V_{OL} | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$ | $I_{OL} = 12 \text{ mA}$ | 0.25 | 0.4 | 0.25 | 0.4 | | V | |
| | | $I_{OL} = 24 \text{ mA}$ | | | 0.35 | 0.5 | | | |
| | | $I_{OL} = 48 \text{ mA}^{\#}$ | | | 0.4 | 0.5 | | | |
| I_{OZH} | $V_{CC} = \text{MAX}$, \bar{G} at 2 V, $V_O = 2.7 \text{ V}$ | | | 20 | | | 20 | μA | |
| I_{OZL} | $V_{CC} = \text{MAX}$, \bar{G} at 2 V, $V_O = 0.4 \text{ V}$ | | | -0.4 | | | -0.4 | mA | |
| I_I | A or B DIR or \bar{G} | $V_{CC} = \text{MAX}$ | $V_I = 5.5 \text{ V}$ | | 0.1 | | 0.1 | mA | |
| | | | $V_I = 7 \text{ V}$ | | 0.1 | | 0.1 | | |
| I_{IH} | $V_{CC} = \text{MAX}$, $V_{IH} = 2.7 \text{ V}$ | | | 20 | | | 20 | μA | |
| I_{IL} | $V_{CC} = \text{MAX}$, $V_{IL} = 0.4 \text{ V}$ | | | -0.4 | | | -0.4 | mA | |
| I_{OS}^{\ddagger} | $V_{CC} = \text{MAX}$ | -40 | | -225 | -40 | | -225 | mA | |
| I_{CC} | Outputs high | $V_{CC} = \text{MAX}$, Outputs open | | 48 | 70 | | 48 | 70 | mA |
| | Outputs low | | | 62 | 90 | | 62 | 90 | |
| | Outputs at Hi-Z | | | 64 | 95 | | 64 | 95 | |

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

[‡]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

[#]The 48-mA condition applies for the SN74LS640-1 and SN74LS645-1 only.



SN54LS640, SN54LS645
SN74LS640, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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switching characteristics, $V_{CC} = 5 V$, $T_A = 25^\circ C$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS640, 'LS640-1 | | | 'LS645, 'LS645-1 | | | UNIT |
|--|----------------|-------------|---|------------------|-----|-----|------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low-to-high-level output | A | B | $C_L = 45 \text{ pF}$, $R_L = 667 \Omega$, See Note 2 | | 6 | 10 | | 8 | 15 | ns |
| | B | A | | | 6 | 10 | | 8 | 15 | |
| t_{PHL} Propagation delay time, high-to-low-level output | A | B | | | 8 | 15 | | 11 | 15 | ns |
| | B | A | | | 8 | 15 | | 11 | 15 | |
| t_{PZL} Output enable time to low level | \overline{G} | A | | | 31 | 40 | | 31 | 40 | ns |
| | \overline{G} | B | | | 31 | 40 | | 31 | 40 | |
| t_{PZH} Output enable time to high level | \overline{G} | A | | | 23 | 40 | | 26 | 40 | ns |
| | \overline{G} | B | | | 23 | 40 | | 26 | 40 | |
| t_{PLZ} Output disable time from low level | \overline{G} | A | $C_L = 5 \text{ pF}$, $R_L = 667 \Omega$, See Note 2 | | 15 | 25 | | 15 | 25 | ns |
| | \overline{G} | B | | | 15 | 25 | | 15 | 25 | |
| t_{PHZ} Output disable time from high level | \overline{G} | A | | | 15 | 25 | | 15 | 25 | ns |
| | \overline{G} | B | | | 15 | 25 | | 15 | 25 | |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



TYPICAL CHARACTERISTICS

SN54LS'
 INVERTING OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE

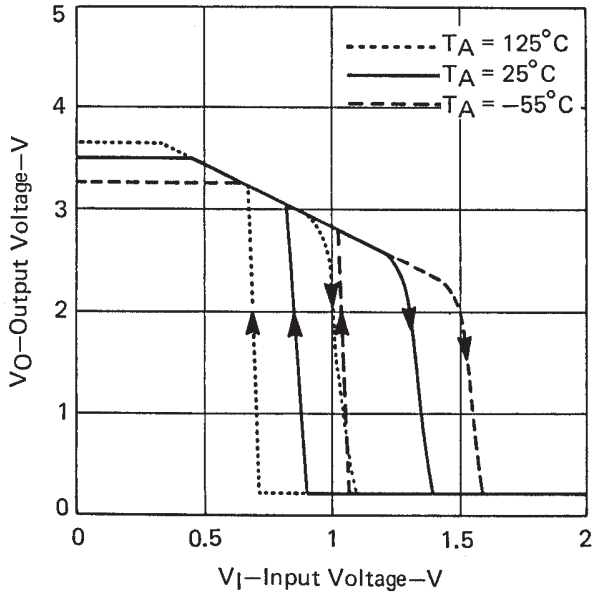


FIGURE 1

SN74LS'
 INVERTING OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE



FIGURE 2

SN54LS'
 NONINVERTING OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE

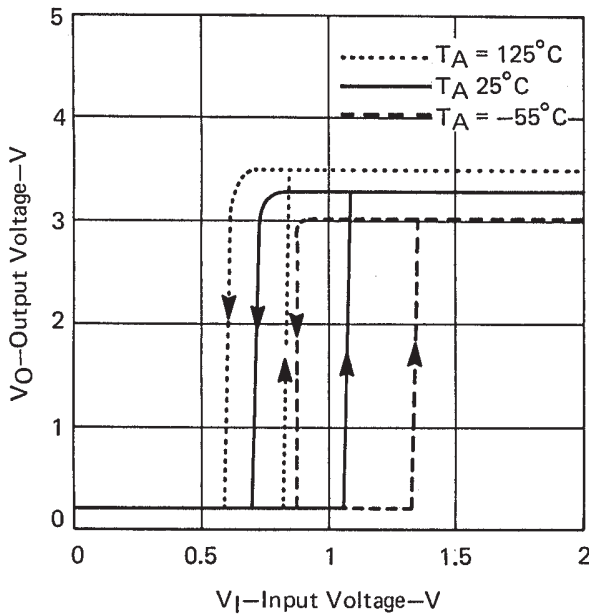


FIGURE 3

SN74LS'
 NONINVERTING OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE



FIGURE 4

SN54LS641, SN54LS642, SN54LS644
SN74LS641, SN74LS642, SN74LS644
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|-------------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: All inputs and I/O ports | 7 V |
| Operating free-air temperature range: SN54LS641, SN54LS642, SN54LS644 | – 55° C to 125° C |
| SN74LS641, SN74LS642, SN74LS644 | 0° C to 70° C |
| Storage temperature range | – 65° C to 150° C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| PARAMETER | SN54LS641 SN54LS642 SN54LS644 | | | SN74LS641 SN74LS642 SN74LS644 | | | UNIT |
|--------------------------------------|-------------------------------------|-----|-----|-------------------------------------|------|-----|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| | V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | 0.5 | | | 0.6 | | | V |
| V_{OH} High-level output voltage | 5.5 | | | 5.5 | | | V |
| I_{OL} Low-level output current | 12 | | | 24 | | | mA |
| | | | | 48 § | | | |
| T_A Operating free-air temperature | – 55 125 | | | 0 70 | | | °C |

§ The 48 mA limit applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS † | SN54LS641 SN54LS642 SN54LS644 | | | SN74LS641 SN74LS642 SN74LS644 | | | UNIT |
|-------------------------------------|--|--|---|-------|-------------------------------------|-------|-------|---------------|
| | | MIN | TYP ‡ | MAX | MIN | TYP ‡ | MAX | |
| | | V_{IK} | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | – 1.5 | | | – 1.5 | |
| Hysteresis ($V_{T+} - V_{T-}$) | $V_{CC} = \text{MIN}, A \text{ or } B \text{ input}$ | 0.1 | 0.4 | | 0.2 | 0.4 | | V |
| I_{OH} | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$ | 0.1 | | | 0.1 | | | mA |
| V_{OL} | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$ | $I_{OL} = 12 \text{ mA}$ | | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | $I_{OL} = 24 \text{ mA}$ | | | | 0.35 | 0.5 | |
| | | $I_{OL} = 48 \text{ mA} §$ | | | | 0.4 | 0.5 | |
| I_I | A or B | $V_{CC} = \text{MAX}$ | $V_I = 5.5 \text{ V}$ | | 0.1 | | 0.1 | mA |
| | DIR or \bar{G} | | $V_I = 7 \text{ V}$ | | 0.1 | | 0.1 | |
| I_{IH} | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | 20 | | | 20 | | | μA |
| I_{IL} | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | – 0.4 | | | – 0.4 | | | mA |
| I_{CC} | Outputs high | $V_{CC} = \text{MAX},$ Outputs open | 48 | 70 | 48 | 70 | mA | |
| | Outputs low | | 62 | 90 | 62 | 90 | | |
| | Outputs at Hi-Z | | 64 | 95 | 64 | 95 | | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ The 48 mA condition applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.



SN54LS641, SN54LS642, SN54LS644
 SN74LS641, SN74LS642, SN74LS644
 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

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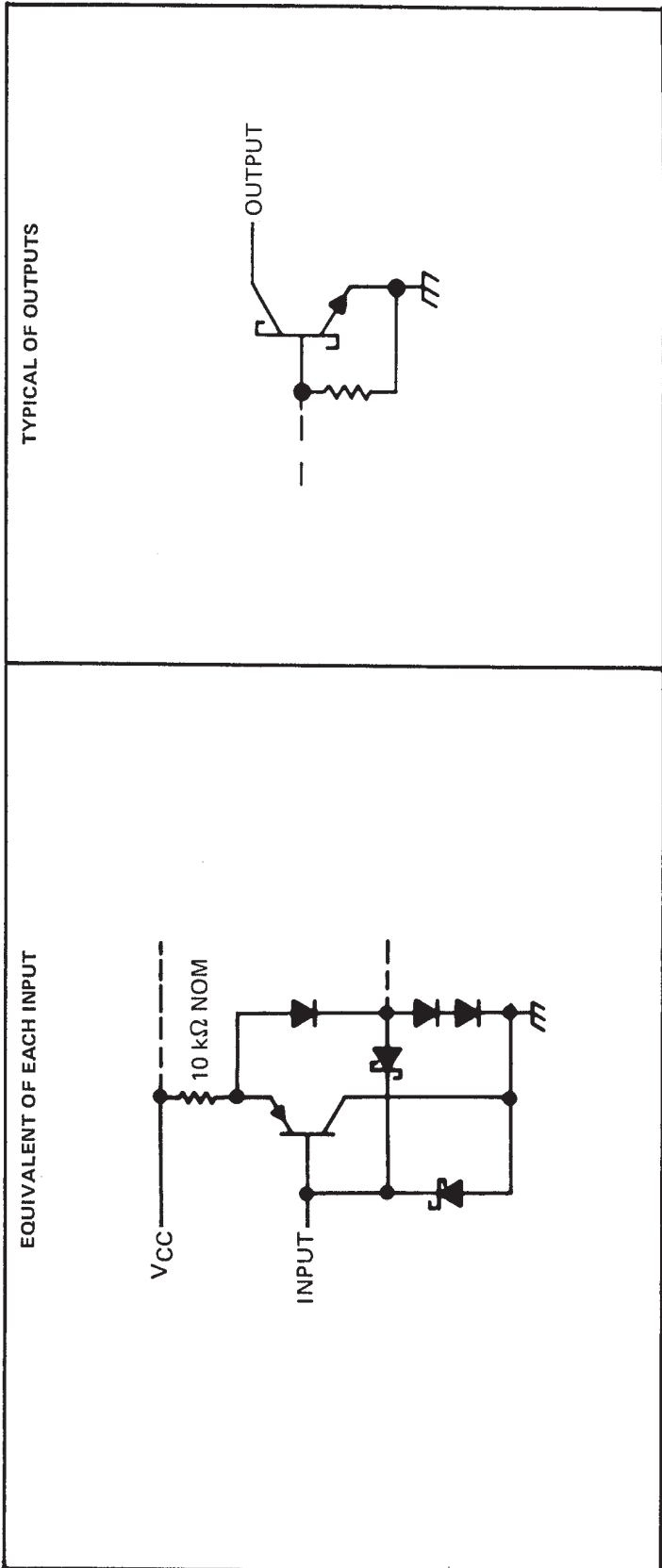
switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'LS641, 'LS641-1 | | 'LS642, 'LS642-1 | | 'LS644, 'LS644-1 | | UNIT |
|---|-----------------|-------------|------------------|-----|------------------|-----|------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t _{PLH} Propagation delay time, low-to-high-level output | A | B | 17 | 25 | 19 | 25 | 17 | 25 | ns |
| | B | A | 17 | 25 | 19 | 25 | 19 | 25 | |
| t _{PHL} Propagation delay time, high-to-low-level output | A | B | 16 | 25 | 14 | 25 | 14 | 25 | ns |
| | B | A | 16 | 25 | 14 | 25 | 16 | 25 | |
| t _{PLH} Output disable time from low level | \bar{G} , DIR | A | 23 | 40 | 26 | 40 | 26 | 40 | ns |
| | \bar{G} , DIR | B | 25 | 40 | 28 | 40 | 25 | 40 | |
| t _{PHL} Output enable time from high level | \bar{G} , DIR | A | 34 | 50 | 43 | 60 | 43 | 60 | ns |
| | \bar{G} , DIR | B | 37 | 50 | 39 | 60 | 37 | 50 | |

TEST CONDITIONS
 $C_L = 45\text{ pF}$,
 $R_L = 667\ \Omega$,
 See Note 2

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-8416101VRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-8416101VSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |
| 84161012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 8416101RA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| 8416101SA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |
| SN54LS640J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54LS645J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74LS640-1DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640-1DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640-1DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640-1DWR | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI |
| SN74LS640-1N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS640-1NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS640-1NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640-1NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640-1NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS640N3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI |
| SN74LS640NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS640NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS640NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641-1DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| | | | | | | no Sb/Br) | | |
| SN74LS641-1DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641-1DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641-1DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641-1DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641-1DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641-1N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS641-1N3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI |
| SN74LS641-1NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS641DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS641N3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI |
| SN74LS641NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS641NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS641NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS642-1DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS642-1DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS642-1DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS642-1N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS642-1NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS642DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LS642DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS642DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS642N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS642NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS642NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS642NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS642NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS644-1N | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI |
| SN74LS644N | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI |
| SN74LS645-1DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645-1DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645-1DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645-1DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645-1DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645-1DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645-1N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS645-1N3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI |
| SN74LS645-1NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS645-1NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645-1NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645-1NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645DWR | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI |
| SN74LS645N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS645N3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI |
| SN74LS645NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LS645NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS645NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54LS640FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54LS640J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS640W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |
| SNJ54LS645FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54LS645J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LS645W | OBSOLETE | CFP | W | 20 | | TBD | Call TI | Call TI |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS640-1NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS640DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS640NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS641-1DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS641DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS641NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS642NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS645-1DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS645-1NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS645NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS640-1NSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS640DWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS640NSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS641-1DWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS641DWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS641NSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS642NSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS645-1DWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS645-1NSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LS645NSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

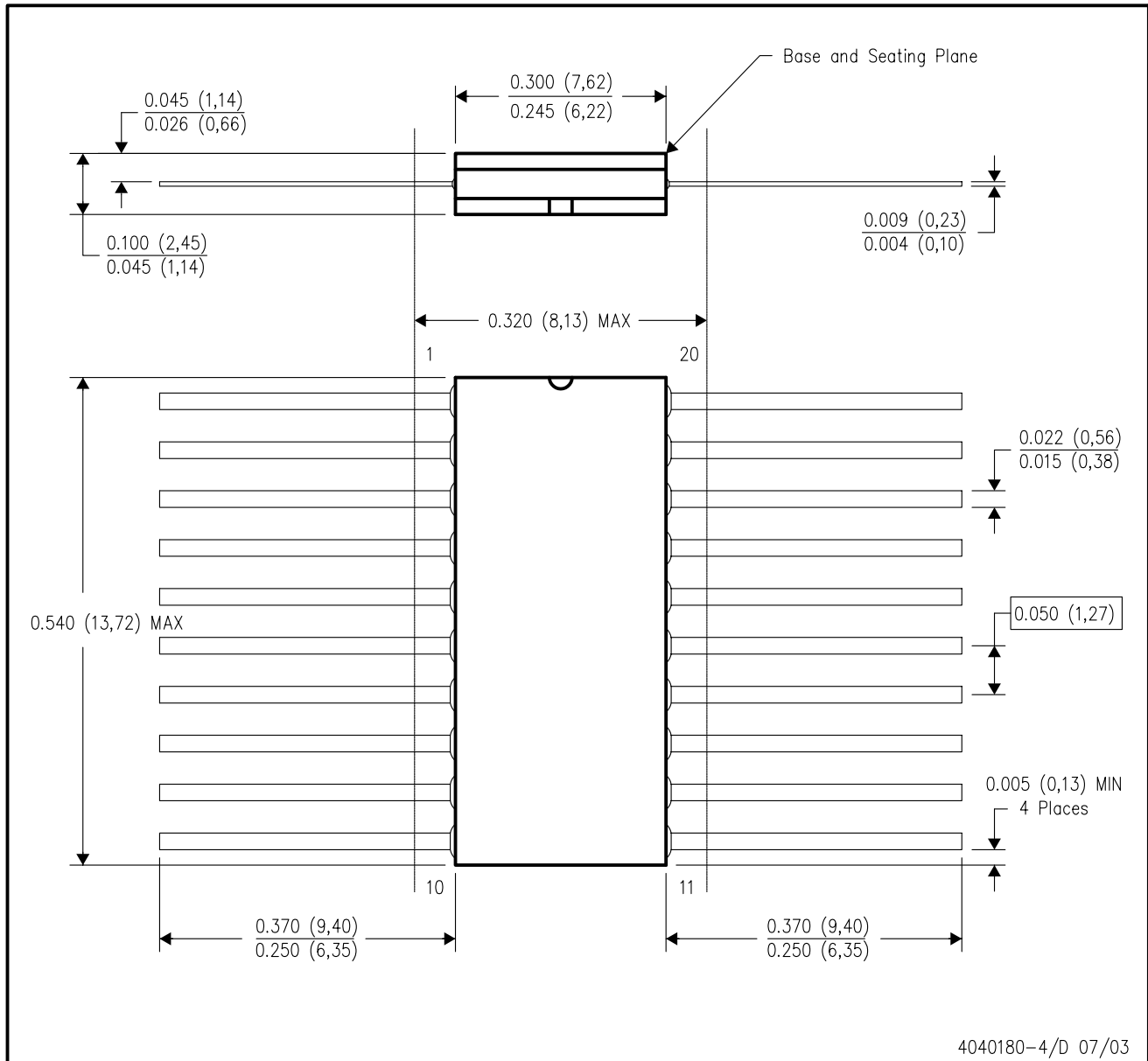


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

DW (R-PDSO-G20)

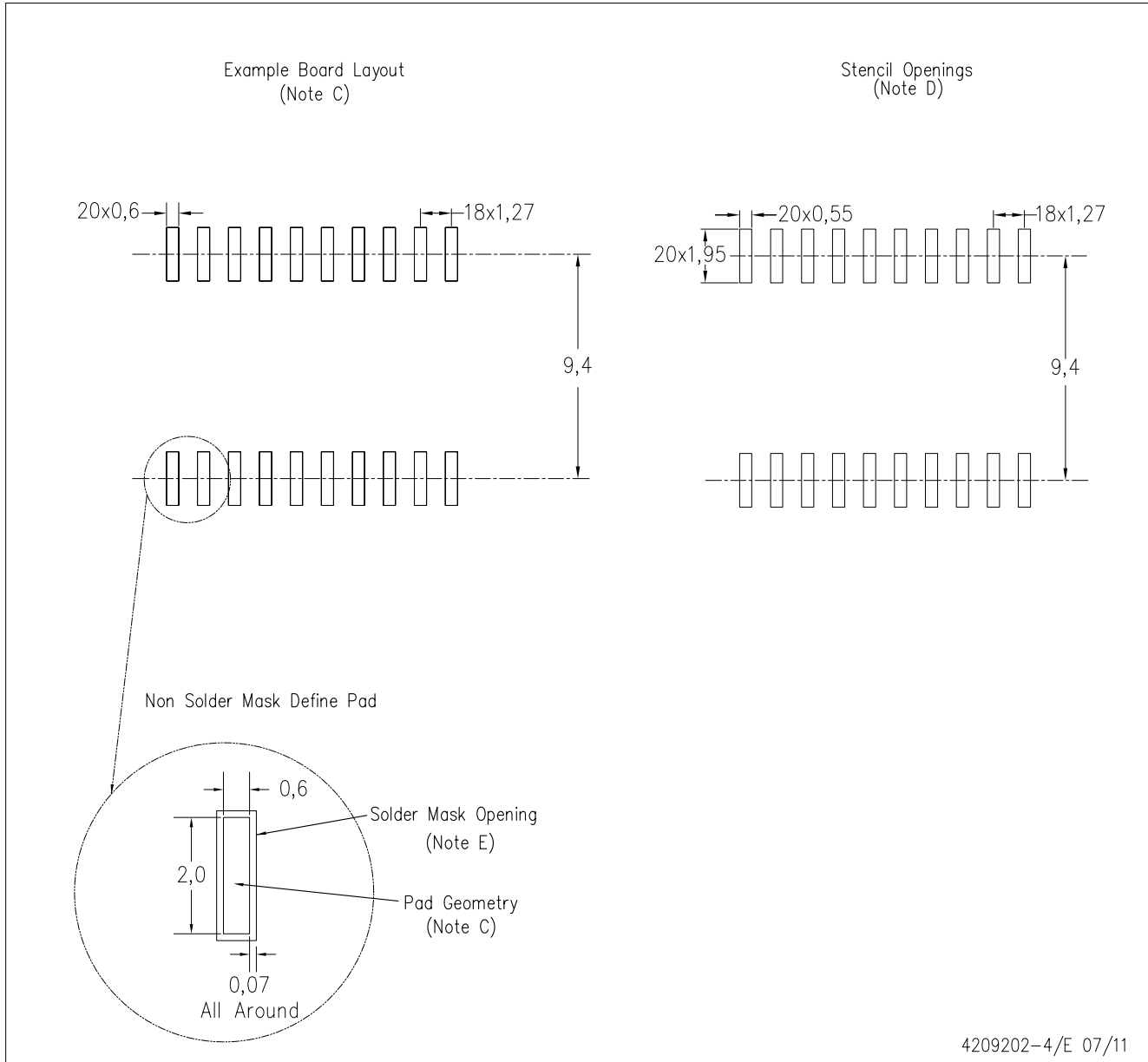
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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