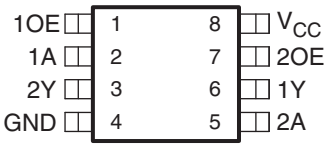
LOW-POWER DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Check for Samples: SN74AUP2G126

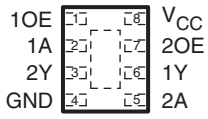
FEATURES

- **Available in the Texas Instruments NanoStar™ Package**
- **Low Static-Power Consumption (I_{CC} = 0.9 µA Max)**
- **Low Dynamic-Power Consumption (C_{pd} = 4 pF Typ at 3.3 V)**
- **Low Input Capacitance (C_i = 1.5 pF Typ)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **Input-Disable Feature Allows Floating Input Conditions**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 9.9 ns Max at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

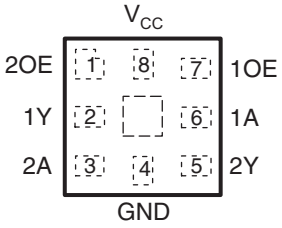
DCU PACKAGE
(TOP VIEW)



DQE PACKAGE
(TOP VIEW)

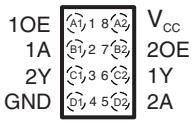


RSE PACKAGE
(TOP VIEW)



The exposed center pad, if used, must be connected only as a secondary GND or left electrically open.

YFP OR YZP PACKAGE
(TOP VIEW)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

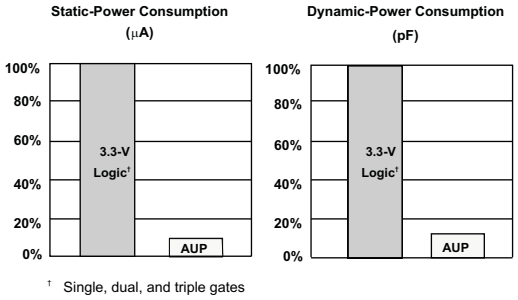


Figure 1. AUP – The Lowest Power Family

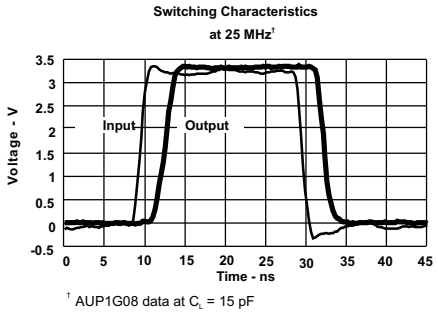


Figure 2. Excellent Signal Integrity

The SN74AUP2G126 is a dual bus driver/line driver with 3-state outputs, designed for 0.8-V to 3.6-V V_{CC} operation. The outputs are disabled when the associated output-enable (OE) input is low. This device has the input-disable feature, which allows floating input signals.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G126YFPR	_ _ _ HN_
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP2G126YZPR	_ _ _ HN_
	uQFN – DQE	Reel of 5000	SN74AUP2G126DQER	PW
	QFN – RSE	Reel of 5000	SN74AUP2G126RSER	HN
	VSSOP – DCU	Reel of 3000	SN74AUP2G126DCUR	H26_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).
DCU: The actual top-side marking has one additional character to designate the wafer fab/assembly site.

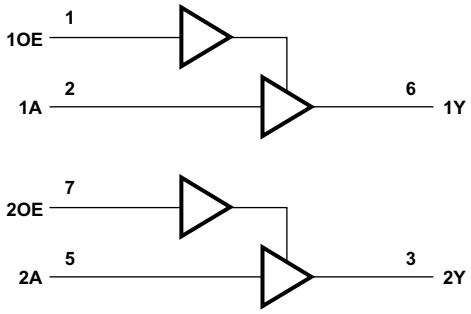
FUNCTION TABLE

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X(1)	Z

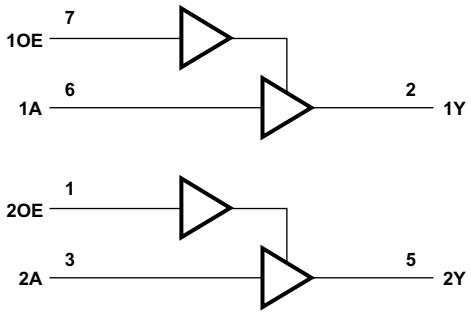
(1) Floating inputs allowed

LOGIC DIAGRAMS (POSITIVE LOGIC)

DCU, DQE, YFP, and YZP Packages



RSE Package



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage range in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DCU package		227	°C/W
		DQE package		261	
		RSE package		253	
		YZP package		102	
		YFP package		98.8	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}	3.6	V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}	3.6	
		V_{CC} = 2.3 V to 2.7 V	1.6	3.6	
		V_{CC} = 3 V to 3.6 V	2	3.6	
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V	0	0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V	0	0.7	
		V_{CC} = 3 V to 3.6 V	0	0.9	
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
		I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
		I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
		I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = –3.1 mA		1.9			1.85		
		I_{OH} = –2.7 mA	3 V	2.72			2.67		
		I_{OH} = –4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	A or OE input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	µA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	µA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.9	µA
I_{OZ}		V_O = V_{CC} or GND	3.6 V			0.1		0.5	µA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), OE = V_{CC} , I_O = 0	0.8 V to 3.6 V			0.5		0.9	µA
ΔI_{CC}	A input	V_I = V_{CC} – 0.6 V(1), I_O = 0	3.3 V			40		50	µA
	OE input					110		120	
	All inputs	V_I = GND to 3.6 V, OE = GND(2)	0.8 V to 3.6 V			0		0	
C_I		V_I = V_{CC} or GND	0 V		2				pF
			3.6 V		2				
C_o		V_O = V_{CC} or GND	3.6 V		3				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND
(2) To show I_{CC} is very low when the input-disable feature is enabled

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		19.2				ns
			1.2 V ± 0.1 V	0.5	7.5	17.9	0.5	18.7	
			1.5 V ± 0.1 V	0.6	5.2	10.8	0.5	12.4	
			1.8 V ± 0.15 V	0.8	4.1	8.1	0.5	9.7	
			2.5 V ± 0.2 V	1.1	2.9	5	0.5	6.5	
			3.3 V ± 0.3 V	0.5	3	9.5	0.5	9.9	
t_{en}	OE	Y	0.8 V		19.6				ns
			1.2 V ± 0.1 V	0.5	8.4	20.8	0.5	21.8	
			1.5 V ± 0.1 V	0.5	5.6	11.8	0.5	13.7	
			1.8 V ± 0.15 V	0.7	4.3	8.8	0.5	10.6	
			2.5 V ± 0.2 V	0.9	2.9	5.4	0.5	7	
			3.3 V ± 0.3 V	0.5	2.8	8.8	0.5	9.3	
t_{dis}	OE	Y	0.8 V		12.1				ns
			1.2 V ± 0.1 V	0.6	5.2	10.9	0.5	11.1	
			1.5 V ± 0.1 V	1.1	3.8	7	0.9	7.1	
			1.8 V ± 0.15 V	1.9	3.5	5.6	1.6	5.8	
			2.5 V ± 0.2 V	0.9	2.5	3.9	0.8	4.2	
			3.3 V ± 0.3 V	0.5	3.5	9.3	0.5	9.3	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		23				ns
			1.2 V ± 0.1 V	0.5	8.7	20.6	0.5	21.3	
			1.5 V ± 0.1 V	1.2	6	12.2	0.5	13.7	
			1.8 V ± 0.15 V	1.4	4.8	9.2	0.5	10.8	
			2.5 V ± 0.2 V	1.5	3.4	5.8	0.5	7.2	
			3.3 V ± 0.3 V	0.5	3.4	8.9	0.5	9.4	
t_{en}	OE	Y	0.8 V		21.9				ns
			1.2 V ± 0.1 V	0.5	9.7	23.1	0.5	24	
			1.5 V ± 0.1 V	1	6.4	13.2	0.5	15	
			1.8 V ± 0.15 V	1	5	9.9	0.5	11.7	
			2.5 V ± 0.2 V	1.2	3.4	10.4	0.5	12	
			3.3 V ± 0.3 V	0.5	3.2	8.1	0.5	8.7	
t_{dis}	OE	Y	0.8 V		13.4				ns
			1.2 V ± 0.1 V	0.8	6.2	12.6	0.6	12.7	
			1.5 V ± 0.1 V	2.1	4.6	7.9	1.9	8.1	
			1.8 V ± 0.15 V	1.7	4.7	8.2	1.5	8.3	
			2.5 V ± 0.2 V	1	3.3	5.1	0.9	5.3	
			3.3 V ± 0.3 V	1.2	4.5	7.8	1.1	7.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		26.2				ns
			1.2 V ± 0.1 V	0.5	9.7	22.7	0.5	23.4	
			1.5 V ± 0.1 V	1.7	4.6	13.6	0.5	15	
			1.8 V ± 0.15 V	1.7	5.4	10.2	0.5	11.7	
			2.5 V ± 0.2 V	1.7	3.9	6.5	0.5	7.9	
			3.3 V ± 0.3 V	0.5	3.7	8.4	0.5	8.9	
t_{en}	OE	Y	0.8 V		23				ns
			1.2 V ± 0.1 V	0.5	10.5	24.8	0.5	25.6	
			1.5 V ± 0.1 V	1.5	7.1	14.3	0.5	16	
			1.8 V ± 0.15 V	1.4	5.6	10.8	0.5	12.4	
			2.5 V ± 0.2 V	1.6	3.9	6.8	0.5	8.3	
			3.3 V ± 0.3 V	0.5	3.6	7.6	0.5	8.3	
t_{dis}	OE	Y	0.8 V		13.6				ns
			1.2 V ± 0.1 V	1.1	6.5	12.7	1	12.8	
			1.5 V ± 0.1 V	0.5	4.8	9.1	0.5	9.2	
			1.8 V ± 0.15 V	1.8	5.4	9.2	1.7	9.3	
			2.5 V ± 0.2 V	1.6	3.7	5.5	1.5	5.7	
			3.3 V ± 0.3 V	2.8	5.3	7.9	2.7	7.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

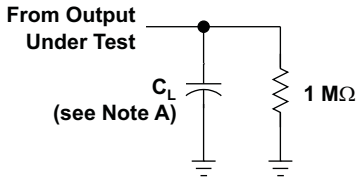
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		36.4				ns
			1.2 V ± 0.1 V	0.5	13	30.8	0.5	31.2	
			1.5 V ± 0.1 V	2.7	9.1	18	1.1	19.1	
			1.8 V ± 0.15 V	2.6	7.2	13.6	1	14.8	
			2.5 V ± 0.2 V	2.6	5.3	8.6	1.3	9.9	
			3.3 V ± 0.3 V	1.4	4.8	7.9	0.7	8.6	
t_{en}	OE	Y	0.8 V		32.8				ns
			1.2 V ± 0.1 V	0.5	14.4	32.4	0.5	33.1	
			1.5 V ± 0.1 V	2.5	9.7	18.5	1.1	19.9	
			1.8 V ± 0.15 V	2.3	7.6	14.3	0.8	15.7	
			2.5 V ± 0.2 V	2.4	5.3	9	1.2	10.3	
			3.3 V ± 0.3 V	2.8	4.6	7.2	1.7	8.2	
t_{dis}	OE	Y	0.8 V		20.1				ns
			1.2 V ± 0.1 V	0.5	10.3	19.3	0.5	19.3	
			1.5 V ± 0.1 V	1.9	7.6	14.5	1.8	14.5	
			1.8 V ± 0.15 V	3	8.8	14.9	2.8	14.9	
			2.5 V ± 0.2 V	2.9	6.5	10	2.9	10.1	
			3.3 V ± 0.3 V	0.5	8.2	17.9	0.5	17.9	

OPERATING CHARACTERISTICS

T_A = 25°C

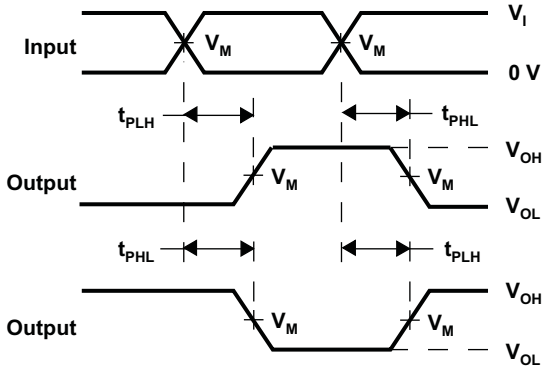
PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	0.8 V	3.8	pF
				1.2 V ± 0.1 V	3.7	
				1.5 V ± 0.1 V	3.7	
				1.8 V ± 0.15 V	3.7	
				2.5 V ± 0.2 V	3.9	
				3.3 V ± 0.3 V	4	
		Outputs disabled	f = 10 MHz	0.8 V	0	
				1.2 V ± 0.1 V	0	
				1.5 V ± 0.1 V	0	
				1.8 V ± 0.15 V	0	
				2.5 V ± 0.2 V	0	
				3.3 V ± 0.3 V	0	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)

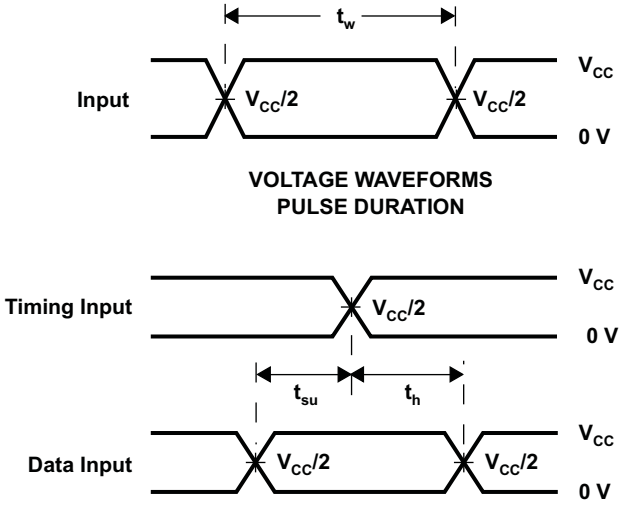


LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



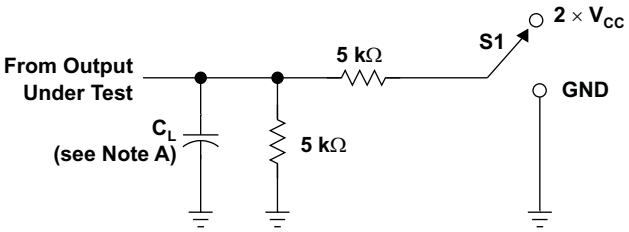
VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

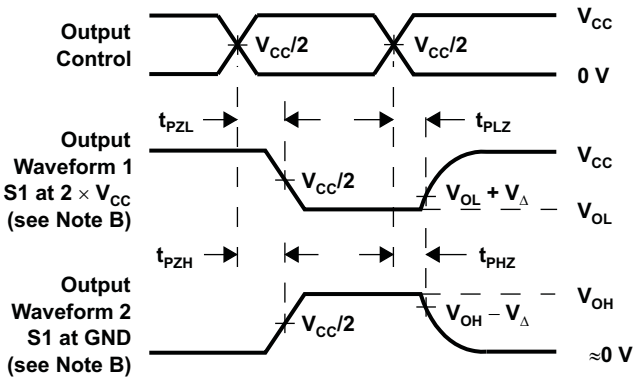
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	2 × V_{CC} GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP2G126DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R	Samples
SN74AUP2G126DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW	Samples
SN74AUP2G126RSER	ACTIVE	UQFN	RSE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW	Samples
SN74AUP2G126YFPR	ACTIVE	DSBGA	YFP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HN7 ~ HNN)	Samples
SN74AUP2G126YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HN7 ~ HNN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

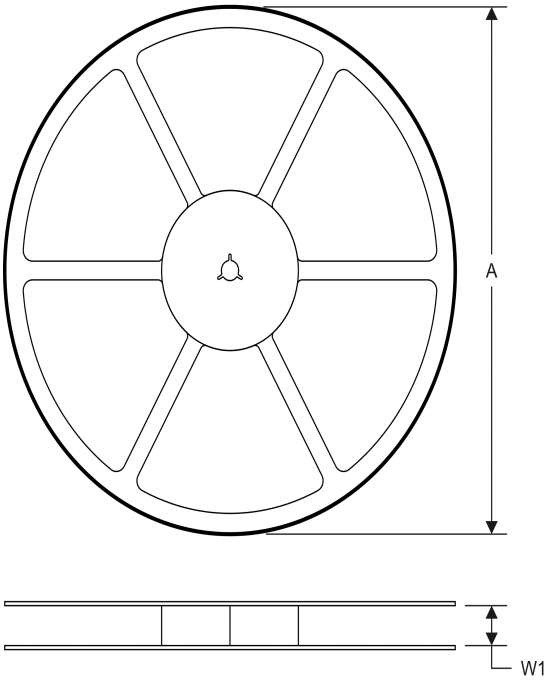
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

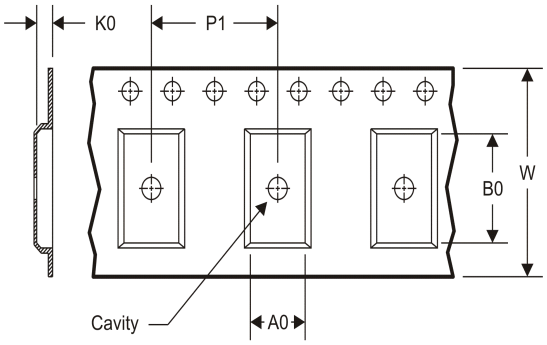
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



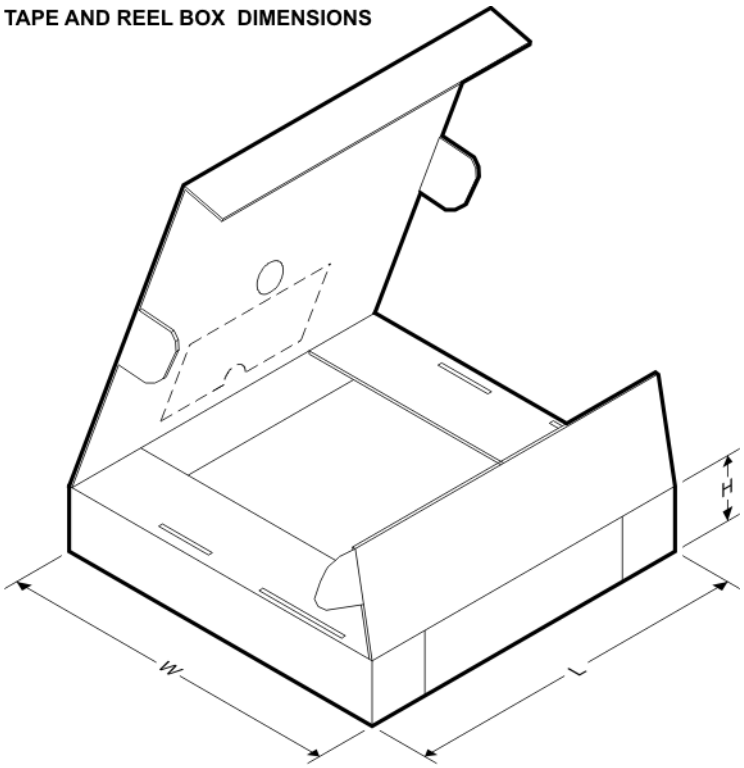
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G126DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G126DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP2G126RSER	UQFN	RSE	8	5000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2
SN74AUP2G126YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1
SN74AUP2G126YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

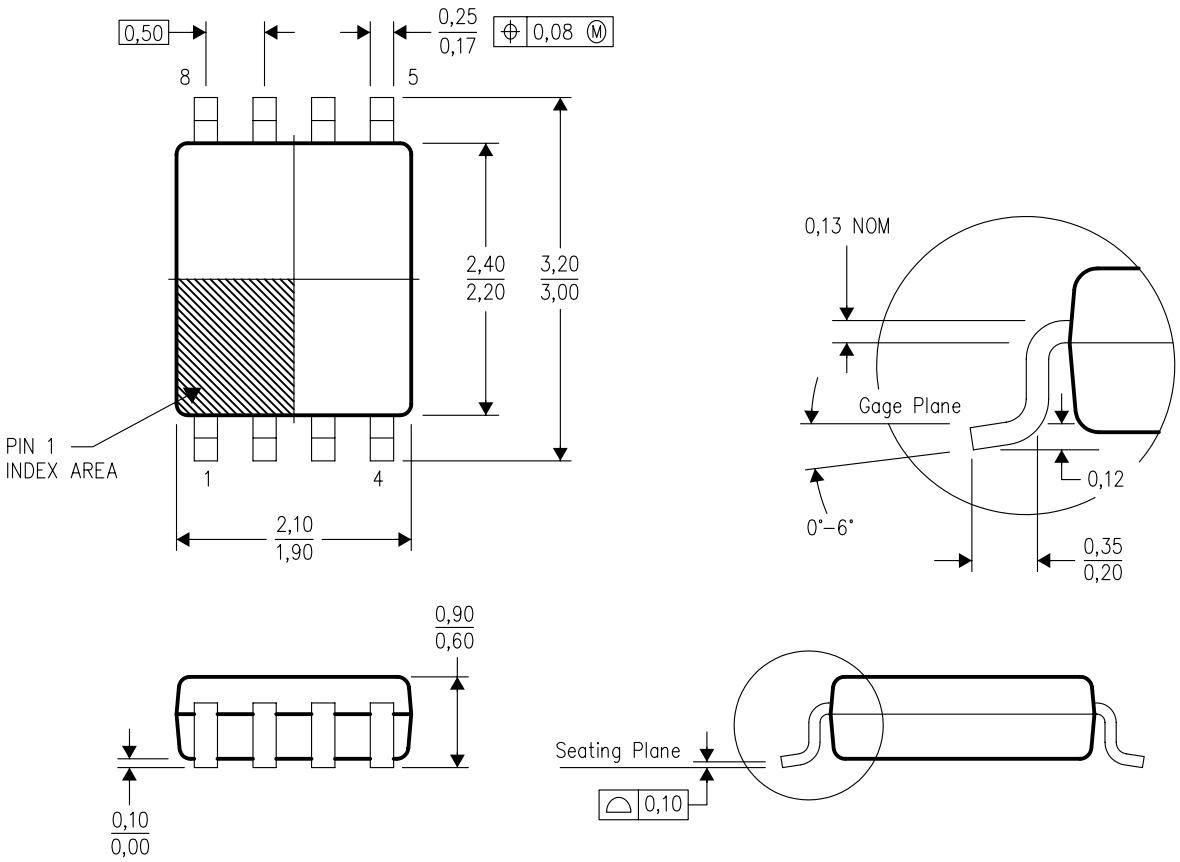
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G126DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G126DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP2G126RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP2G126YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0
SN74AUP2G126YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

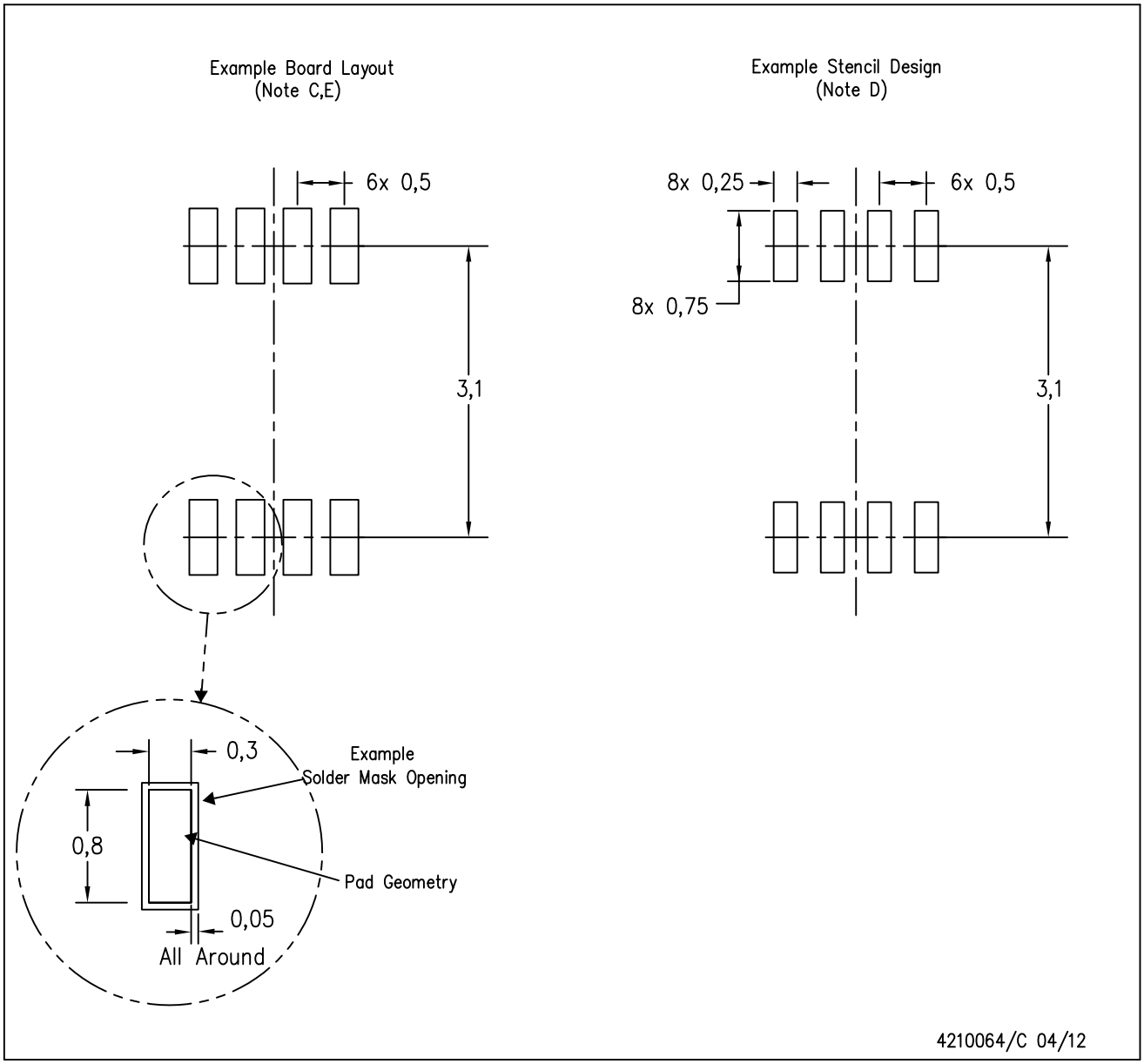
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

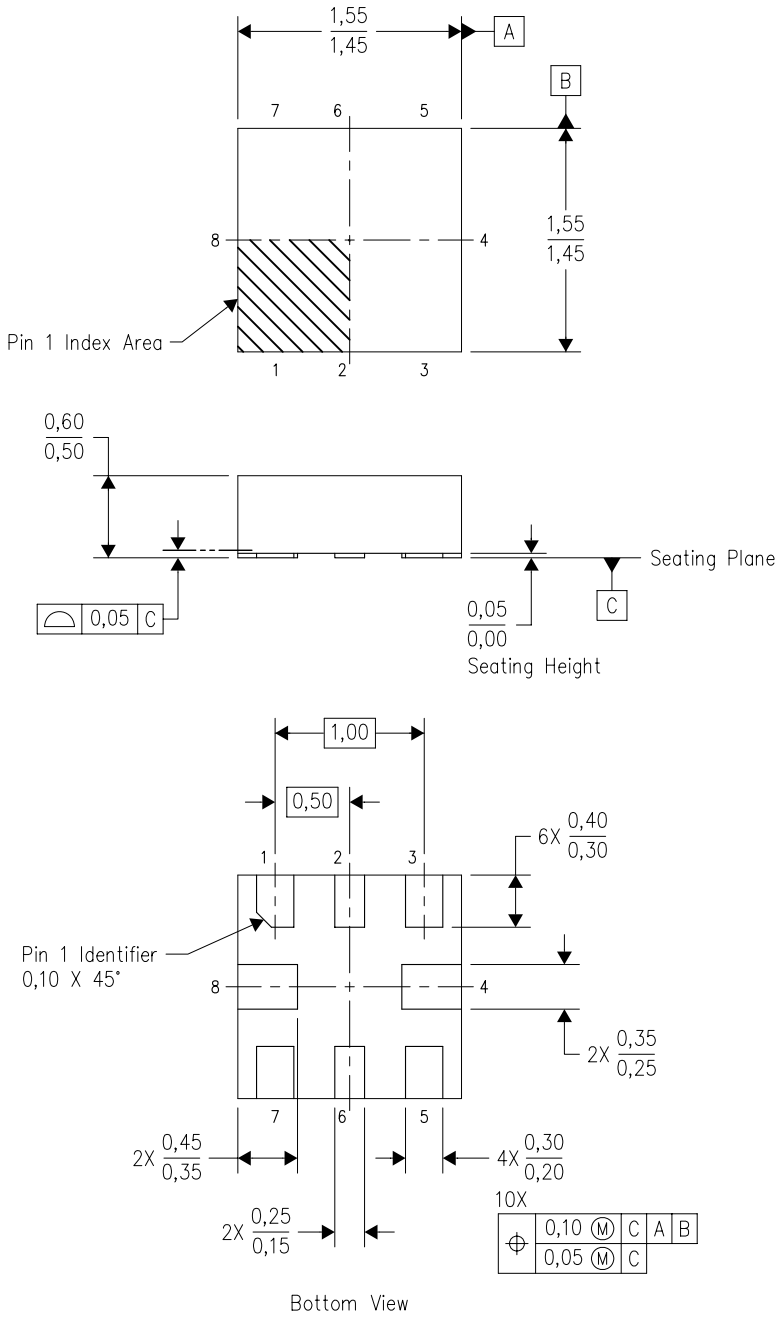
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

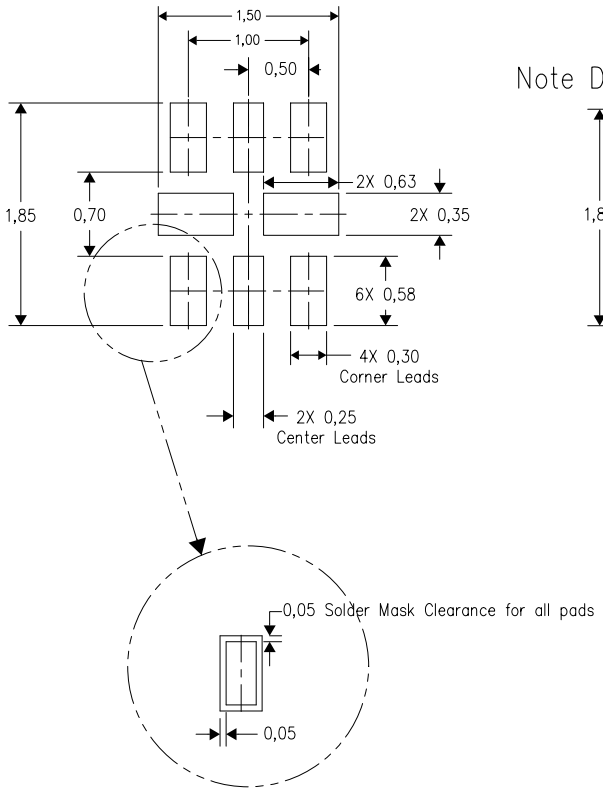


4207268–2/D 01/11

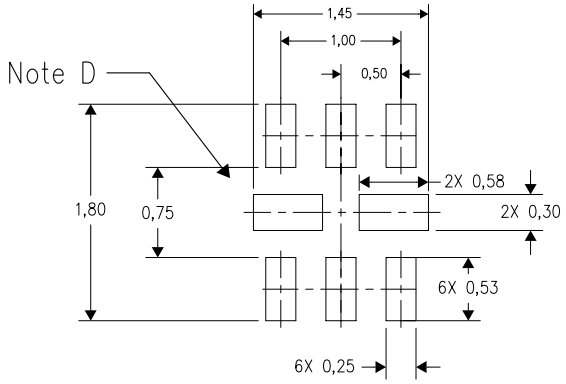
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UECD.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout



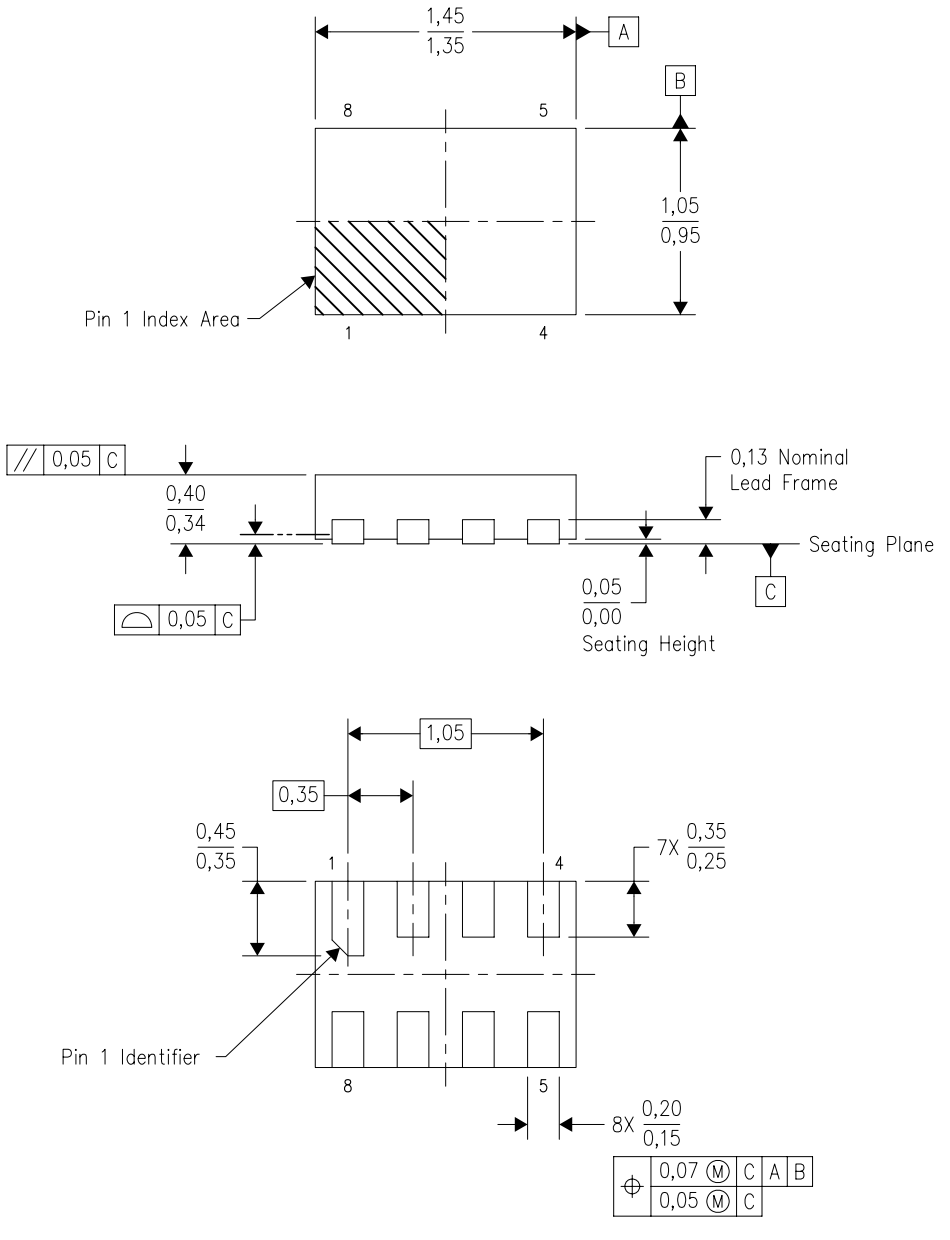
Example Stencil Design
(Note E)



4208106–2/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

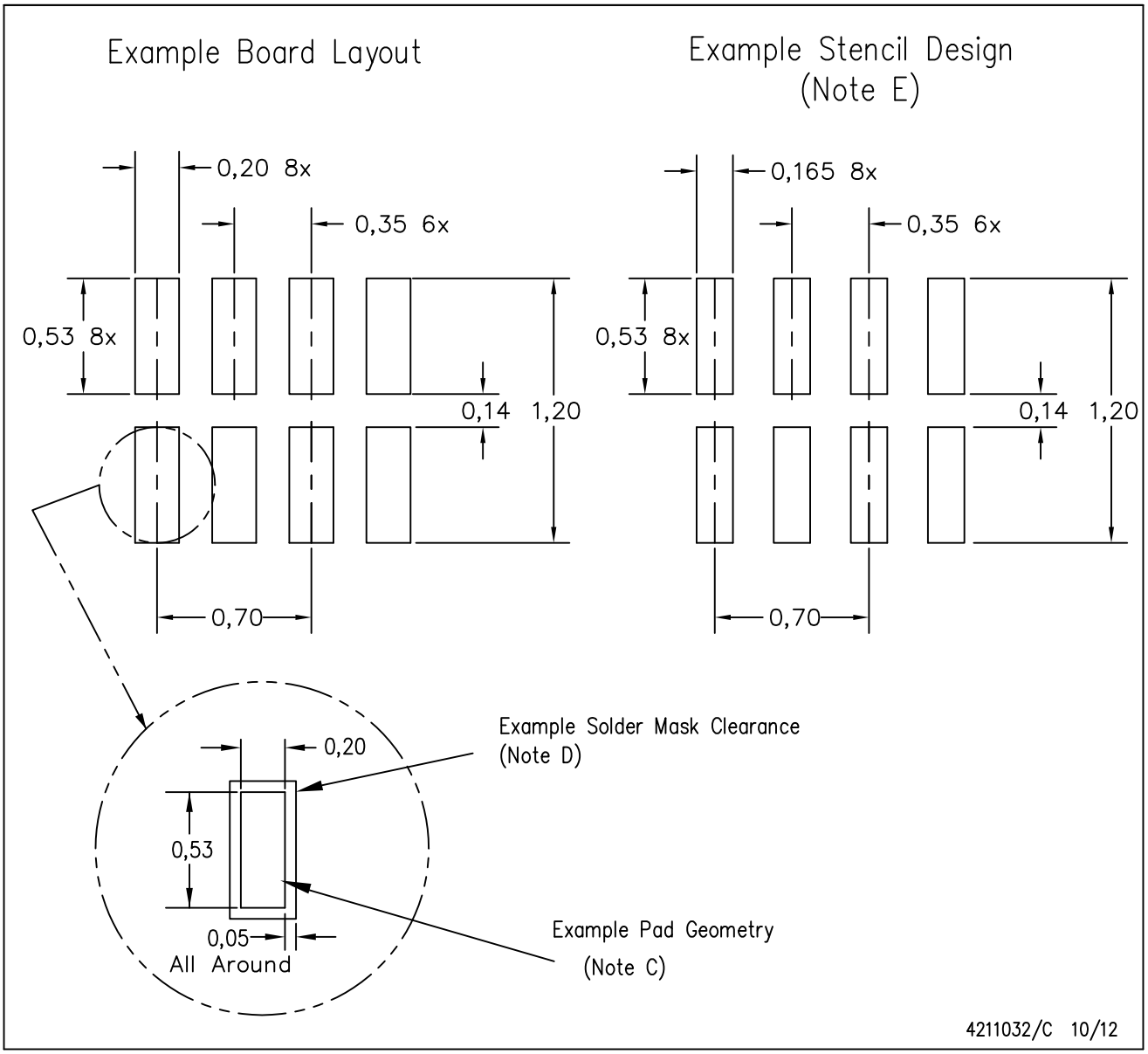
DQE (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4209779/B 10/2008

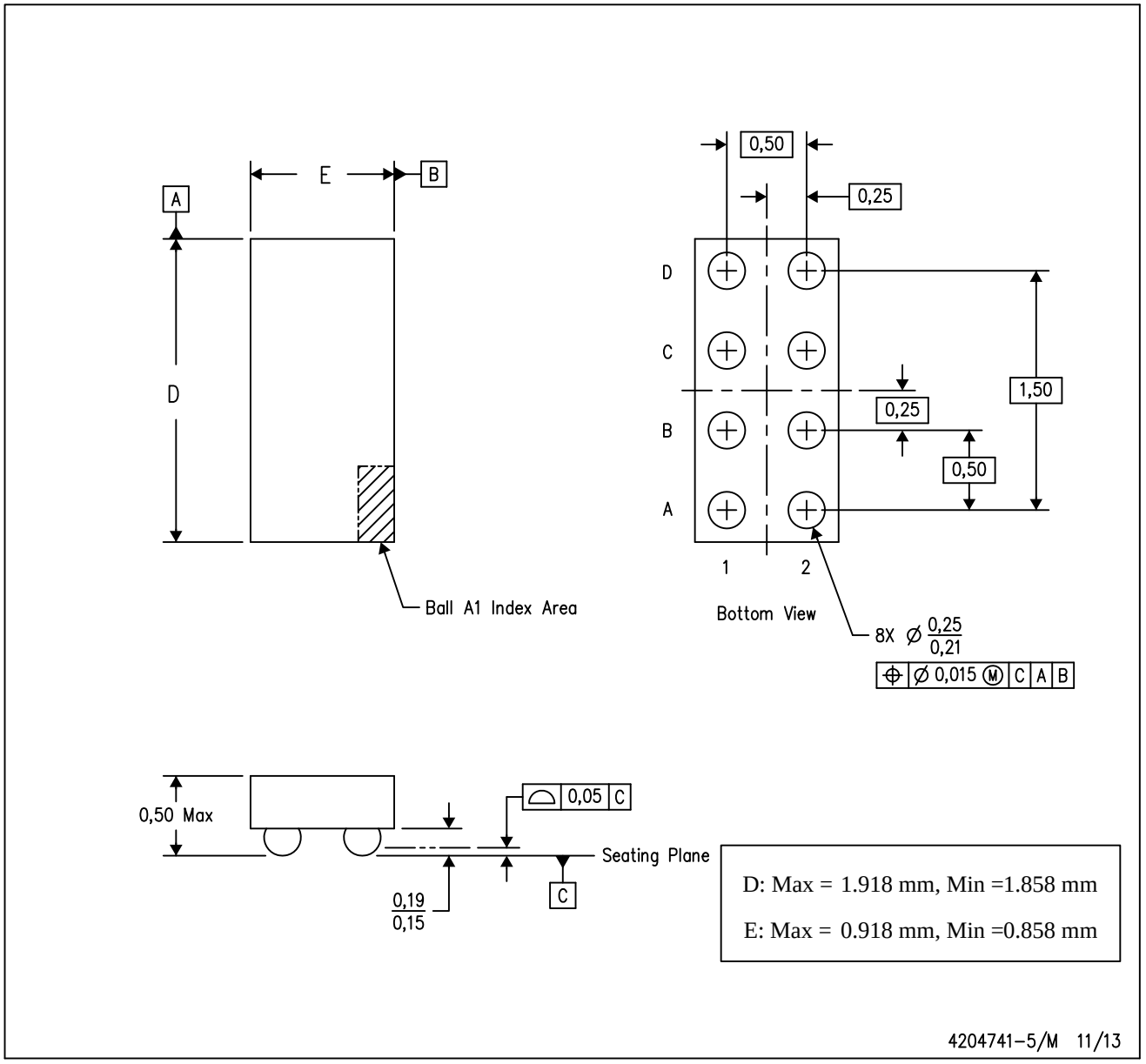
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation X2EAF.

DQE (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.

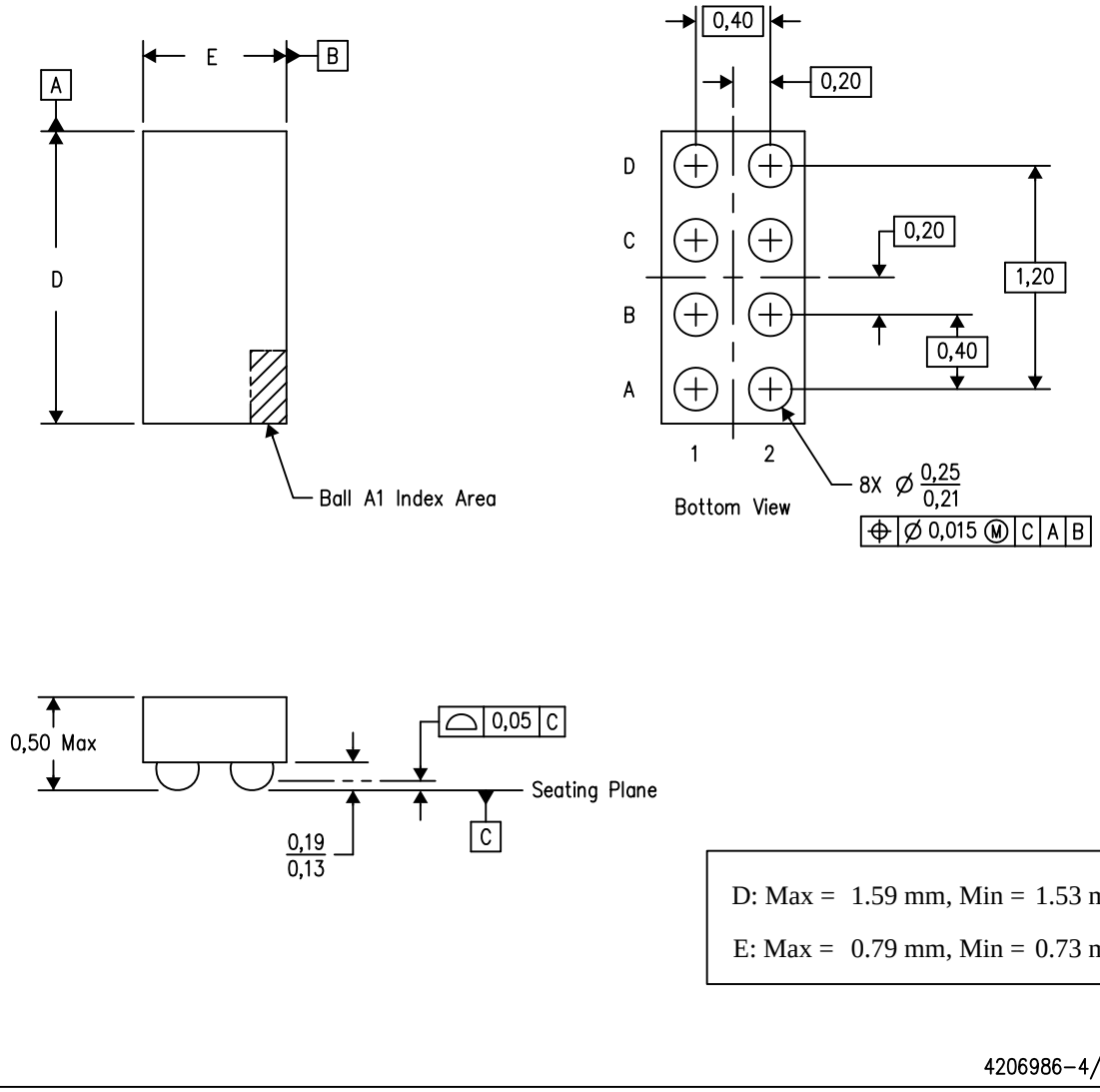
YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

YFP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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