

SN54ACT564, SN74ACT564 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS549B – NOVEMBER 1995 – REVISED NOVEMBER 2002

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 8.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible
- 3-State Inverted Outputs Drive Bus Lines Directly
- Flow-Through Architecture to Optimize PCB Layout
- Full Parallel Access for Loading

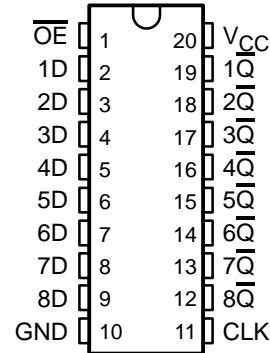
description/ordering information

The 'ACT564 devices are octal D-type edge-triggered flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

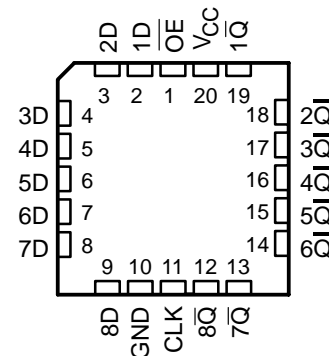
On the positive transition of the clock (CLK) input, the \bar{Q} outputs are set to the complements of the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

SN54ACT564 . . . J OR W PACKAGE
SN74ACT564 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT564 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ACT564N	SN74ACT564N
	SOIC – DW	Tube	SN74ACT564DW	ACT564
		Tape and reel	SN74ACT564DWR	
	SOP – NS	Tape and reel	SN74ACT564NSR	ACT564
	SSOP – DB	Tape and reel	SN74ACT564DBR	AD564
	TSSOP – PW	Tape and reel	SN74ACT564PWR	AD564
-55°C to 125°C	CDIP – J	Tube	SNJ54ACT564J	SNJ54ACT564J
	CFP – W	Tube	SNJ54ACT564W	SNJ54ACT564W
	LCCC – FK	Tube	SNJ54ACT564FK	SNJ54ACT564FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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description/ordering information (continued)

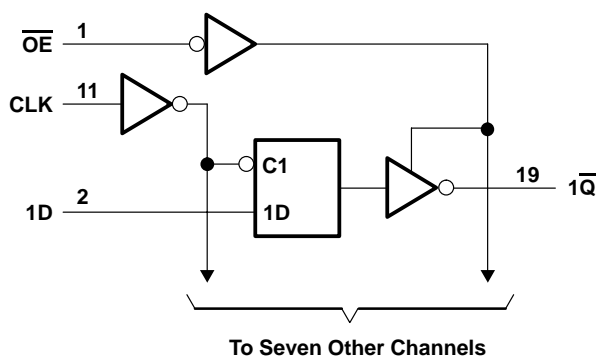
\overline{OE} does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	\overline{Q}
L	↑	H	L
L	↑	L	H
L	H or L	X	\overline{Q}_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		SN54ACT564		SN74ACT564		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54ACT564		SN74ACT564		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.49	4.4		4.4		V	
		5.5 V	5.4	5.49	5.4		5.4			
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.86		3.7		3.76			
		5.5 V	4.86		4.7		4.76			
	$I_{OH} = -50 \text{ mA}^\dagger$	5.5 V			3.85					
$I_{OH} = -75 \text{ mA}^\dagger$	5.5 V					3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	0.1	V	
		5.5 V			0.1		0.1	0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	$I_{OL} = 50 \text{ mA}^\dagger$	5.5 V					1.65			
$I_{OL} = 75 \text{ mA}^\dagger$	5.5 V						1.65			
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.25		± 5	± 2.5	μA	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	± 1	μA	
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80	40	μA	
ΔI_{CC}^\ddagger	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.6		1.6		1.5	mA	
C_i	$V_I = V_{CC}$ or GND	5 V		4.5					pF	
C_o	$V_O = V_{CC}$ or GND	5 V		15					pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

	$T_A = 25^\circ\text{C}$		SN54ACT564		SN74ACT564		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency	85		65		75		MHz
t_w Pulse duration, CLK high or low	3		5		3.5		ns
t_{su} Setup time, data before CLK \uparrow	2.5		3.5		3		ns
t_h Hold time, data after CLK \uparrow	1		2.5		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54ACT564		SN74ACT564		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			85	90		65		75	MHz	
t_{PLH}	CLK	\bar{Q}	2	6.5	10.5	1	12.5	1.5	11.5	ns
t_{PHL}			1.5	6	9.5	1	11.5	1.5	10.5	
t_{PZH}	$\overline{\text{OE}}$	\bar{Q}	1.5	5.5	9	1	10.5	1.5	9.5	ns
t_{PZL}			1.5	5.5	8.5	1	10.5	1	9.5	
t_{PHZ}	$\overline{\text{OE}}$	\bar{Q}	1.5	7	10.5	1	12.5	1.5	11.5	ns
t_{PLZ}			1.5	5	8	1	9.5	1	8.5	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	50	pF

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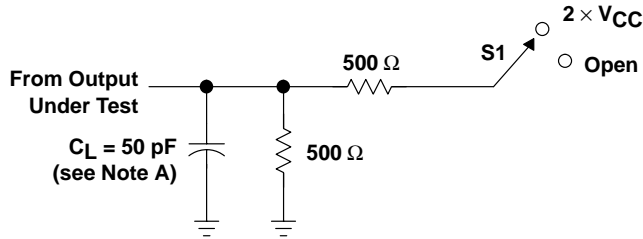


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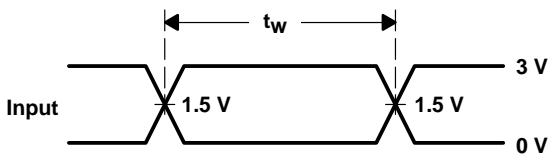
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PARAMETER MEASUREMENT INFORMATION

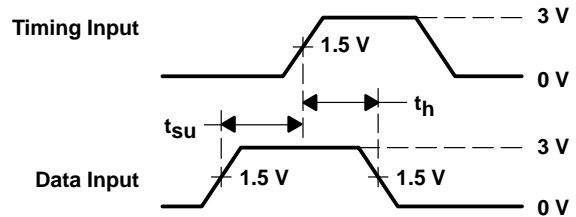


LOAD CIRCUIT

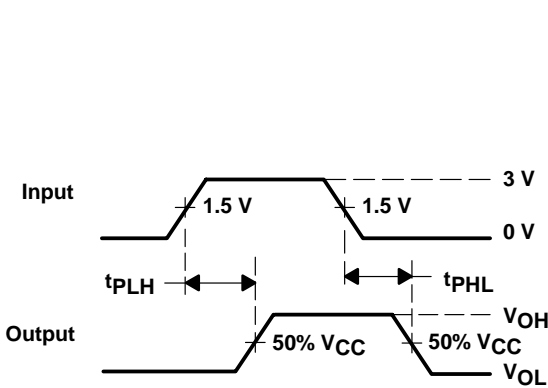
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



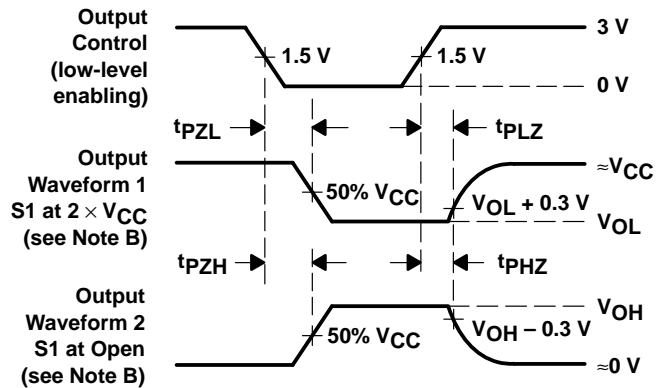
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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