

## 5-V PECL-to-TTL Translator

### FEATURES

- 3ns (TYP) Propagation Delay
- Operating Range:  $V_{CC} = 4.2\text{ V}$  to  $5.7\text{ V}$  with  $GND = 0\text{ V}$
- 24-mA TTL Output
- Deterministic Output Value for Open Input Conditions or When Inputs  $< 1.3\text{ V}$
- Built-In Temperature Compensation
- Drop-In Compatible to the MC10ELT21, MC100ELT21

### APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion for Clock or Data

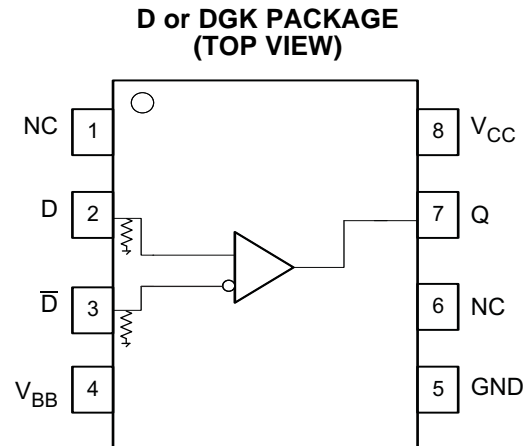
### DESCRIPTION

The SN65ELT21 is a differential PECL-to-TTL translator. It operates on +5-V supply and ground only. The device includes circuitry to maintain Q to a low logic level when inputs are in an open condition or  $< 1.3\text{ V}$ .

The  $V_{BB}$  pin is a reference voltage output for the device. When the device is used in single-ended mode, the unused input should be tied to  $V_{BB}$ . This reference voltage can also be used to bias the input when it is ac coupled. When it is used, place a  $0.01\mu\text{F}$  decoupling capacitor between  $V_{CC}$  and  $V_{BB}$ . Also limit the sink/source current to  $< 0.5\text{ mA}$  to  $V_{BB}$ . Leave  $V_{BB}$  open when it is not used.

The SN65ELT21 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

### PIN ASSIGNMENT



**Table 1. Pin Descriptions**

PIN	FUNCTION
D, $\bar{D}$	PECL data inputs
Q	TTL output
$V_{CC}$	Positive supply
$V_{EE}$	Negative supply
$V_{BB}$	Reference voltage output

### ORDERING INFORMATION<sup>(1)(2)</sup>

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65ELT21D	ELT21	SOIC	NiPdAu
SN65ELT21DGK	SIII	SOIC-TSSOP	NiPdAu

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Leaded device options are not initially available; contact a sales representative for further details.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL mode supply voltage	$V_{CC}$ (GND = 0 V)	6	V
Sink/source current, $V_{BB}$		$\pm 0.5$	mA
PECL input voltage	GND = 0 V, $V_I \leq V_{CC}$	6	V
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

## THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$\theta_{JB}$	Junction-to-board thermal resistance	SOIC	79		°C/W
		SOIC-TSSOP	120		
$\theta_{JC}$	Junction-to-case thermal resistance	SOIC	98		°C/W
		SOIC-TSSOP	74		

## KEY ATTRIBUTES

CHARACTERISTICS	VALUE	
Internal input pull-down resistor	50 k $\Omega$	
Moisture sensitivity level	Level 1	
Flame ability rating (oxygen index: 28 to 34)	UL 94 V-0 at 0.125 in	
Electrostatic discharge	Human body model	2 kV
	Charged-device model	1.5 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test		

## PECL DC CHARACTERISTICS

At  $V_{CC} = 5.0\text{ V}$ ,  $GND = 0.0\text{ V}$  (unless otherwise noted)<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ\text{C}$			$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IH}$	High-level input voltage, single-ended	3835		4120	3835		4120	3835		4120	mV
$V_{IL}$	Low-level input voltage, single-ended	3190		3525	3190		3525	3190		3525	mV
$V_{BB}$	Output reference voltage	3.62	3.69	3.74	3.62	3.69	3.74	3.62	3.69	3.74	V
$V_{IHCMR}$	High-level input voltage, common-mode range, differential	See <sup>(3)</sup>			2.2		5.0	2.2		5.0	V
$I_{IH}$	High-level input current			150			150			150	$\mu\text{A}$
$I_{IL}$	Low-level input current	0.5			0.5			0.5			$\mu\text{A}$

- (1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $+0.7\text{ V} / -0.8\text{ V}$ .
- (3)  $V_{IHCMR(\text{min})}$  varies 1:1 with  $GND$ ,  $V_{IHCMR(\text{max})}$  varies 1:1 with  $V_{CC}$ .

## TTL DC CHARACTERISTICS

At  $V_{CC} = 4.2\text{ V}$  to  $5.7\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CCH}$	Power supply current			20	mA
$I_{CCL}$	Power supply current			20	mA
$V_{OH}$	High-level output voltage	$I_{OH} = -3.0\text{ mA}$		2.4	See <sup>(2)</sup> V
$V_{OL}$	Low-level output voltage	$I_{OL} = 24\text{ mA}$		0.5	V
$I_{OS}$	Output short circuit current	-150		-60	mA

- (1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2)  $V_{OH(\text{max})}$  level is  $V_{CC} - 0.7$ .

## AC CHARACTERISTICS

At  $V_{CC} = 4.2\text{ V}$  to  $5.7\text{ V}$ ,  $GND = 0.0\text{ V}$  (unless otherwise noted)<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ\text{C}$			$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{\text{MAX}}$	Maximum switching frequency	At $V_{ol} < 0.5\text{ V}$ (See Figure 4)			200			200			MHz
$t_{\text{PLH}}/t_{\text{PHL}}$	Propagation delay times	2		4.5	2		4.5	2		4.5	ns
$t_{\text{JITTER}}$	Random clock jitter (RMS)		5	20		5	20		5	20	ps
$V_{\text{PP}}$	Input swing	See <sup>(3)</sup>			200		1000	200		1000	mV
$t_r/t_f$	Output rise/fall times	Q (10%–90%)			750			780			ps

- (1) The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2)  $R_L = 500\ \Omega$  to  $GND$  and  $C_L = 20\text{ pF}$  to  $GND$ . See Figure 1.
- (3)  $V_{\text{PP}(\text{min})}$  is minimum input swing for which ac parameters are assured.

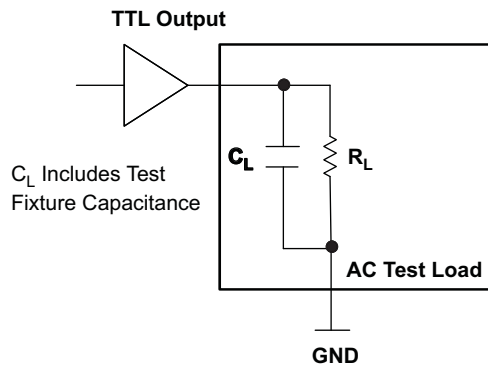


Figure 1. TTL Output AC Test Loading Condition

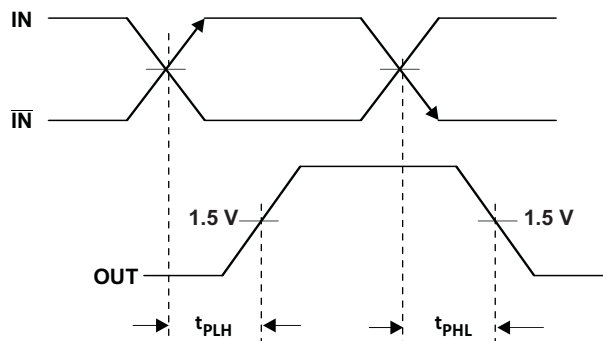


Figure 2. Output Propagation Delay

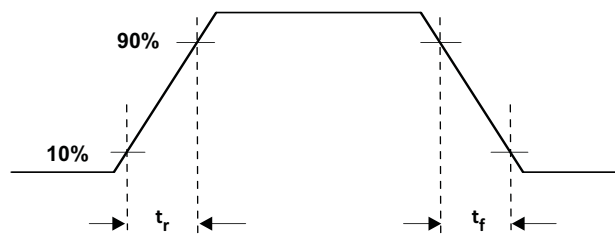
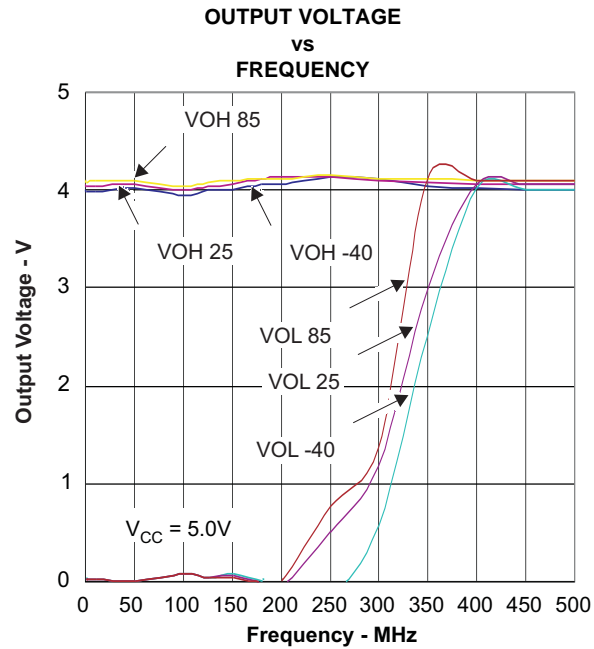


Figure 3. Output Rise and Fall Times



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN65ELT21D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65ELT21DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65ELT21DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65ELT21DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

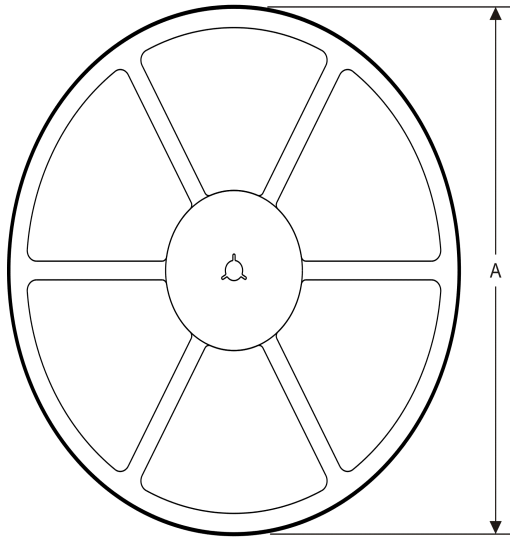
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ELT21DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65ELT21DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

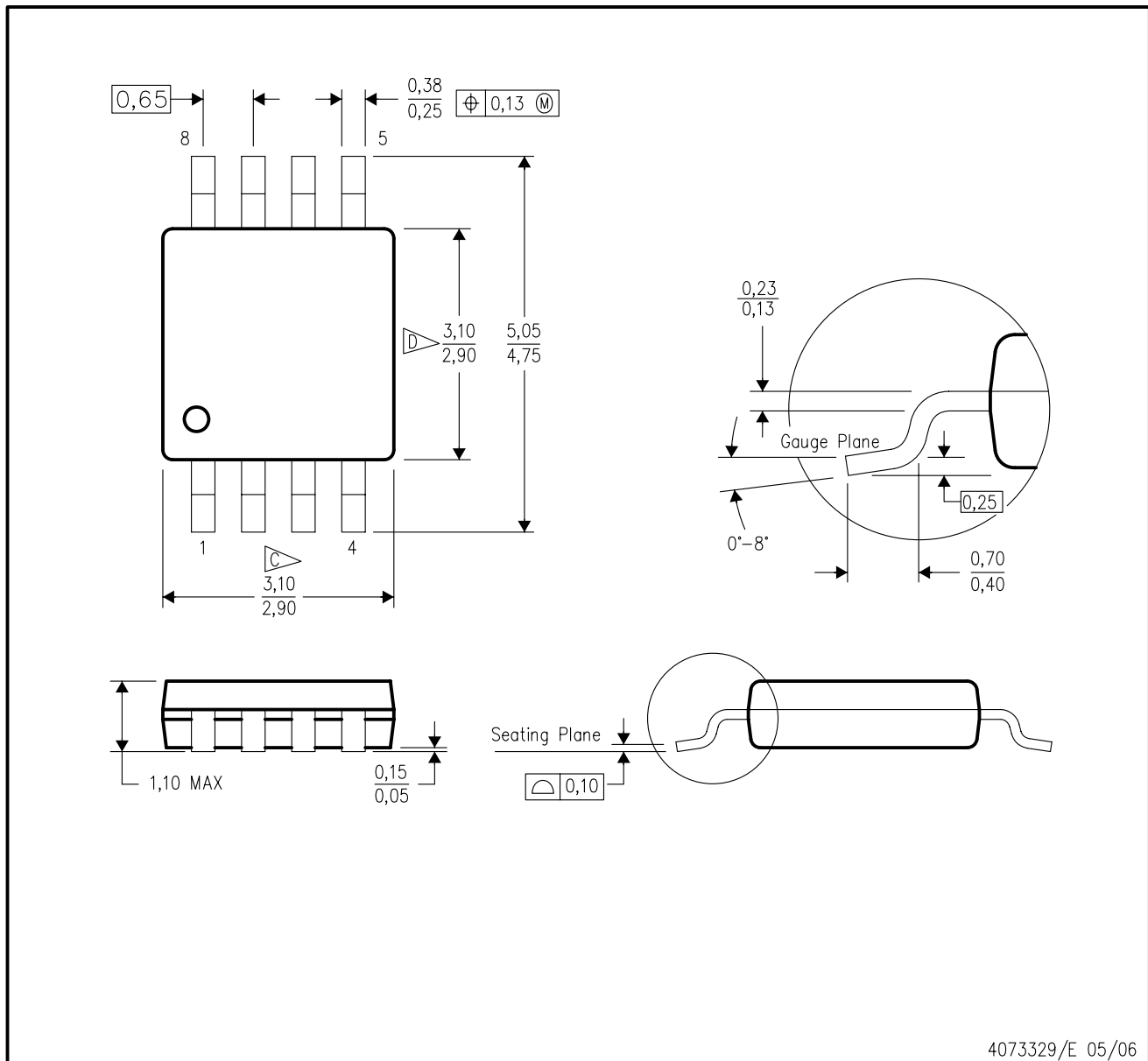

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ELT21DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65ELT21DR	SOIC	D	8	2500	367.0	367.0	35.0



DGK (S-PDSO-G8)

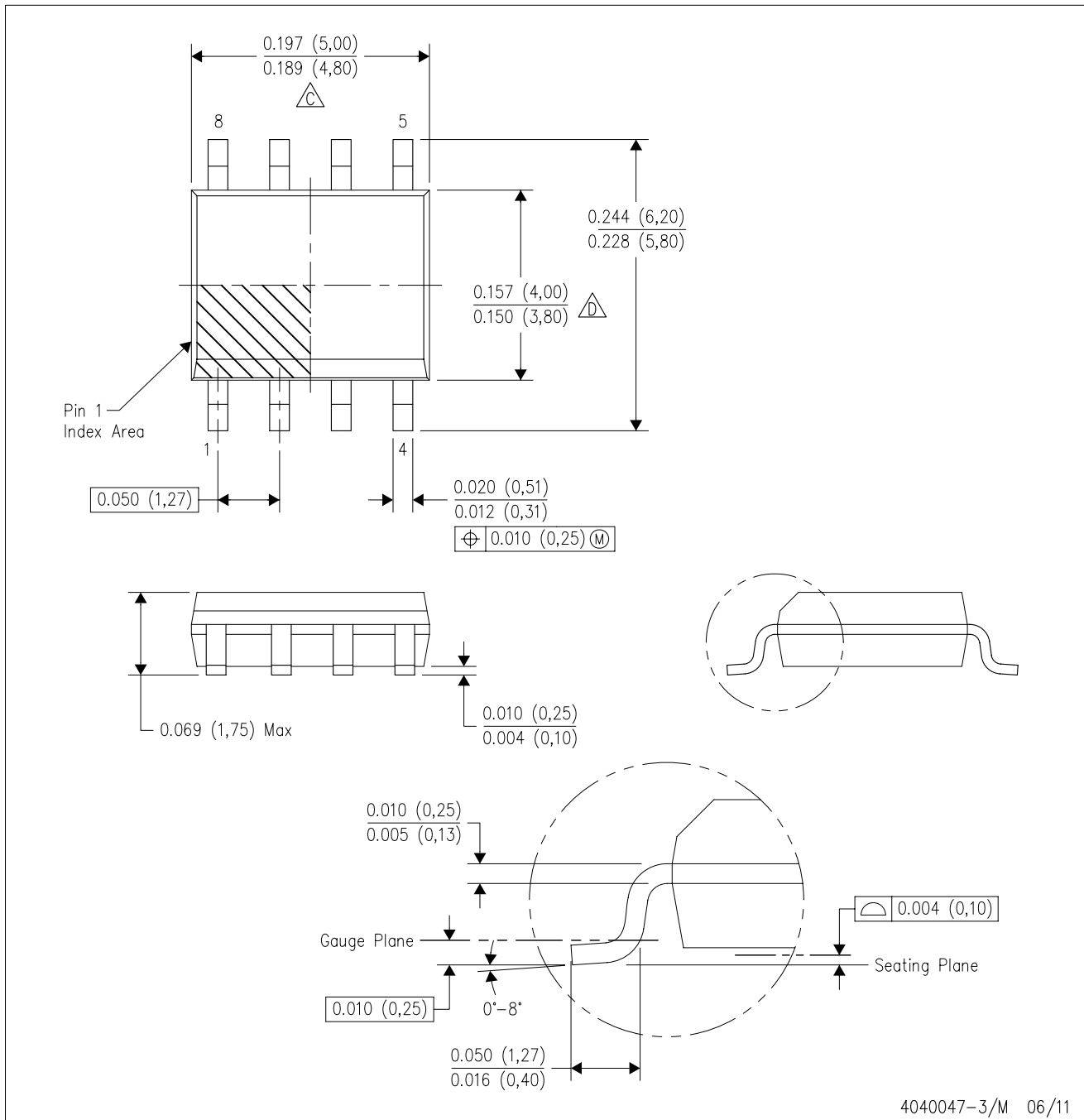
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

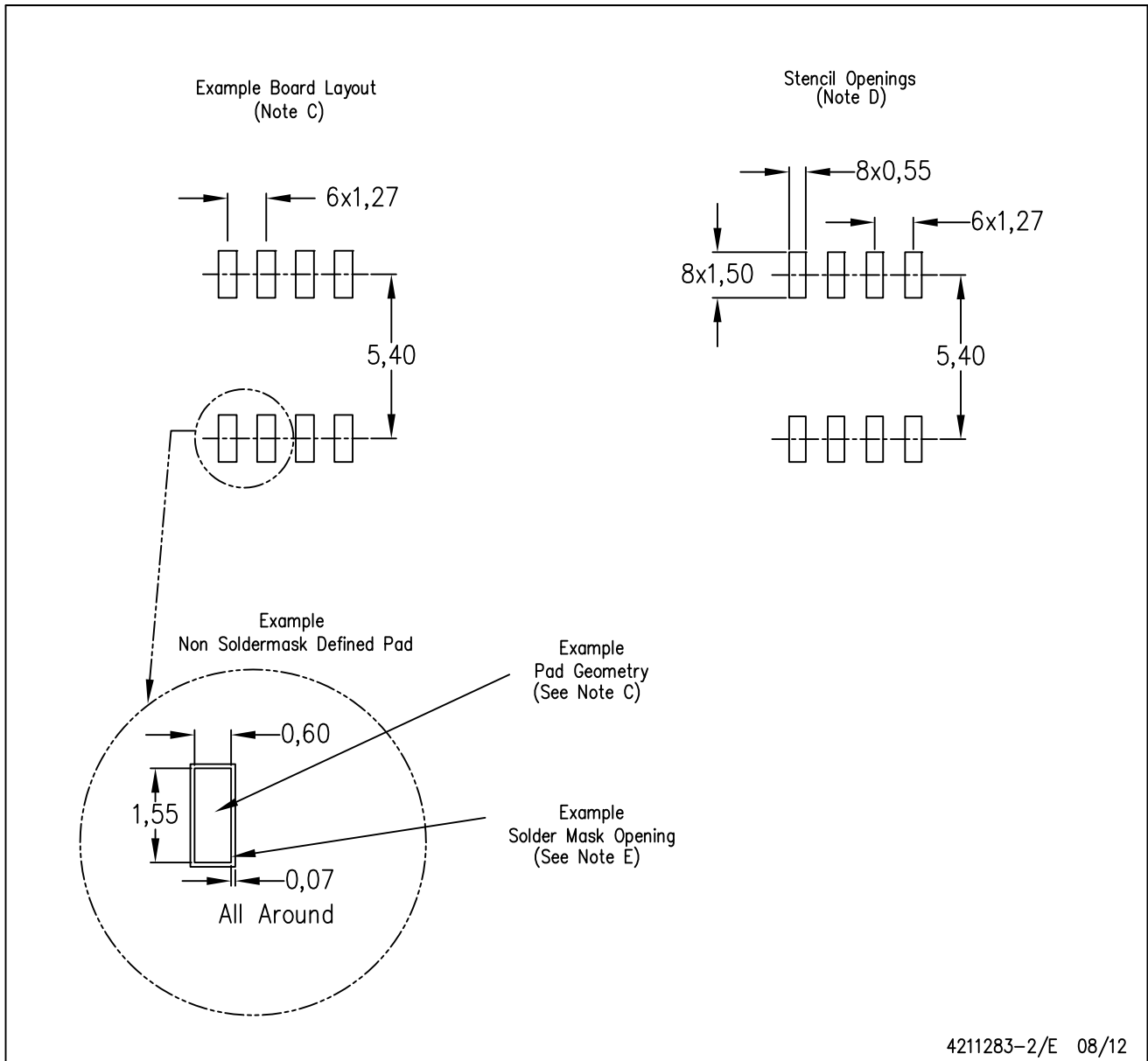
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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