July 27, 2012
Revision 2.1

LM97600RB

Reference Board Users' Guide

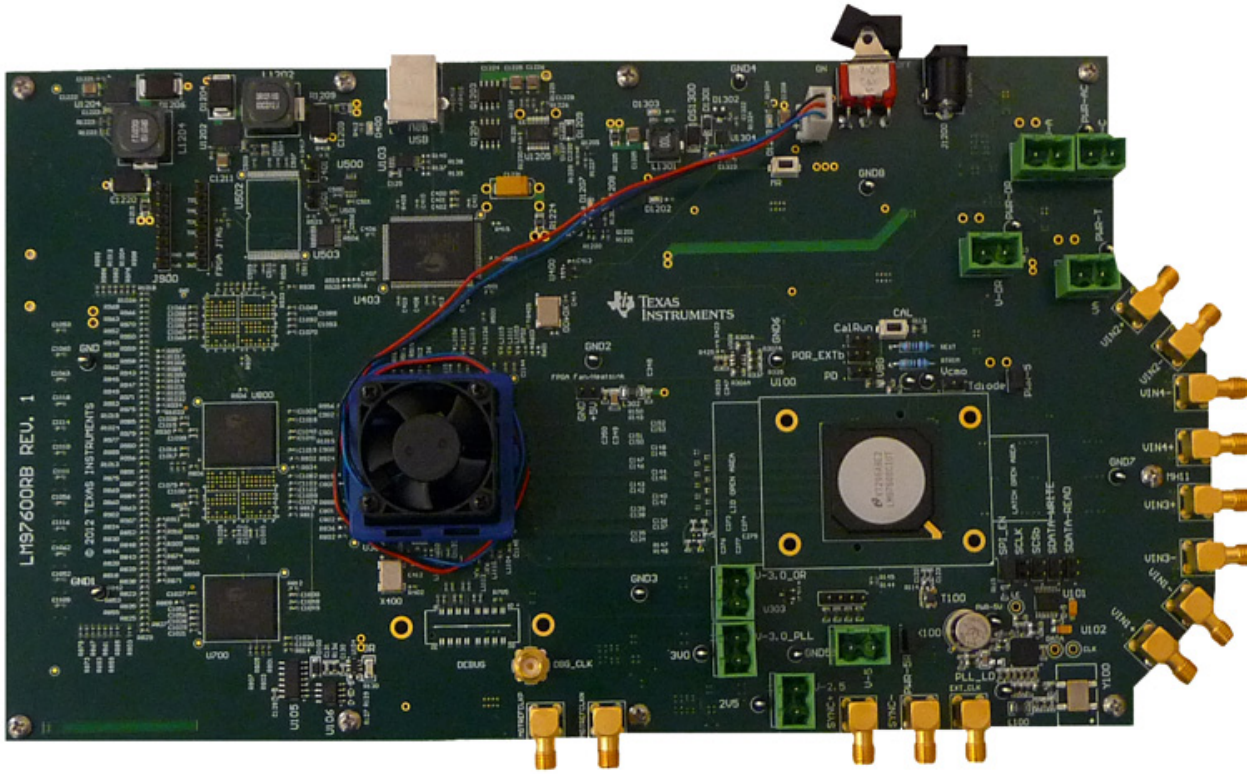


Table of Contents

Overview

The LM97600RB demonstrates a high-performance signal acquisition sub-system that provides an average output word size of 7.6 bits, and corresponding SNR and dynamic range on one to four channels at signal frequencies in excess of 1.0 GHz. Sampling rates of up to 1.25 GSPS on 4 inputs, 2.5 GSPS on 2 inputs, or 5.0 GSPS on 1 input are possible. The board showcases the following Texas Instruments devices:

- **LM97600** analog-to-digital converter
- **LMX2531LQ2570E** clock synthesizer
- **LP3878MR-ADJ** linear LDO regulators
- **LM2738YMY** switching regulators

In addition, the board also employs the **Xilinx XC5VFX70T-3FF1136C Virtex-5** FPGA for the critical function of capturing the high-speed digital data sourced by the ADC.

Features

- Demonstrates the LM97600's typical dynamic performance – see the datasheet for full details.
- Quad channel sample rates of up to 1.25 GS/s (limited by the ADC specifications and the FPGA capture limitations)
- Dual channel sample rates of up to 2.5 GS/s (limited by the ADC specifications and the FPGA capture limitations)
- Single channel sample rates of up to 5.0 GS/s (limited by the ADC specifications and the FPGA capture limitations)
- Large on-board memory for deep captures
- On-board LMX2531 based clock circuit with a connector for a selectable external clock
- A complete high-performance low-noise power management section for the ADC, clock circuit, FPGA and USB controller
- Single +12V power adapter input
- Simplicity and performance of USB 2.0 connection to the PC
- Functions with TI's latest WaveVision 5 signal-path control and analysis software

Packing List

The LM97600RB kit consists of the following components:

- LM97600RB Board
- Documentation on CD Including
  - LM97600RB Users Guide (this document)
  - Wavevision 5 Software
  - LM97600RB schematic & layout
  - LM97600RB bill of materials
  - FPGA source code

  Hardware Kit Including
  - 110V-240V AC to +12V DC Power Adapter
  - USB cable
  - 4 – DC blocks
  - 1 – Anaren balun board (useful bandwidth of 400 MHz to 3 GHz)
  - 1 – Mini-Circuits balun board (useful bandwidth of 4.5 MHz to 3 GHz)
  - 4 – 6" SMA cables

References

- *LM97600 datasheet
- *LMX2531 datasheet

*Note: Please refer to www.ti.com for the latest edition of all datasheets / application notes.

Board Overview

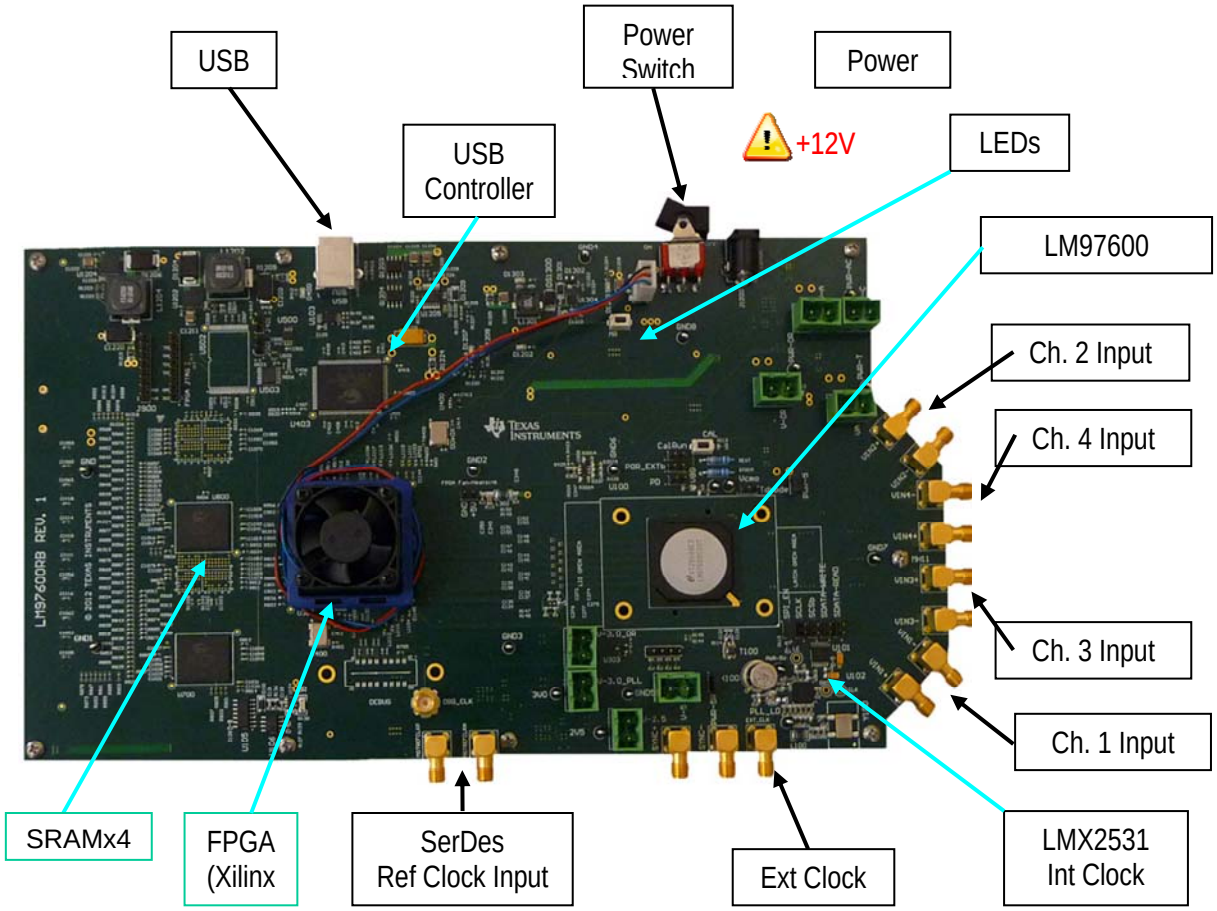


Figure 1: LM97600RB Board Layout

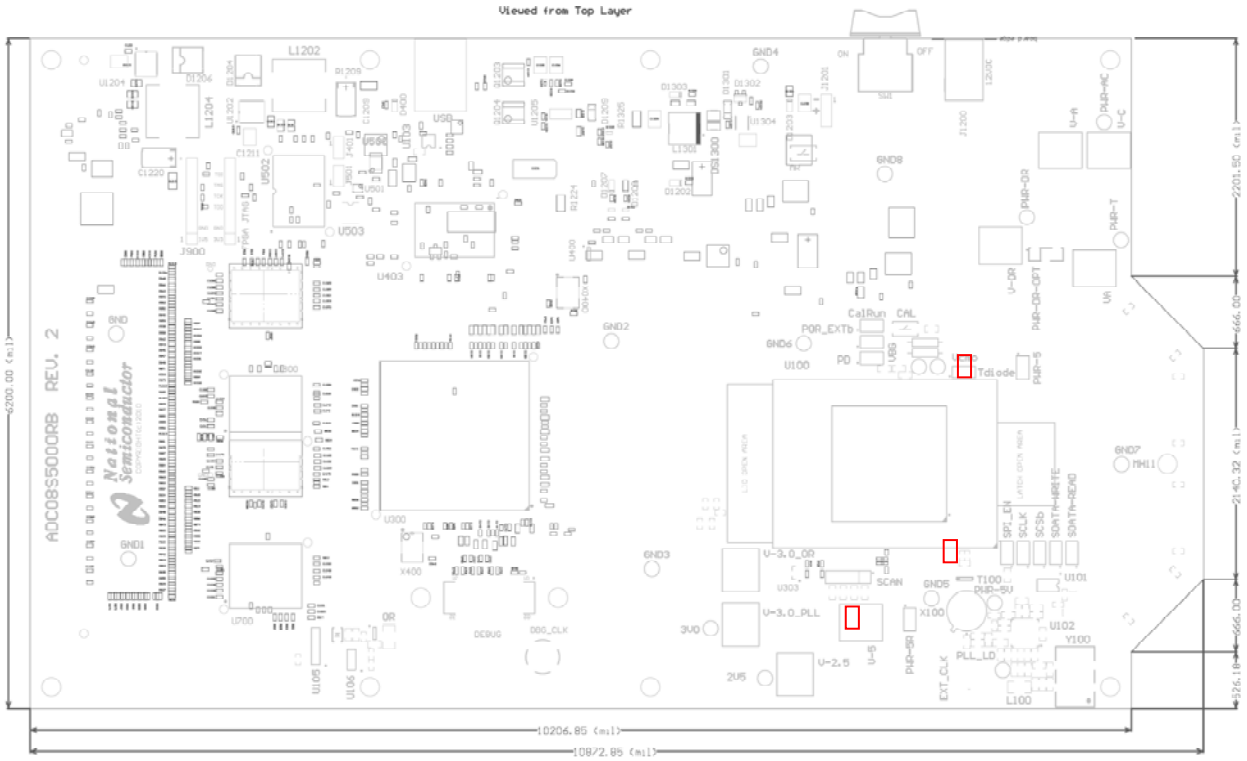


Figure 2: Jumpers and LEDs

Installed Jumpers

Shorting jacks should be installed in the following locations for the default board configuration:

- PWR-5
- SPI_EN
- PWR-5R

Quick Start

This section will aid in bringing up the board for the first time as well as a brief tutorial on the WaveVision 5 (WV5) software. Further description of the Reference Board is in subsequent sections of this document. The software is further described in the WaveVision 5 Users' Guide or the HELP function within the software. The LM97600 and LMX2531 datasheets should be consulted for detailed understanding of device functionality.

The user is advised to construct a lab setup as close to the one shown in Figure 3 as possible. This setup, along with the board and software configuration described below, is what was used to test the reference board at TI's lab. The objective is to assure that the user can achieve the same performance as that recorded at TI's lab prior to board shipment.

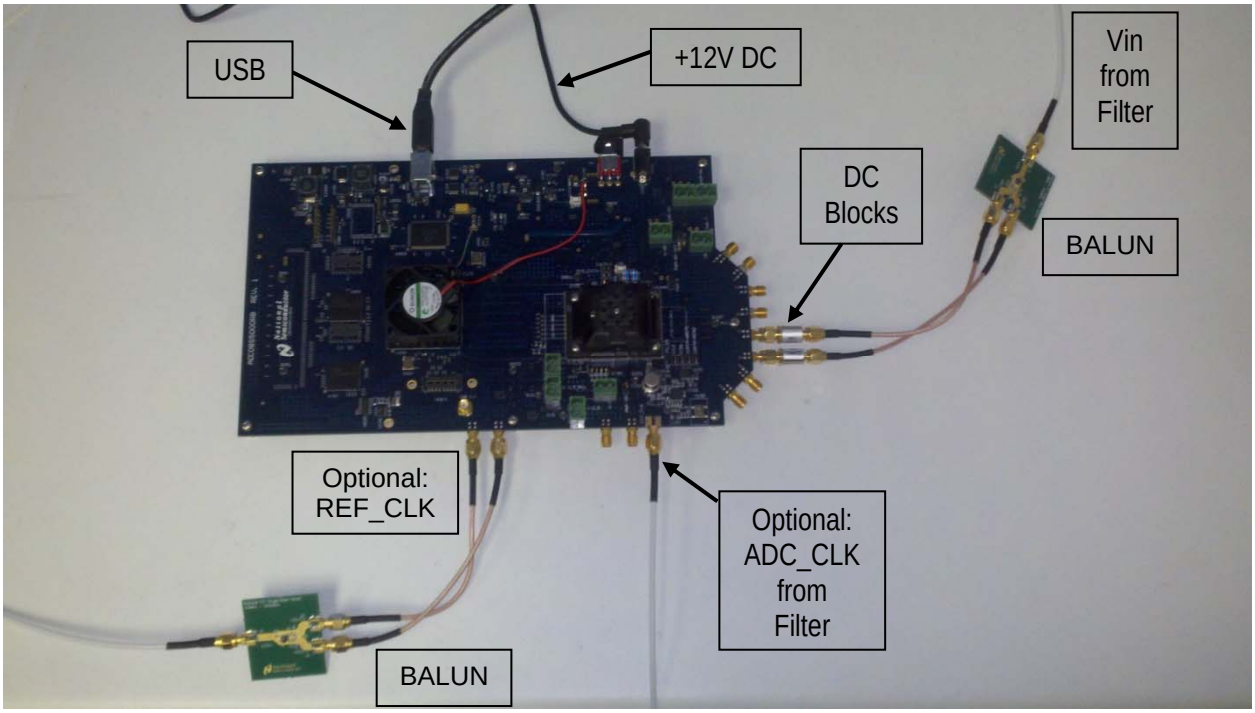


Figure 3: Recommended lab setup for on-board clock mode. A filter may not be necessary on the clock if the generator is very clean (beyond -80dBm SFDR).

Installing the WaveVision 5 Software

(Note: The WaveVision 5 software requires Windows XP 32-bit operating system)

1. Insert the included WaveVision 5 CD-ROM into the computer CD drive.
2. Locate the "install.bat" file in the Software Installation folder on the CD-ROM. Double click this file to install the software.
3. Follow the on-screen instructions to complete the installation using the default file/folder locations.

Installing the LM97600RB Hardware

1. Place the LM97600RB Reference Board on a clean, static-free surface.
2. Make sure the board's jumpers are configured as shown in Figure 2:
3. Connect the enclosed +12V DC power adapter to the power jack. Connect the other side of the power supply to an AC outlet (100-240 VAC, 50-60 Hz).
4. Connect the input signal generator, the band-pass filter, the balun and the DC blocks to the LM97600RB Reference Board's input connectors. Set the signal generator at one of the frequencies and signal levels stated in the reference performance report. Always use high-quality RF SMA cables for optimum performance.

Do not overdrive the signal and clock inputs as the ADC may be damaged. Refer to the Electrical Specification section of the datasheet for the voltage tolerance of these inputs. Including insertion loss from filters, baluns, cables, DC blocks, etc. input power should not exceed operating limits as found in the datasheet.

5. In the TI lab, the following (or equivalent performance) equipment are used to test the board. It is essential that the customer use signal generators, filters, DC blocks and a balun of equivalent or better performance.
    - Rohde & Schwarz SML03, SME-03 or SMA-100 signal generator
    - Filters - Trilithic 5VF 5% tunable bandpass filter or other fixed frequency bandpass filter of equivalent performance
    - Balun – Mini-Circuits or Anaren Balun Board
    - DC blocks – Mini Circuits BLK-89 S+

    Note: The board comes equipped with DC-blocks, to be applied to the signal input connectors. These must be used at all times - that is, the channel being used must be connected through dc-blocks if the ADC is configured for ac-coupled operation (as shipped). This is graphically illustrated in Figure 3.
6. Turn on the rocker power switch. Verify that the green LEDs (labeled D1203 and D1303) are illuminated.
7. Connect the supplied USB 2.0 cable from the PC USB port to the LM97600RB USB jack.
8. At this point, the driver for the board will be installed. Follow the instructions to install the software automatically, but without connecting to the internet. Once the driver has been successfully installed, proceed to the next step.

Launch the WaveVision 5 Software.

Start the WaveVision 5 software on your computer by selecting the desktop icon "WaveVision 5" or by clicking on the Start button, and selecting

`Programs -> WaveVision 5 -> WaveVision 5`

The software will automatically detect the board and load the appropriate software profile and will proceed to download the controller firmware and FPGA code onto the reference board. Be patient, as it takes approximately 20-30 seconds to load the FPGA code. As an alternative, the icon on the desktop

can be used to launch WaveVision 5. Once the FPGA is loaded and configured, additional LEDs will illuminate, and the WaveVision 5 user interface will appear on the computer screen.

The status LED's should take on the following states when the system is ready for an acquisition:

Meaning of the status LED's:
D1203 On – 12V power applied, and SW1 on
D1303 On – Digital Power (SPIO_PWR_EN) Active
D1202 On – ADC Power (3V3_MEZ) Active
D1207 On – FPGA Initialized
D400 Blinking – Microcontroller Ready (will blink more slowly during repetitive captures)

WaveVision 5 - User Interface Overview

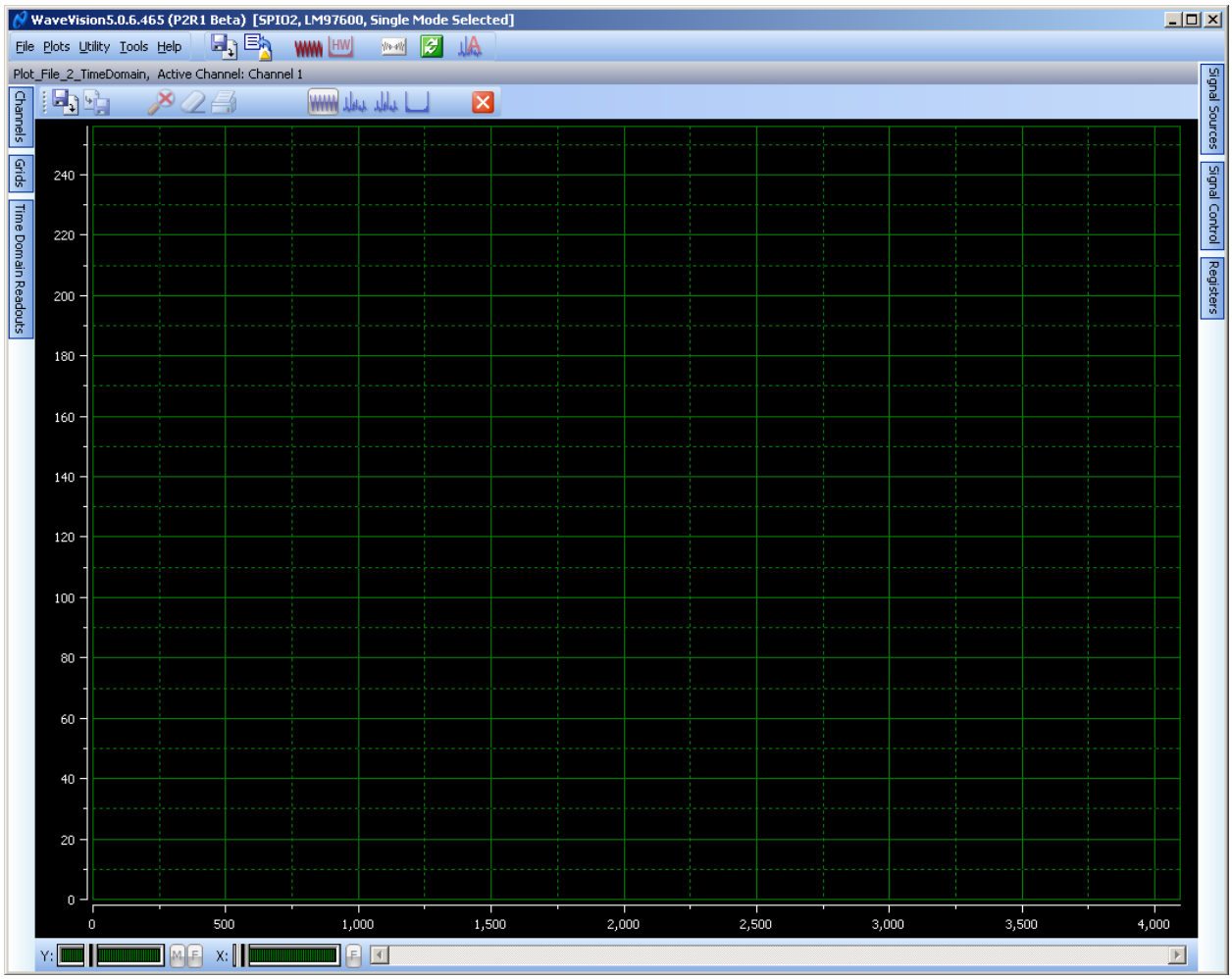


Figure 4: WaveVision 5 Example Window

Figure 4 above shows the WV5 user interface panel (GUI). This is the top level interface panel. It is arranged in such a way that the plot is always in the middle. There are tabs arranged on each side of the window to give the user additional information or control of features.

The tabs available on the **left side** access panels that are pertinent to the current plot window - such as *channel selection*, *grid selection*, *FFT Readouts*, and *FFT controls*.

The **right side** panels allow the user to take control of the hardware. These include the *Signal Source*, *Signal Control* and *Registers* panels (the most relevant for this board).

In addition, a small FFT parameter summary box can be displayed by pressing CTL-R.

For more details on the general operation and use of WaveVision 5, please refer to the **WaveVision 5 Users Guide**.

System / Device Configuration

Prior to capturing data, confirm that the board is in the "ECE (Extended Control Enable)" mode, The ECE jumper is located in the ADC pin control jumper area as shown in Figure 2. The board should be sent with this jumper in place. This means that the ADC will be controlled through the SPI interface and not with jumpers driving the control pins. This allows the user to control the ADC's behavior through the WaveVision 5 Registers panel.

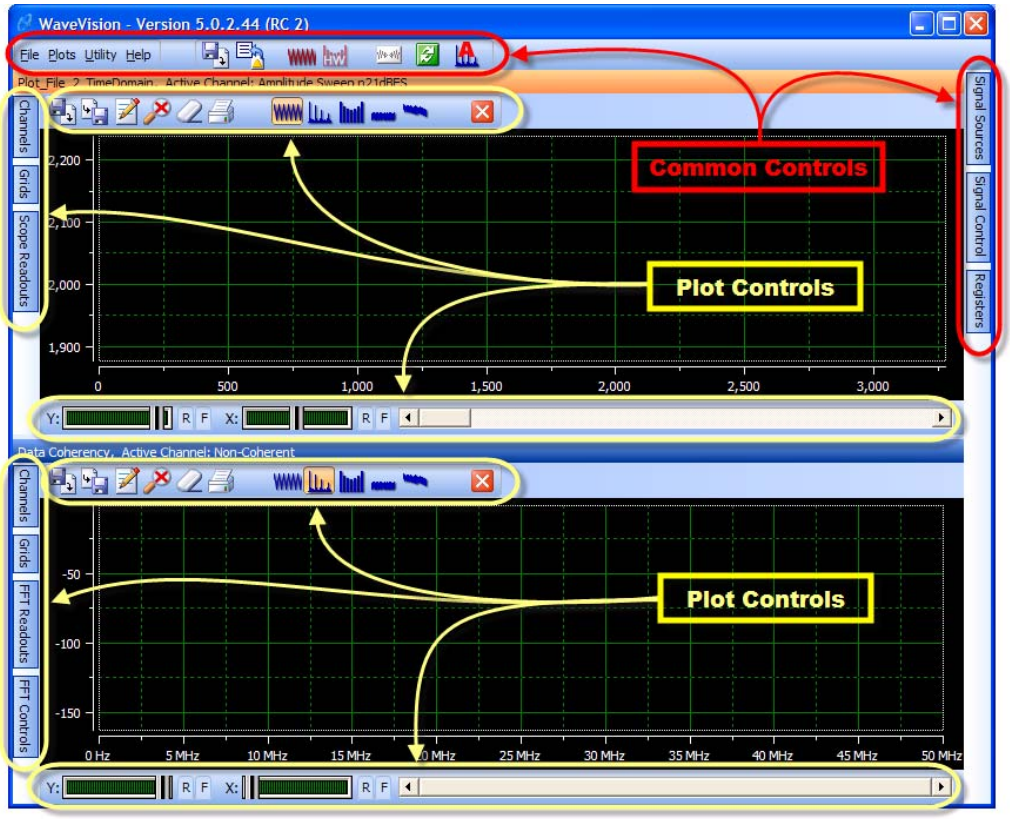


Figure 5: WaveVision 5 overview of control buttons

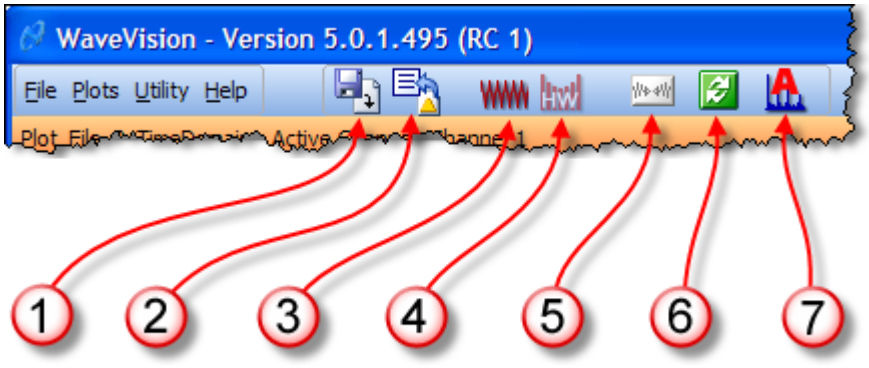


Figure 6: WaveVision 5 main window command buttons

Main Panel

The main menu bar of the WaveVision 5 software has several control buttons as shown in Figures 5 and 6, which may be used to perform most tasks with a button click.

1 - Load Plot
A new plot window is created and the Plot Load dialog is displayed. The selected plot file is loaded into the new window.

2 - Import Data
Clicking this button creates a new time-domain plot and opens the Import Data dialog. Data may be imported from WaveVision 4 data files as well as from ASCII data files created by other programs.

3 - Create a New Time Domain Plot
Clicking this button creates a new time-domain plot. The plot will contain no data, but is available as a data destination.

4 - Create a New Hardware Histogram Plot
Clicking this button creates a new hardware histogram plot. Hardware histograms are available only in conjunction with evaluation boards which can gather histogram data internally. This button is enabled only when an evaluation board which supports hardware histograms is attached.

5 - Acquire Data
Click this button to acquire data to the active plot. If you have created more than one plot, the Active plot has a highlighted title bar.

6 - Continuous Acquisition
This button is a toggle - when it is pressed, data is acquired continuously, one buffer after another as fast as the hardware can go; when pressed again data acquisition stops. When in continuous acquisition mode, acquisition may be started and stopped using the Acquire button without leaving the continuous acquisition mode.

7 - FFT Averaging
This button is also a toggle - when it is pressed, FFT's are averaged. The number of buffers to be averaged is specified in the hardware section of the Signal Sources tab.

Please refer to the **WaveVision 5 Users Guide** for more information.

Plot Window Controls

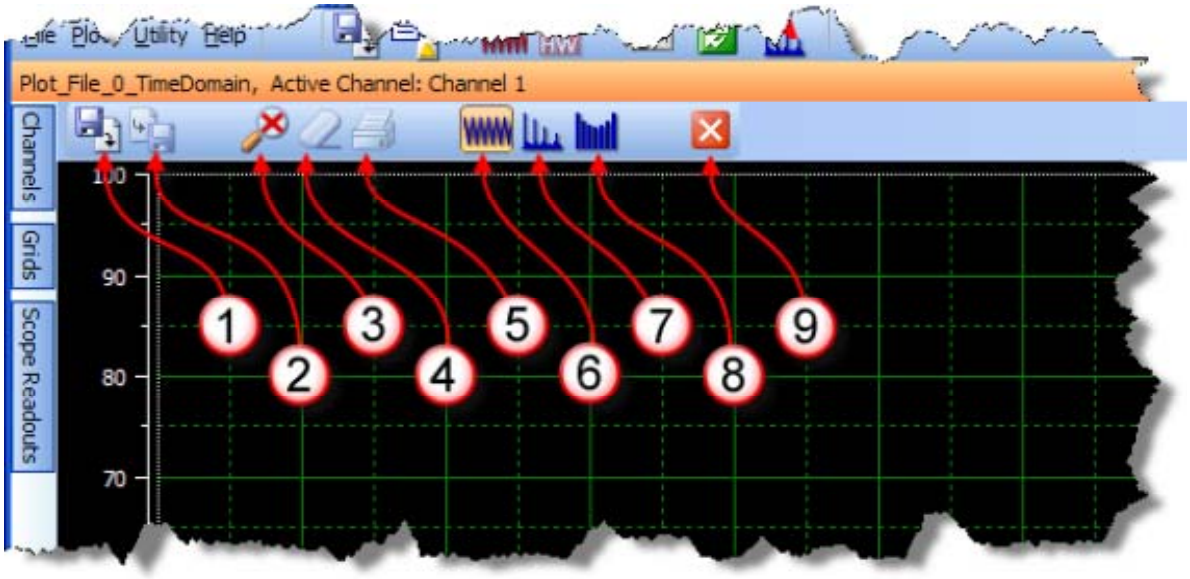


Figure 7: WaveVision 5 plot window controls

1 - Load Plot
The Plot Load dialog is displayed, and the selected plot file is loaded into the new window.

2 - Save Plot
Displays the Plot Save dialog (this button is only active when the plot contains one or more channels with data).

3 - Reset Zoom
Reset X and Y axis zoom to 100%.

4 - Clear
Clear data from all channels.

5 - Print
Print the plot.

6 - Time Domain
Display the plot as time domain data.

7 - FFT
Display the plot as an FFT

8 – Histogram
Display a histogram of the data.

9 - Close
Close this plot.

Right Panels – Signal Source

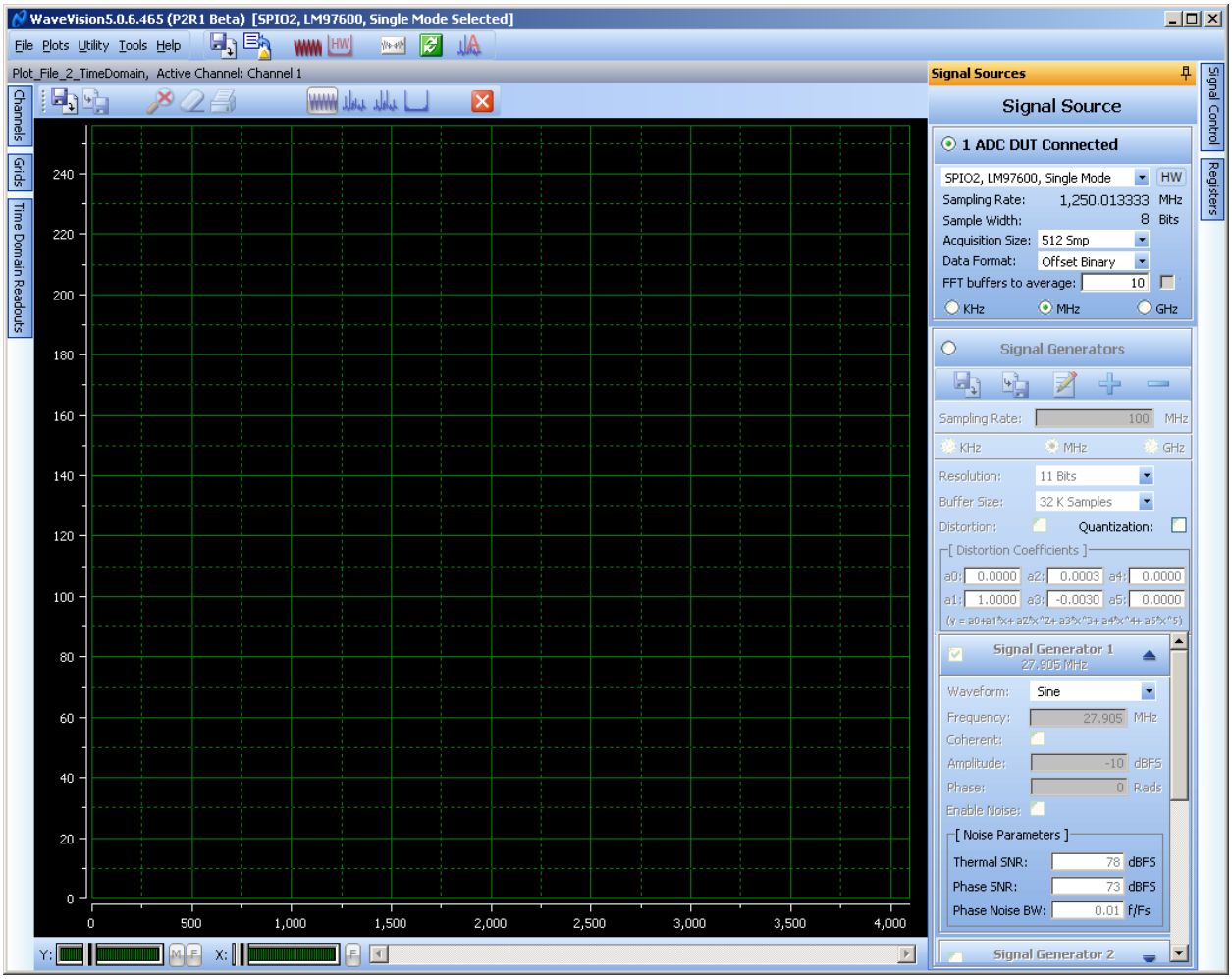


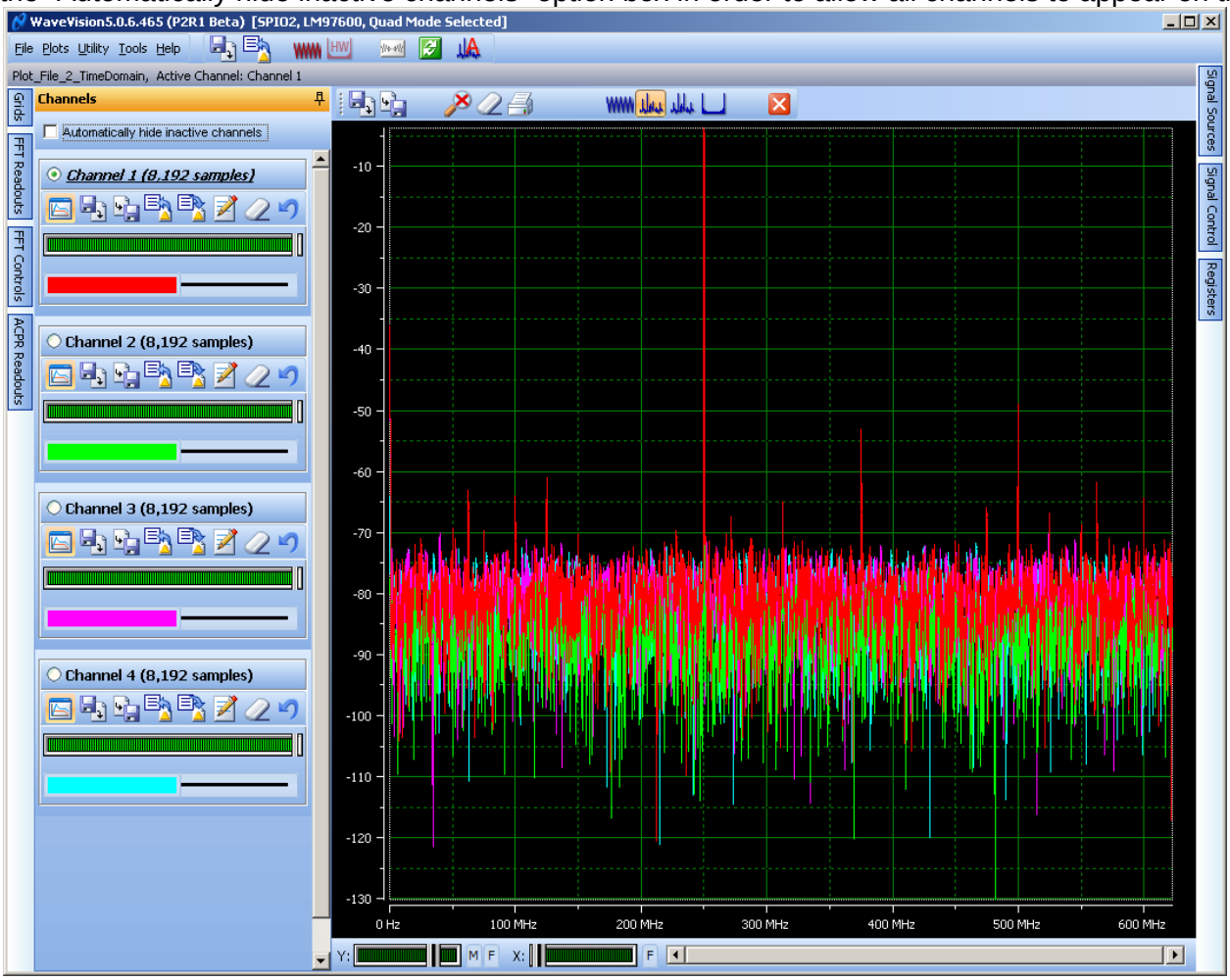
Figure 8a: WaveVision 5 main window command buttons

Open the *Signal Source* panel on the right side of the window and confirm that the LM97600RB is available and confirm that it is selected. There are seven possible modes of operation selectable here:

- Single Mode – Single Input Sampled at 2X the ADC Clock Frequency
- Dual Mode – Dual Inputs Each Sampled at 1X the ADC Clock Frequency
- Quad Mode – Quad Inputs Each Sampled at ½ the ADC Clock Frequency
- 10 Bit Raw, Lanes 0-3 – Diagnostic Mode
- 10 Bit Raw, Lanes 4-7 – Diagnostic Mode

Note: In Single, Dual and Quad modes, the selection of inputs is done using Registers Tab settings.

Note – When using Dual or Quad modes, it is also necessary to select the *Channels* tab and deselect the "Automatically hide inactive channels" option box in order to allow all channels to appear on the plot.



Alternatively, one channel may be displayed per plot:

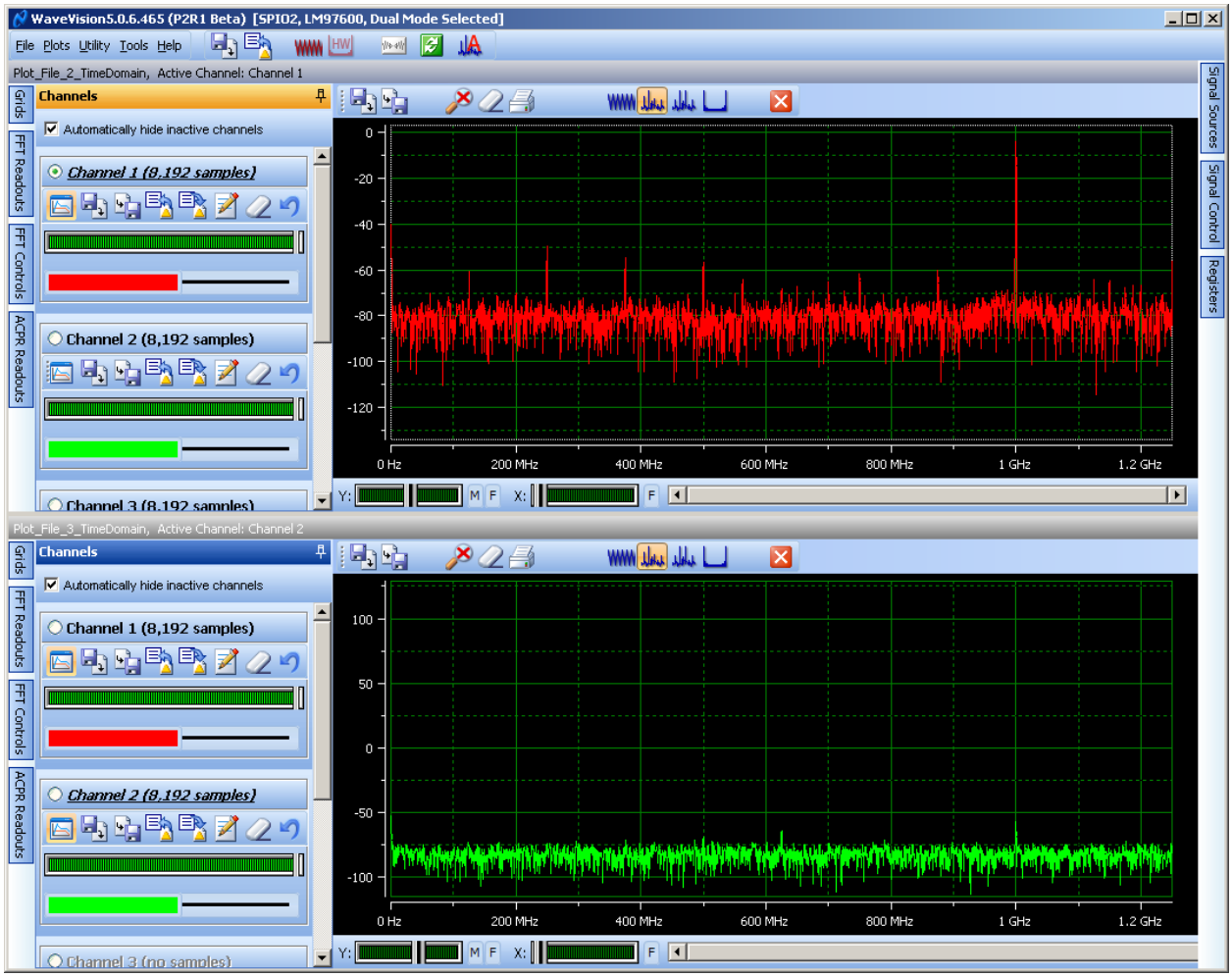


Figure 8b: Dual mode – one channel displayed per plot

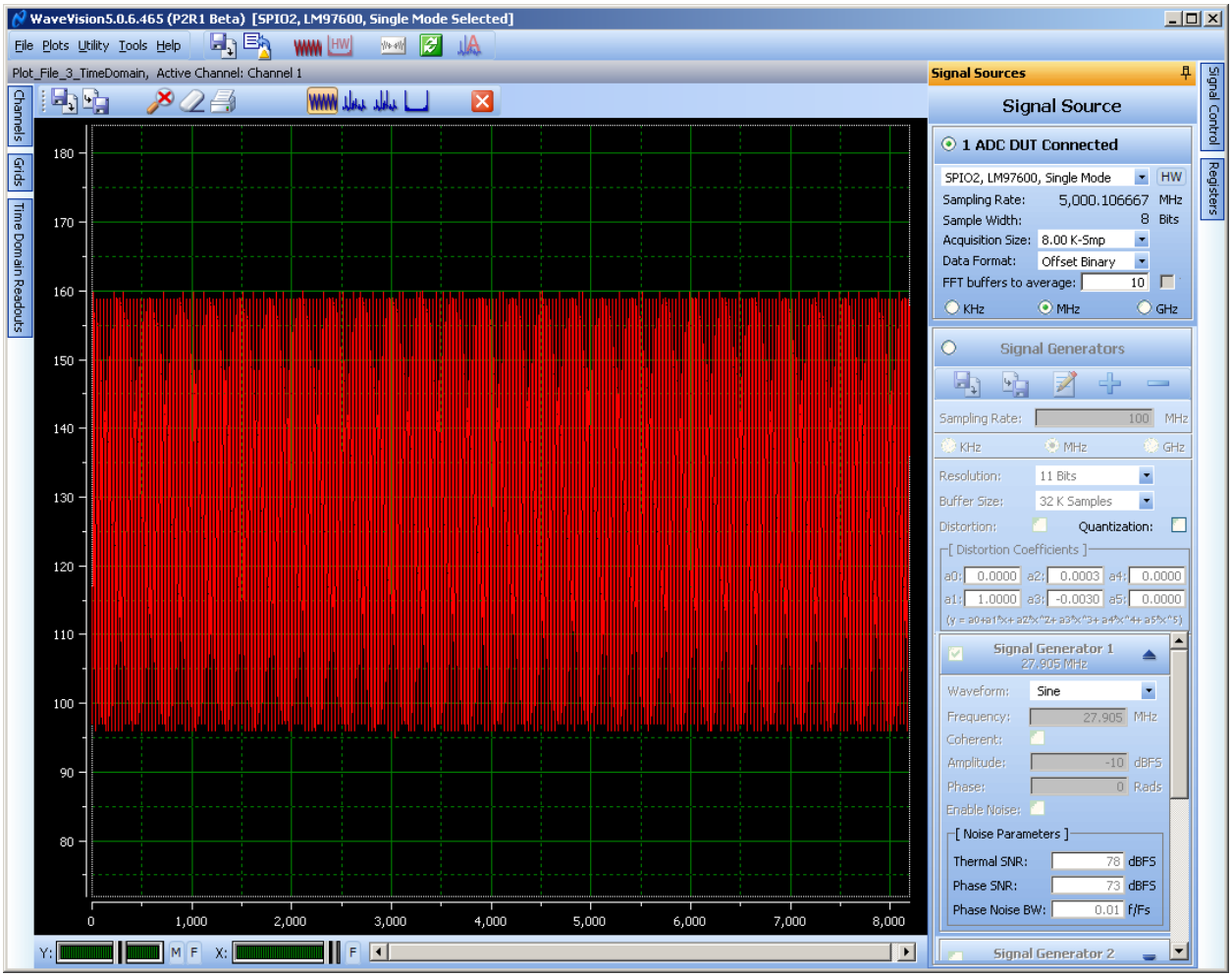


Figure 9: WaveVision 5 Signal Sources Tab Settings

- **Sampling Rate** - When the signal source panel is selected, the sampling rate is displayed. In this example, 2500 MHz is generated by the LMX2531 on the reference board. The resulting ADC sampling rate in Single Mode is 5000 MSPS. The sampling rate is determined by the FPGA when the board is powered up, with a calculation accuracy of better than 1%. If an external source is in use, confirm that this number corresponds to the clock reference that is applied. If it is not correct, subsequent data captures and display will not be correct.
- **Resolution** – This will always be set to the peak LM97600 word size which is 8 bits.
- **Acquisition Size** - This setting displays and selects the number of samples captured in each acquisition. 512 samples is the default, with valid settings up to 4M samples. **It is highly recommended to choose a setting of 8k samples or higher to provide the best FFT results.** A larger sample size increases the equivalent FFT bandwidth resolution, but at the expense of more memory and slower acquisition time.
- **Data Format** - The default data format is *offset binary* for the LM97600.
- **FFT buffers to average** - The last option is the FFT averaging function. Using this feature, subsequent samples can be averaged to obtain improved signal to noise. However, this is at the expense of time for the results to settle once changes have been made to the input signal or device settings.

Right Panels - Registers

Next, configure the hardware (including the ADC) using the Registers control panel on the right side. This is the most important of all the panels for controlling the LM97600RB.
This panel has thirteen sub-tabs that control the settings of the board and registers inside the LM97600. The thirteen sub-tabs are shown below and include; *Settings, Mode,OPEN(unused),ChA, ChB, ChC, ChD, Serial, TestPat, Dbg0, Dbg1, Dbg2, Dbg3.* The last four tabs are the raw register contents so that the user may verify register settings to be programmed in the system.

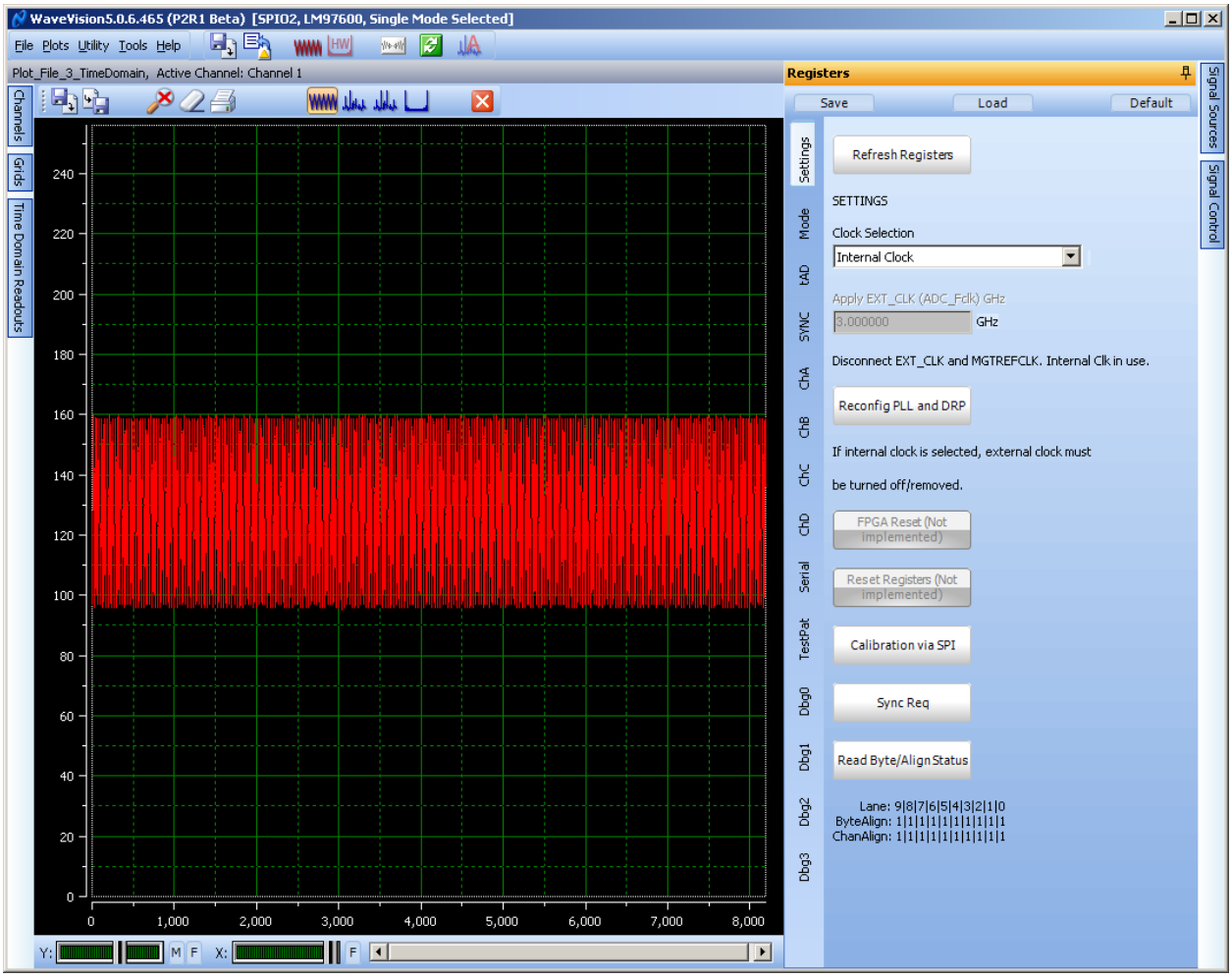


Figure 10: The top level of the Register panel showing the available tabs

The following is a short description of each tab under the ***Register*** panel.

Settings: This tab gives choice of either Internal Clock or External Clock, and buttons to initiate Reconfig PLL and DRP, Calibration via SPI, Sync Req and Read Byte/Align Status.

When switching between Internal and External clocking, and/or changing the frequency of the external clock, it is necessary to first enter the new ADC clock frequency in the entry field. This action will cause the MGTREFCLK to be recalculated. This is the frequency that must be applied to the FPGA REF_CLK inputs and is 1/12.5 of the ADC clock applied. Once the proper clock frequencies are applied, click the Reconfig PLL and DRP button followed by the Sync Req button. These actions reconfigure the GTX

receivers in the FPGA for the new data rate. After this procedure is done the ByteAlign and ChanAlign status information should be all ones as shown in the example above. If 0s are present, then some lanes have failed Byte or Channel alignment, and the ADC data captured by the FPGA will not be valid.

When switching back to Internal Clock, change the selection to Internal Clock, then click the Reconfig PLL and DRP button followed by the Sync Req button. At that point the External Clock signal generator should be disconnected or switched off to prevent performance degradation.

Calibration of the ADC should be performed if changes occur such as device temperature, mode changes (single channel to dual channel or quad channel), etc. For more information, refer to the Calibration section of the LM97600 datasheet.

Mode: This tab configures various features and modes of the LM97600 and is shown below. It accesses or changes the following functions, all of which are controlled through Configuration Register 1.

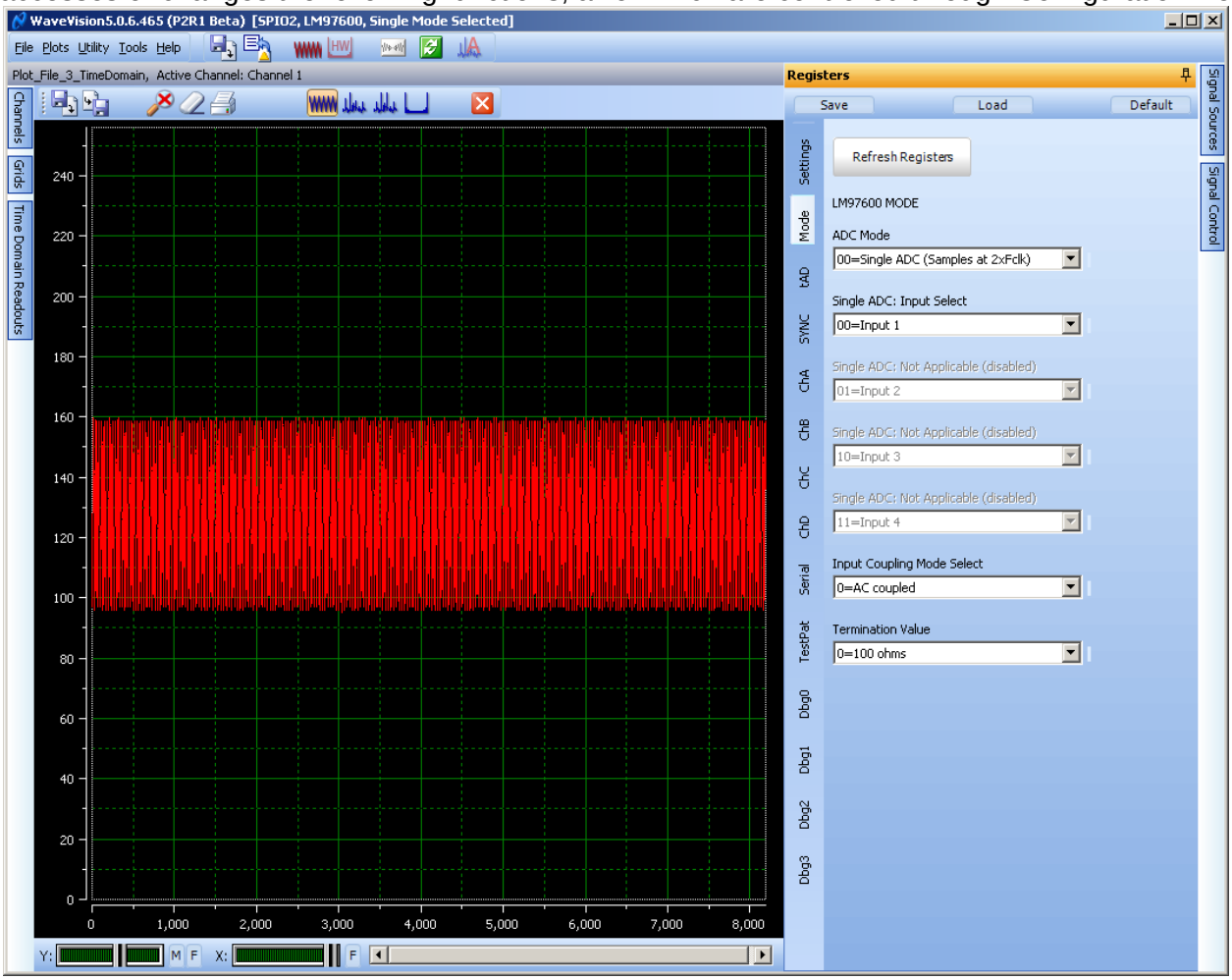


Figure 11: Mode Panel

- **Refresh Registers** – This button reads all register values from the ADC and updates form fields accordingly
- **ADC Mode** – This pull-down sets the ADC to Single, Dual or Quad operating mode.
  - In Single Mode, one selected input is sampled by all internal converters.
  - In Dual Mode, any two selected inputs can be sampled by the internal converter groups.
  - In Quad Mode, any 4 selected inputs can be sampled by the internal converters.
  - The choice of Input to Converter mapping is made with the next four fields as applicable for the set ADC Mode.
- **Input Select 1** – Selects input for Single, Dual or Quad modes.
- **Input Select 2** – Selects inputs for Dual or Quad modes.
- **Input Select 3** – Selects inputs for Quad modes.
- **Input Select 4** – Selects inputs for Quad modes.
- **Input Coupling Mode Select** – This setting configures the inputs for AC coupled or DC coupled mode of operation. In AC coupled mode, it is important to use DC blocks on the signal inputs. For DC coupled mode, the Vcmo voltage should be used to set the common mode voltage of the applied signal.
- **Termination Value Select** – Sets the signal input and clock input termination value targets to either 100 or 150 ohms. These targets are used when calibrating the input termination values.

Note: Register values are written as soon as the new selection is made.

tAD: This tab configures the Aperture Delay Enable/Disable and Adjustments which are controlled through a bit in Configuration Register 1 and several fields within the Aperture Delay register.

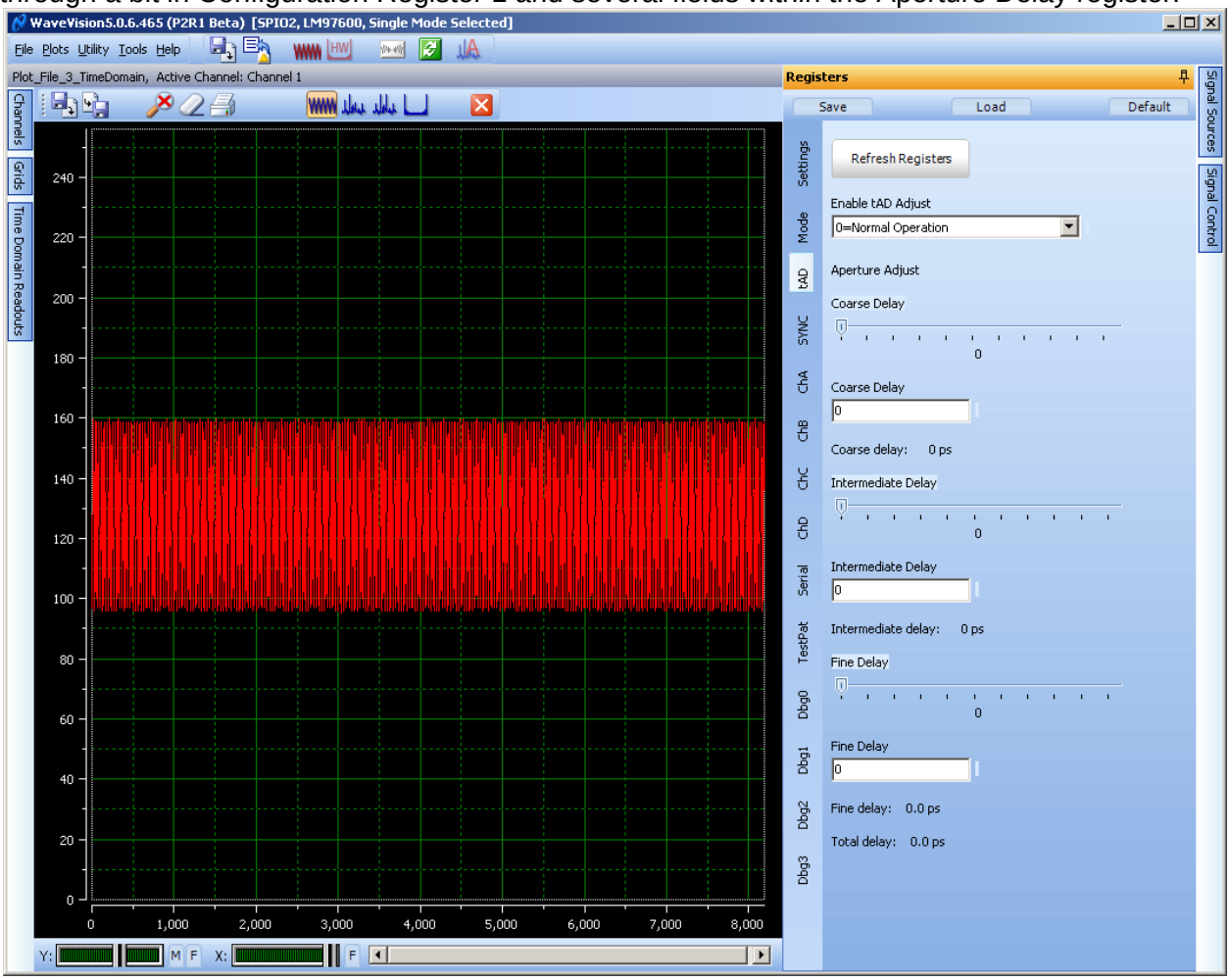


Figure 12: tAD Panel

- **Refresh Registers** – This button reads all register values from the ADC and updates form fields accordingly
- **Enable Tad Adjust** – Enables the aperture delay function**. Note:** Enabling and disabling the aperture delay adjustment causes a step change in the output data clock phase. This change is sufficient to upset the serial data interface. Once the feature has been enabled or disabled, click the Sync Req button on the settings tab to re-initialize the link.
- **Coarse Delay** –This slider and entry box allow the coarse aperture delay adjustment to be set as desired. **Note:** Because this adjustment causes a step in the delay of all device output clocks, it can only be adjusted in small steps without affecting the serial data interface. If too large a change is made, it will be necessary to re-initialize the serial data interface by clicking the Sync Req button on the Settings tab.
- **Intermediate Delay** –This slider and entry box allow the intermediate aperture delay adjustment to be set as desired.
- **Fine Delay** –This slider and entry box allow the fine aperture delay adjustment to be set as desired.

Note: Register values are written as soon as the new selection is made.

SYNC: This tab configures the device synchronization features which are controlled through a bit in Configuration Register 1 and several fields within the SYNC register.

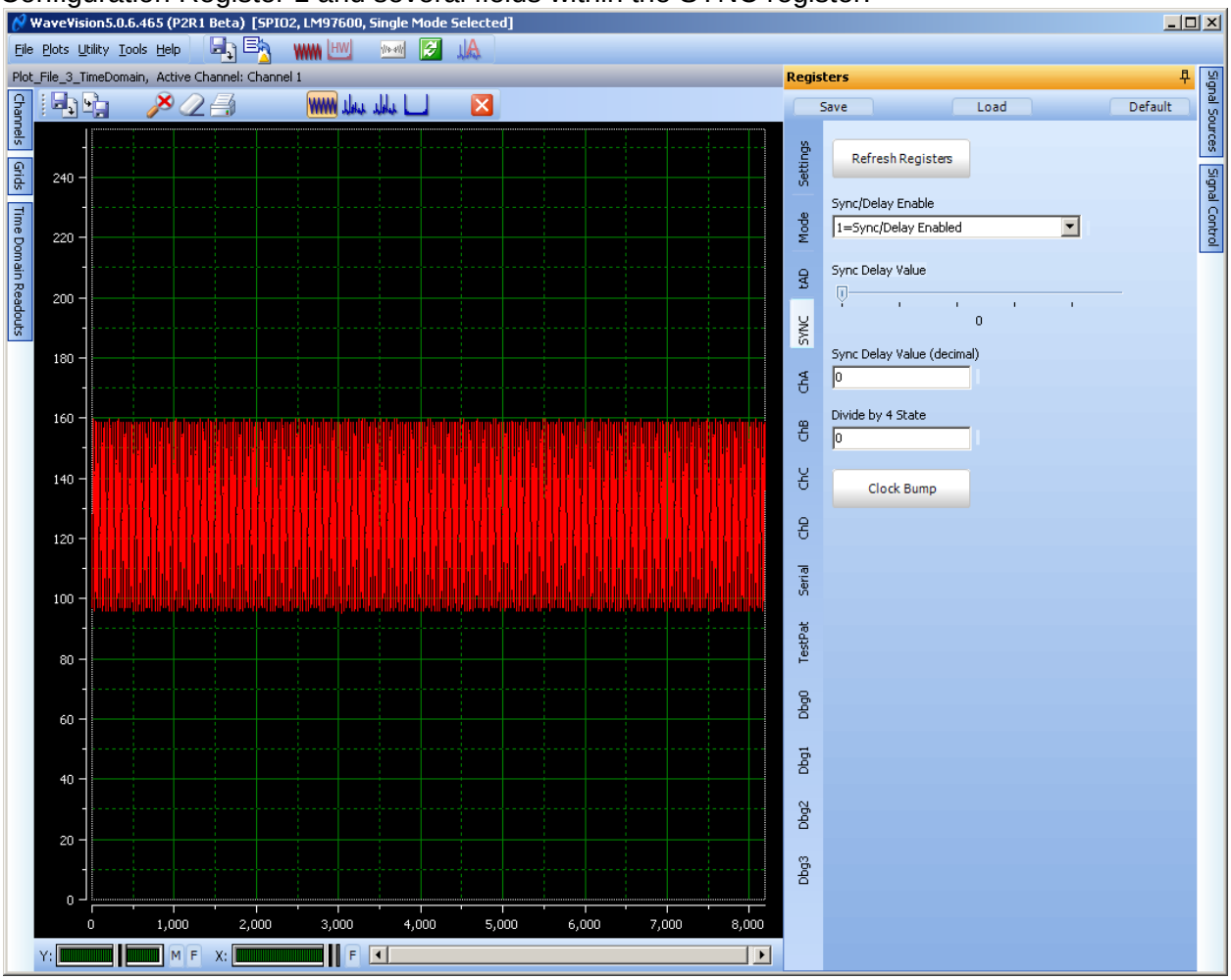


Figure 13: SYNC Panel

- **Refresh Registers** – This button reads all register values from the ADC and updates form fields accordingly
- **Sync/Delay Enabled** – This enables or disables the serializer training pattern and multi-ADC sync features of the LM97600.
- **Sync Delay Value** – This slider and entry box adjusts the Sync Delay Value.
- **Divide by 4 State** – This text box displays the Divide by 4 State bits. These bits indicate the state of the internal divide by 4 clock circuit when the SYNC input signal was captured by the rising edge of the ADC Clock input.
- **Bump** – Sets and then clears the clock bump bit. This sequence causes the internal divide by 4 clock circuit to ignore one ADC Clock rising edge, enabling the divide by 4 circuits of multiple LM97600 in a system to be synchronized.

Note: Register values are written as soon as the new selection is made.

ChA: This tab controls the Full Scale Range and Offset adjustments for Channel A.

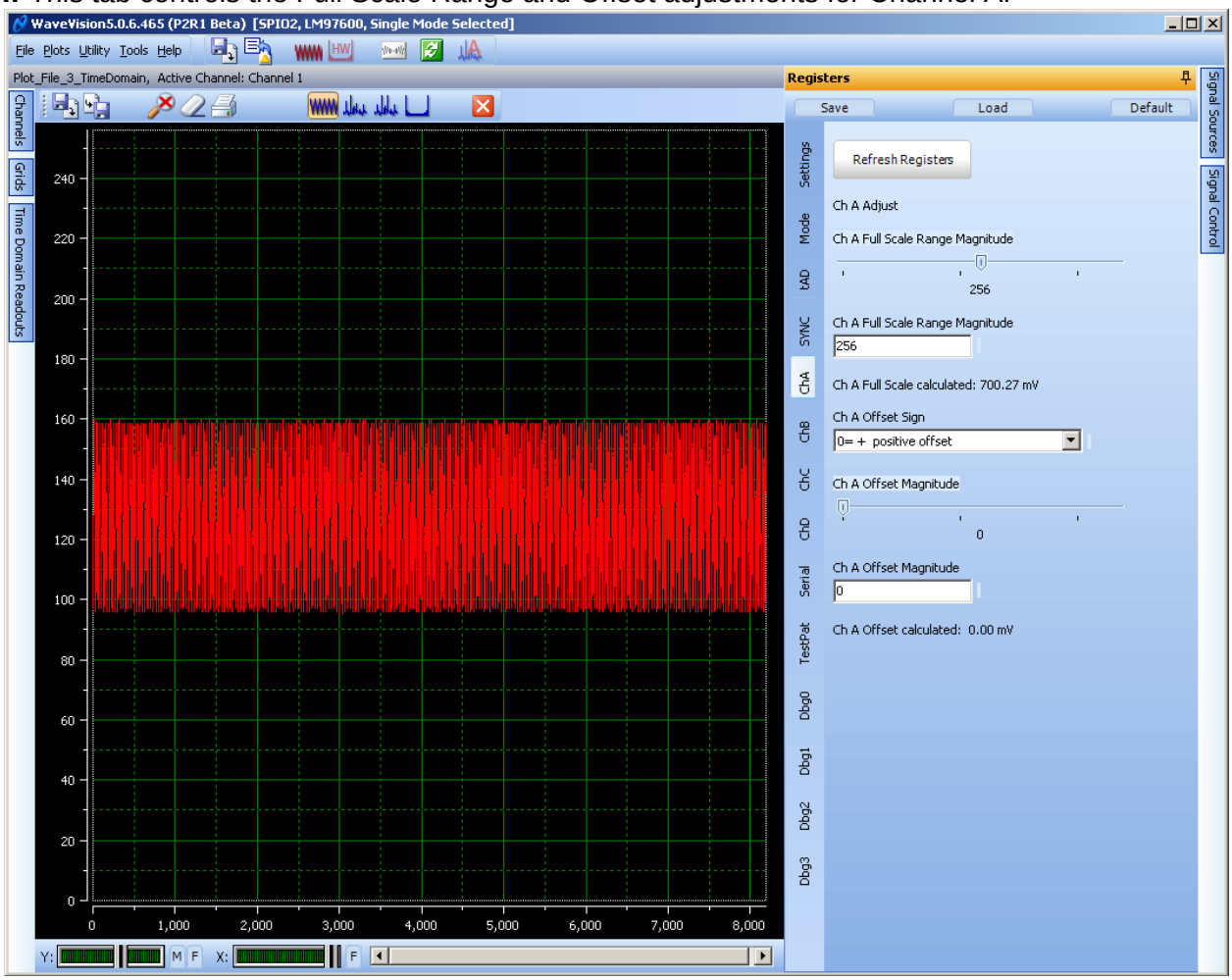


Figure 14: ChA Adjust Panel

- **Ch A Full Scale Range Magnitude** – Sets the full scale range of ADC Channel A. Settings of 0 to 511 give an approximate FSR of 560 mVp-p to 840 mVp-p.
- **Ch A Offset Sign** – Sets the sign of the offset adjustment applied.
- **Ch A Offset Magnitude** – Sets the magnitude of the offset adjustment applied. Settings of 0 to 511 give an approximate offset adjustment of 0 to 45 mV.

Note: Register values are written as soon as the new selection is made. The ADC should be re-calibrated after significant changes to the Full Scale Range have been made.

The following 3 tabs perform equivalent functions for the B, C and D internal converters.

Serial: This tab controls the settings for the serial interface.

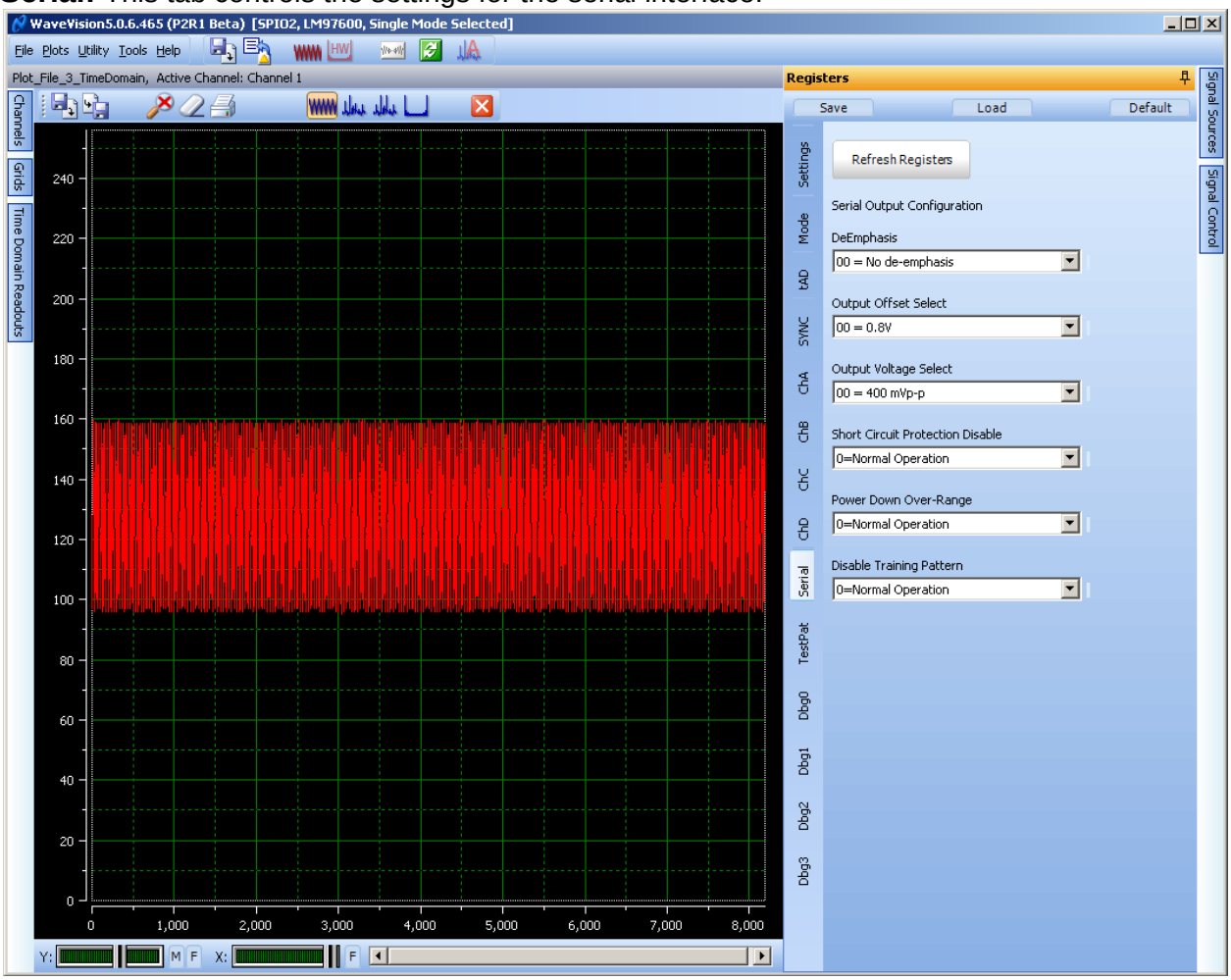


Figure 15: Serial Panel

- **DeEmphasis** – Selects the serial output de-emphasis.
- **Output Offset Select** – Selects the output offset (common mode) voltage.
- **Output Voltage Select** – Selects the output differential voltage.
- **Short Circuit Protection Disable** – Disables the output Short Circuit Protection Features.
- **Power Down Over-Range** – Disables the OverRange output pairs.
- **Disable Training Pattern** – Disables the serializer output training pattern when the SYNC+/- input is asserted. Useful when checking the Div/4 counter state without re-initializing the serial interface.

Note: Register values are written as soon as the new selection is made.

TestPat: This tab controls the Test Pattern features of the device.

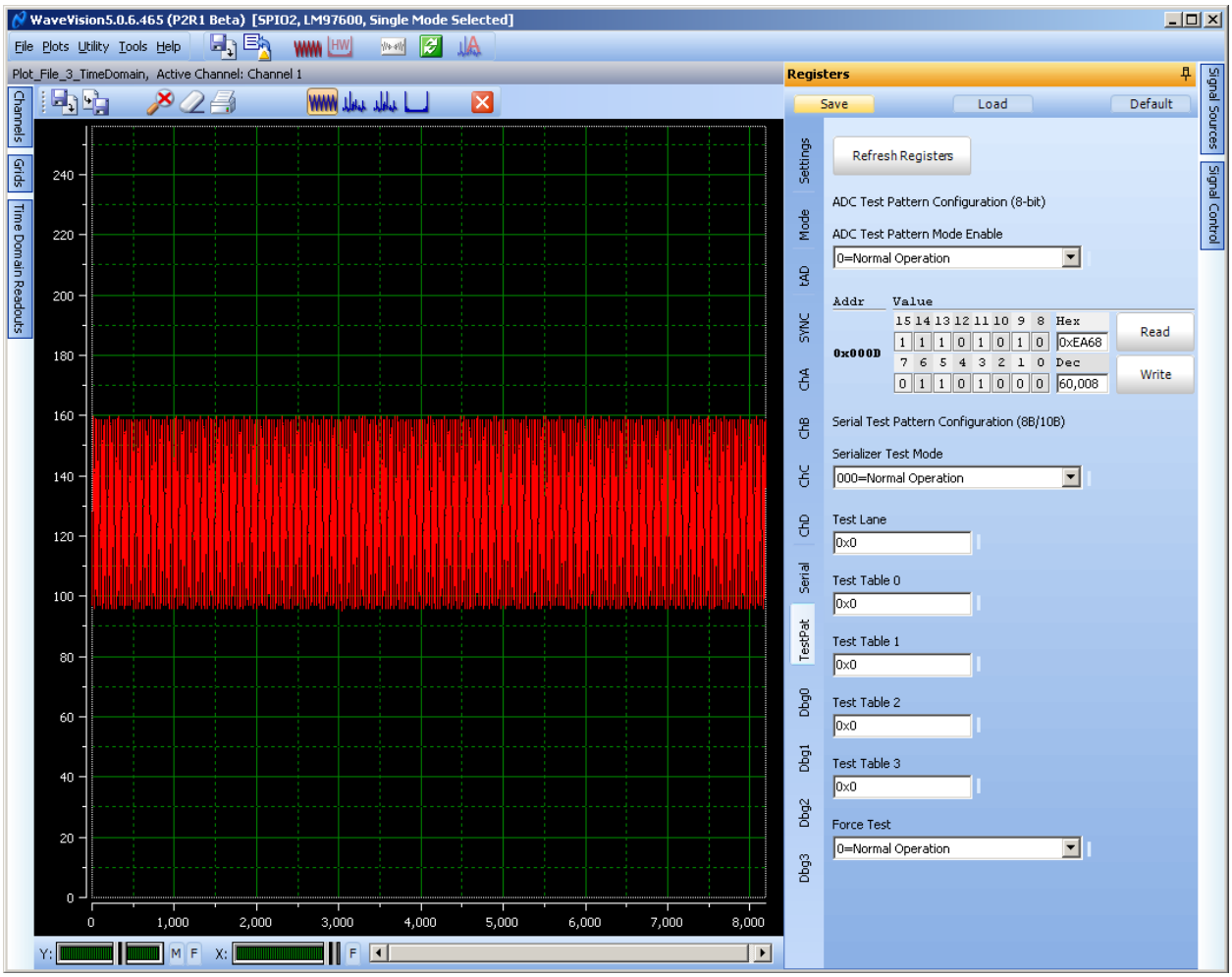


Figure 16: TestPat Adjust Panel

- **ADC Test Pattern Mode Enable** – This enables the ADC Test Pattern mode.
- **ADC Test Pattern Sequence** - This 16 bit value determines the sequence of high (1) / low (0) codes output by each ADC. Default sequence is 0xEA68 hex.
- **Serializer Test Mode** – This enables the Serializer Test Modes. Enabling these modes causes the FPGA to lose lock with the ADC data links, and are only included for diagnostic purposes.
- **Test Lane** – Sets the 10 bit test lane value.
- **Test Table 0** – Sets the 10 bit value for Test Lane 0.
- **Test Table 1** – Sets the 10 bit value for Test Lane 1.
- **Test Table 2** – Sets the 10 bit value for Test Lane 2.
- **Test Table 3** – Sets the 10 bit value for Test Lane 3.
- **Force Test** – Forces the SERDES outputs to enter Test Table mode during ADC calibration.

Note: Register values are written as soon as the new selection is made.

Debug Tabs: These panels provide the actual register settings which are conveniently formatted in the other tabs above. They may also be read to and written from and these changes will be reflected in the corresponding tabs.

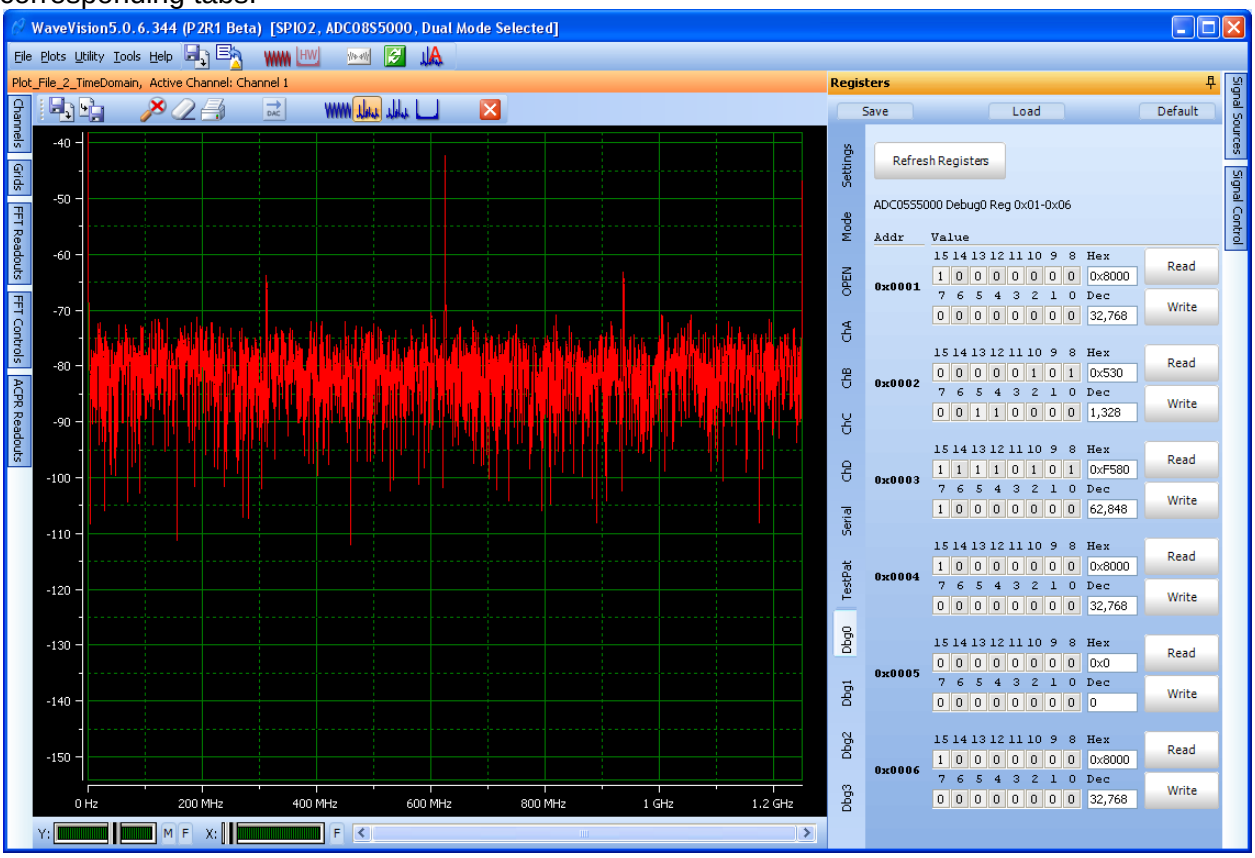


Figure 17: Debug Panels

- **Refresh Registers** – Reads back the value of all registers and populates GUI fields accordingly.
- **Read** – Reads back the individual Register value into the Binary, Hex and Dec fields.
- **Write** – Writes the modified Register value to the specific ADC register.

Note: No ADC register value changes will occur until the **Write** button is clicked.

Data Capturing

VERY IMPORTANT: Initializing the FPGA SERDES Receiver

When the board is first powered on and initialized, one additional step must be taken before capturing ADC data. The FPGA SERDES receiver is configured, but the Sync Req button on the Settings tab must be clicked one time to perform Byte and Channel alignment. After this procedure is done the ByteAlign and ChanAlign status information should be all ones.

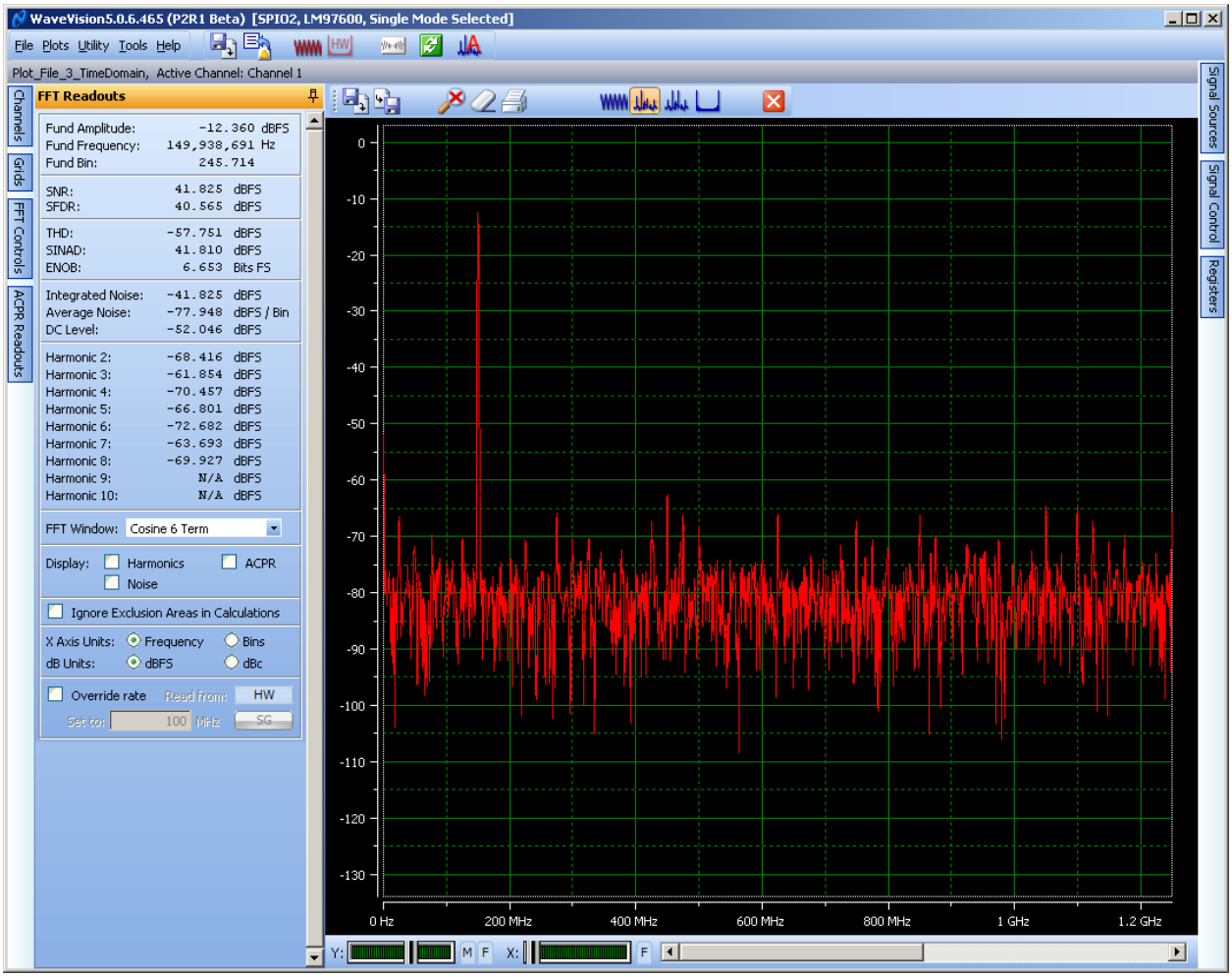
In addition, when switching between Internal and External clocking, and/or changing the frequency of the external clock, it is necessary to first enter the new ADC clock frequency in the entry field. This action will cause the MGTREFCLK to be recalculated. This is the frequency that must be applied to the FPGA REF_CLK inputs and is 1/12.5 the frequency of the ADC clock applied. Once the proper clock frequencies are applied, click the Reconfig PLL and DRP button followed by the Sync Req button. These actions reconfigure the GTX receivers in the FPGA for the new data rate. After this procedure is done the ByteAlign and ChanAlign status information should be all ones as shown in the example above. If 0s are present, then some lanes have failed Byte or Channel alignment, and the ADC data captured by the FPGA will not be valid.

When switching back to Internal Clock, change the selection to Internal Clock, then click the Reconfig PLL and DRP button followed by the Sync Req button. At that point the External Clock signal generator should be disconnected or switched off to prevent performance degradation.

The board is now ready for a data capture. Before proceeding, perform a manual calibration of the ADC. Even though the ADC performs a self-calibration at the time of power-up, it is recommended that the user perform another calibration after sufficient time has passed for the system (primarily temperature) to stabilize. Manual calibration is performed by clicking the *Calibration via SPI* button in the *Register* control panel, *Settings* sub-tab.
Once this is done, capture a single acquisition by clicking the Acquire Data button(Item 5 in Figure 6). This will capture and display a time domain acquisition in the main plot window.

Configure Display Settings

First switch from Time Domain to Frequency Domain display by clicking the FFT button (Item 7 in Figure 7).
Open the FFT Control left panel. Confirm that the *dBFS* unit is selected. Also confirm that the correct clock frequency is being measured by the software by checking in the *Signal Source* right panel.
Note: A known bug will cause temporary erroneous frequency display in Dual and Quad modes. To correct the plot display, click the Acquire Data button again and if necessary click on the zoom X-axis to full display button at the bottom of the FFT screen.



The default frequency of the on-board clock source is shown in the board performance data shipped with your board.

Check Input Amplitude

Start with an input signal amplitude that is no higher than 0 dBm. Then increase carefully while capturing data in Time or Frequency domain mode until at the desired input amplitude.

IMPORTANT: Since the ADC signal and clock inputs are not provided with additional protection circuitry on this board, the burden is on the user to not overdrive the inputs to the extent of damaging them. An "Over-range" LED is provided for each channel to indicate that the signal amplitude is beyond the ADC full-scale range. Keep the signal amplitude within the operating ratings as specified in the datasheet. Thus, the safe method of setting the signal amplitude to full-scale level is to utilize the LED as described in the previous paragraph to roughly obtain the full-scale amplitude and then inspect the captured data in the software's time-domain plot to fine tune the amplitude to the desired level.

Acquire and Display Data

Perform a data acquisition by clicking the Acquire Data button (Item #5 in Figure 6).
The acquired data will now appear in the (default) time domain plot window. Switch to the frequency-domain window (FFT) using the WaveVision 5 controls. Type Ctrl-r to obtain the summary of the acquisition. Place the software in continuous mode (Item #6 of Figure 6) and then acquire again. This is to confirm that the Over-range LED method used earlier indeed gave a signal to the ADC that is within -

0.5 to -1.0 dB of the full-scale range. If not, adjust the input signal generator's signal power to approximately -0.5dB of full scale.

At this point, dynamic performance metrics similar to those shown on the reference data shipped with the board may be obtained. One of the basic variables that you may experiment with at this point is to change the input signal strength and frequency. Please note that to achieve the reference performance, band-pass filters similar to the items referenced in Section 2.2 should be used. The absence of these filters on the input signal or external clock will usually result in sub-standard performance.

The displayed units should be in dBFS as selected earlier. You may switch the units to dBc and back to dBFS as desired.

External Clock Source

It is also possible to apply a high-quality external signal source to the clock input rather than using the on-board LMX2531 clock synthesizer. This will help quantify the LMX2531's performance in an ultra-high-speed signal-path such as this one. When connecting an external clock source, the generator amplitude should be set to +2 dBm. Experiment with the clock signal strength to determine what effect this has on the channel performance. Care should be taken to not exceed +4 dBm at the clock input, to avoid damage to the ADC.

The external clock source is enabled through the register control panel in the software after applying the signal generator to the Clock input SMA.

The external clock source should be disconnected or turned off when the on-board clock source is selected. Failure to do so will result in poor performance due to the mixing of the on-board clock and the small amount of external clock signal leaking through the clock selection relay.

It is important to keep in mind that if the ADC's operating conditions are changed in any significant way, especially temperature, the ADC should be calibrated again before proceeding.

Please refer to the WaveVision 5 Users' Guide and integral Help feature for more information concerning the software.

Secondary Panel Description

Please refer to the WaveVision 5 Users Guide for detailed descriptions of the remaining Left and Right panels, and additional Main Panel features.

System Block Diagram

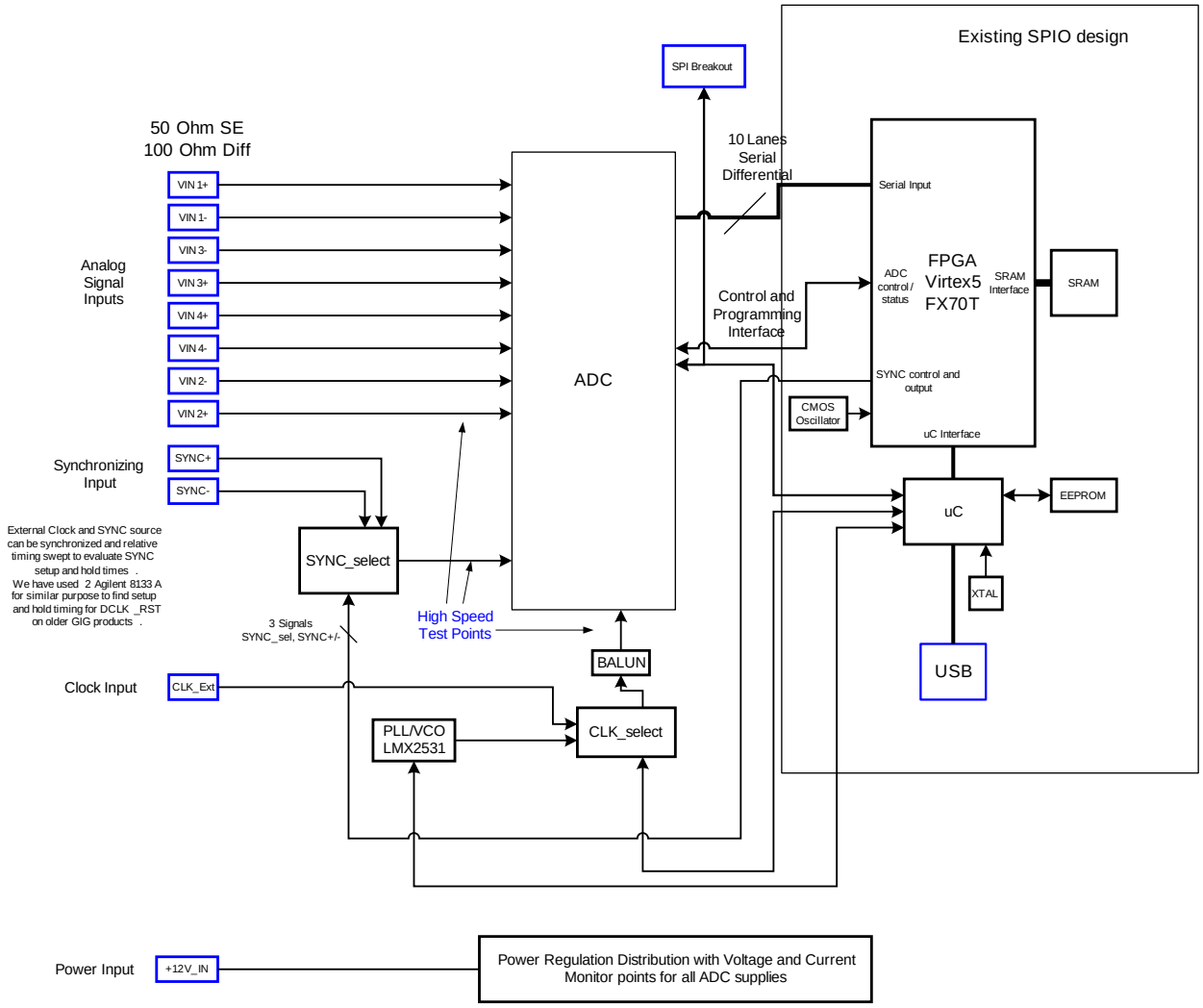


Figure 17: LM97600RB System Block Diagram

System Description

The LM97600

LM97600 forms the heart of this reference board. This low-power, high-performance CMOS analog-to-digital converter provides an average output word size of 7.6 bits at guaranteed minimum sampling rates of 1.25 GS/s in quad channel mode, 2.5 GS/s in dual channel mode and 5.0 GS/s in single channel mode. The LM97600 is targeted at achieving very good accuracy and dynamic performance while consuming the lowest power available in the industry. The product is packaged in a thermally enhanced BGA package that operates over the rated ambient temperature range of -40 degrees C to +85 degrees C. Refer to the latest version of the LM97600 datasheet for more detailed information.

This reference board gives complete control over the LM97600 and gives the user direct performance results of the chip without the need for an elaborate setup.

Analog Front-End: The analog signal connection to the ADC is kept simple on this board in order to achieve the highest possible bandwidth. The board is designed to be coupled to front-end circuitry in a DC or AC coupled manner. AC-coupling requires the use of dc-blocks on the SMA connectors. The ADC is configured for AC coupled operation by default, but can be set to DC coupled mode via the WaveVision5 GUI register controls.

Multi-channel ADC synchronization: A SYNC+/- signal input is provided to synchronize the ADCs on multiple boards or systems. Please refer to the LM97600 datasheet for more details.

LMX2531 Clock Synthesis chip

The LMX2531xxxx family provides a single-chip, very low-jitter clock solution at frequencies up to 3132 MHz. In this application, the LMX2531LQ2570E is used - which can be programmed to operate over a range of frequencies. On the LM97600RB board, the device is configured for 2500 MHz through the serial interface.

The clock source for the ADC can be selected between the on-board LMX2531 or an external clock source connected through the EXT_CLK SMA connector. The selection is performed through the WV 5 register panel. It is recommended that the external clock source should be connected and enabled before it is selected. ***For optimum performance, the external clock signal generator and the LMX2531 should not be enabled at the same time.*** This is because the RF relay used to select between them does not provide adequate isolation to keep one from affecting the other. Having both clocks on simultaneously will result in excessive spurious signals. The default setting for this board is the on-board LMX2531 clock source.

FPGA

The design employs a Xilinx Virtex-5 FPGA for capturing the digital data. While the board is powered up and configured, the FPGA is continually receiving data from the ADC. In response to a user command through the WV-5 software, the ADC captures the desired amount of data in its on-chip buffer (up to a maximum of 4M samples) then uploads the captured data to the PC through the USB interface for further processing.

Please note that Texas Instruments does not provide support for any user-designed FPGA functionality beyond the standard functionality that is shipped with the board.

Electrical Specification

Power Supply:	Nominal =12V Minimum = 11.5V, Maximum = 12.5V *(Voltages outside these levels may cause damage!!)*
Power Consumption:	Nominal = 20 Watts (will reduce at lower external clock frequencies) Maximum = 22 Watts
ADC Input Signals:	Maximum Operating Voltage = see datasheet Recommended/initial (full scale) generator setting = 0 dBm *(The maximum level at the signal generator is dependent upon the insertion loss from other hardware before the ADC inputs. Care should be taken not to exceed the Operating Ratings at the ADC input.)*
Clock Input Signal:	Maximum Operating Voltage = +4 dBm Recommended generator setting = +2 dBm *(The maximum level at the signal generator is dependent upon the insertion loss from other hardware before the clock inputs. Care should be taken not to exceed the maximum limits at the clock inputs.)*
USB Port:	USB 2.0 compliant

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/ kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this is strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

REGULATORY COMPLIANCE INFORMATION (continued)

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjukku-ku, Tokyo, Japan

http://www.tij.co.jp

【ご使用にあたっての注】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree t that :

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions, It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Special Instructions. It is important to operate this EVM within the input voltage range of -0.3 V to 48 V and the output voltage range of 0.9 V to 18 V. Change this line as necessary for your User Guide.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI. Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices.

Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265