

AN-2067 LM5027A Evaluation Board

1 Introduction

The LM5027A evaluation board is designed to provide the design engineer with a fully functional power converter based on the Active Clamp Forward topology to evaluate the LM5027A controller. The evaluation board is provided in an industry standard quarter-brick footprint.

The performance of the evaluation board is:

- Input Operating Range: 36 to 78 V (100 V peak)
- Output Voltage: 3.3 V
- Output Current: 0 to 30 A
- Measured Efficiency: 90.5% @ 30 A, 92.5% @ 15 A
- Frequency of Operation: 250 kHz
- Board Size: 2.3 × 1.45 × 0.5 inches
- Load Regulation: 1%
- Line Regulation: 0.1%
- Line UVLO, Hiccup Current Limit
- A 70% Maximum Duty Cycle

The printed circuit board consists of 6 layers of 2 ounce copper on FR4 material with a total thickness of 0.050 inches. The unit is designed for continuous operation at rated load at <40°C and a minimum airflow of 200 CFM.

2 Theory of Operation

Power converters based on the Forward topology offer high efficiency and good power handling capability in applications up to several hundred watts. The operation of the transformer in a forward topology does not inherently self-reset each power switching cycle; a mechanism to reset the transformer is required. The active clamp reset mechanism is presently finding extensive use in medium level power converters in the 50 to 200 W range.

The Forward converter is derived from the Buck topology family, employing a single modulating power switch. The main difference between the topologies are, the Forward topology employs a transformer to provide input / output ground isolation and a step down or step up function.

Each cycle, the main primary switch turns on and applies the input voltage across the primary winding, which has 12 turns. The transformer secondary has 2 turns, leading to a 6:1 step-down of the input voltage. For an output voltage of 3.3 V the required duty cycle (D) of the main switch must vary from approximately 60% (low line) to 25% (high line). The LM5027A limits the PWM duty cycle output to a maximum of 70% (typical). The maximum duty cycle limits the voltage stress on the Active Clamp Forward converter MOSFETs. The clamp capacitor along with the reset switch reverse biases the transformer primary each cycle when the main switch turns off. This reverse voltage resets the transformer. The clamp capacitor voltage is $V_{in} / (1-D)$.

Feedback from the output is processed by an amplifier and reference, generating an error voltage, which is coupled back to the primary side control through an optocoupler. The LM5027A voltage mode controller pulse width modulates the error signal with a ramp signal derived from the input voltage. Deriving the ramp signal slope from the input voltage provides line feed-forward, which improves line transient rejection. The LM5027A also provides a controlled delay necessary for the reset switch. The evaluation board can be synchronized to an external clock with a recommended frequency range of 275 to 300 kHz.

3 Evaluation Board Schematic

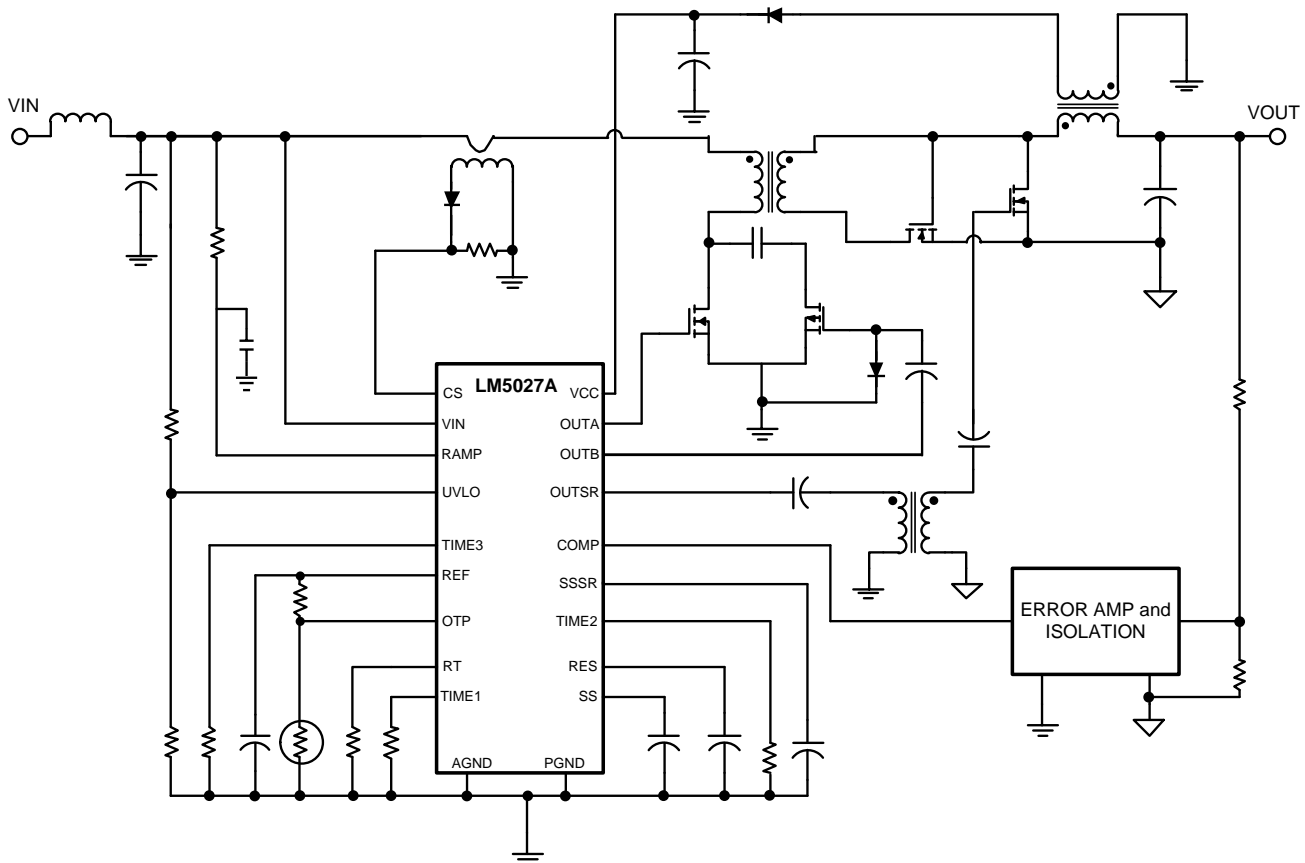


Figure 1. Evaluation Board Schematic

4 Powering and Loading Considerations

When applying power to the LM5027A evaluation board certain precautions need to be followed. A failure or misconnection can present itself in a very alarming manner.

4.1 Proper Connections

When operated at low input voltages the evaluation board can draw up to 3.5 A of current at full load. The maximum rated output current is 30 A. Be sure to choose the correct connector and wire size when attaching the source supply and the load. Monitor the current into and out of the evaluation board. Monitor the voltage directly at the output terminals of the evaluation board. The voltage drop across the load connecting wires will give inaccurate measurements; this is especially true for accurate efficiency measurements. See [Figure 2](#).

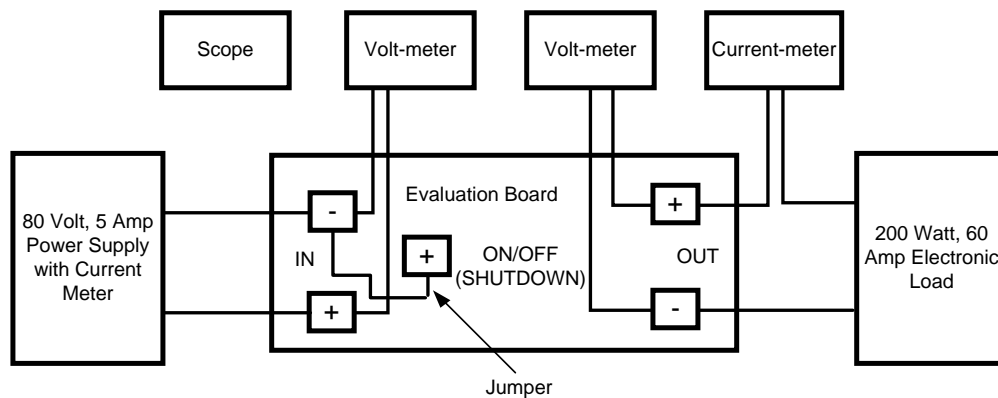


Figure 2. Typical Evaluation Setup

4.2 Source Power

The evaluation board can be viewed as a constant power load. At low input line voltage (36 V) the input current can reach 3.5 A, while at high input line voltage (78 V) the input current will be approximately 1.5 A. Therefore to fully test the LM5027A evaluation board a DC power supply capable of at least 80 V and 4 A is required. The power supply must have adjustments for both voltage and current. An accurate readout of output current is desirable since the current is not subject to loss in the cables as voltage is. The power supply and cabling must present a low impedance to the evaluation board. Insufficient cabling or a high impedance power supply will droop during power supply application with the evaluation board inrush current. If large enough, this droop will cause a chattering condition upon power up. This chattering condition is an interaction with the evaluation board undervoltage lockout, the cabling impedance and the inrush current.

4.3 Loading

An appropriate electronic load, with specified operation down to 3.0 V minimum, is desirable. The resistance of a maximum load is 0.11 Ω . You need thick cables! Consult a wire chart if needed. If resistor banks are used there are certain precautions to be taken. The wattage and current ratings must be adequate for a 30 A, 100 W supply. Monitor both current and voltage at all times. Ensure there is sufficient cooling provided for the load.

4.4 Air Flow

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4.5 Powering Up

Using the shutdown pin provided will allow powering up the source supply with the current level set low. It is suggested that the load be kept quite nominal during the first power up. Set the current limit of the source supply to provide about 1.5 times the wattage of the load. As you remove the connection from the shutdown pin to ground, immediately check for 3.3 V at the output.

A most common occurrence, that will prove unnerving, is when the current limit set on the source supply is insufficient for the load. The result is similar to having the high source impedance referred to earlier. The interaction of the source supply folding back and the evaluation board going into undervoltage shutdown will start an oscillation, or chatter, that may have highly undesirable consequences.

A quick efficiency check is the best way to confirm that everything is operating properly. If something is amiss you can be reasonably sure that it will affect the efficiency adversely. Few parameters can be incorrect in a switching power supply without creating losses and potentially damaging heat.

4.6 Over Current Protection

The evaluation board is configured with hiccup over-current protection. In the event of an output overload (approximately 33 A) the unit will discharge the soft-start capacitor, which disables the power stage. After a delay the soft-start is released. The shutdown, delay and slow recharge time of the soft-start capacitor protects the unit, especially during short circuit event where the stress is highest.

5 Start-Up

Power supplies have a soft-start circuit(s) to control their output voltage when input power is applied. The soft-start sequence limits the peak inrush current as the output capacitors are charged, and prevents the output voltage from over-shooting. In most power supplies there are primary side and secondary side soft-start circuits.

The primary side soft-start circuit is generally in a primary side controller and the soft-start time is set with an external capacitor. The function of the primary side soft-start circuit is to slowly increasing the duty cycle of the controller from zero to the maximum duty cycle. The maximum duty cycle varies based on the controller and the circuit topology.

The secondary side soft-start circuit connects a resistor/capacitor from the secondary side voltage reference to the positive input of the error amplifier. The soft-start time is set by the resistor/capacitor time constant and works by ramping up the voltage reference on the secondary side error amplifier. The output of the error amplifier is fed across the isolation boundary to the primary side controller compensation input which is connected to the controller PWM input. The voltage at the compensation input increases to a value required for regulation as determined by the voltage feedback loop. The secondary side soft-start along with the primary side soft-start work together to control the duty cycle on start-up to controlling the power supplies output start-up time, and limit the stress on the power components.

Figure 3 shows the primary and secondary side soft-start sequence using the LM5027A into an electronic load. After V_{in} is applied the primary side soft-start ramps up. When the voltage on the LM5027A SS pin reached 1.0 V the output drives start and power is delivered to the secondary of the transformer. The power supply output rises and the secondary side soft-start circuit begins to ramp-up. The output of the DC-DC converter monotonically increased with no overshoot to 3.3 V out.

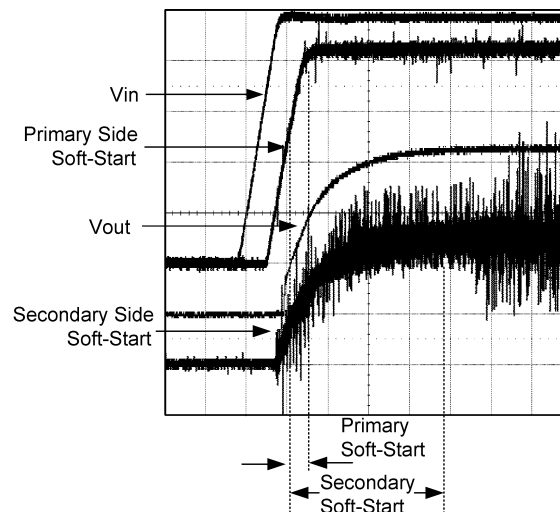


Figure 3. Soft-Start

6 Pre-Bias Load Start-Up

Figure 4 shows a typical Forward Converter topology with an active clamp using self-driven synchronous rectification. It's simple and very efficient; however there are some disadvantages when starting this topology into a pre-biased load. The first occurs because the synchronous rectification is on the secondary side of the transformer and without adding intelligence the output current will flow into the converter via the output choke and the free wheeling MOSFET when the converter starts-up or shut down with pre-bias voltage.

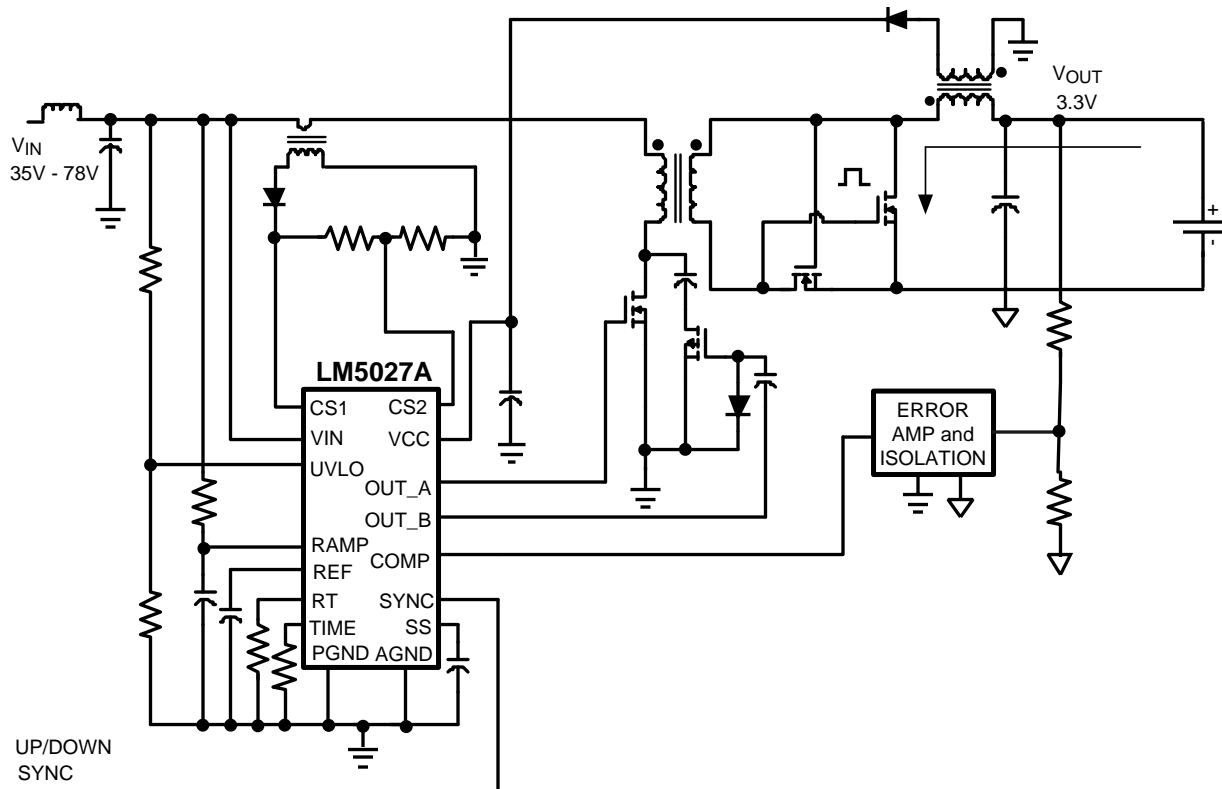


Figure 4. Typical Forward Converter

7 OUTSR Drive

The LM5027A has a dedicated pin (OUTSR) to drive the synchronous rectifier free wheeling MOSFET through a drive transformer as shown in Figure 5. When the converter starts-up, the OUTSR drive is held low and the freewheeling MOSFET is turned-off. As a result, no output current will sink into the converter. The OUTSR is enabled after the primary side soft-start reaches approximately 4.0 V. The OUTSR delay was added to ensure that the power supply output voltage is up and in regulation prior to the freewheeling MOSFET being turned-on, refer to Figure 6 and Figure 7. The OUTSR drive is soft-started; a capacitor on the SSSR pin is released and is charged with a 25 μ A current source, slowly increasing the duty cycle of the freewheeling FET's duty cycle.

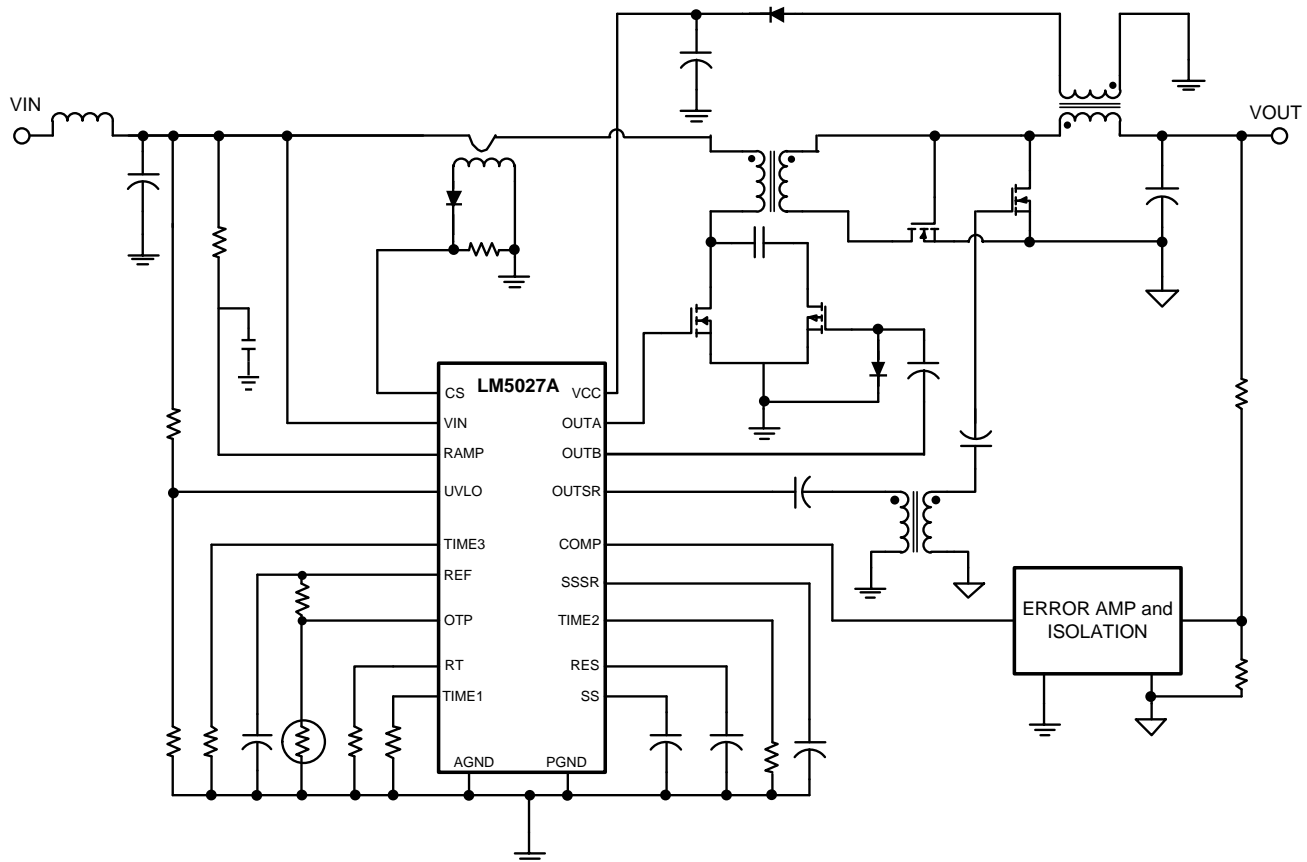


Figure 5. LM5027A Synchronous Rectifier Drive Output (OUTSR)

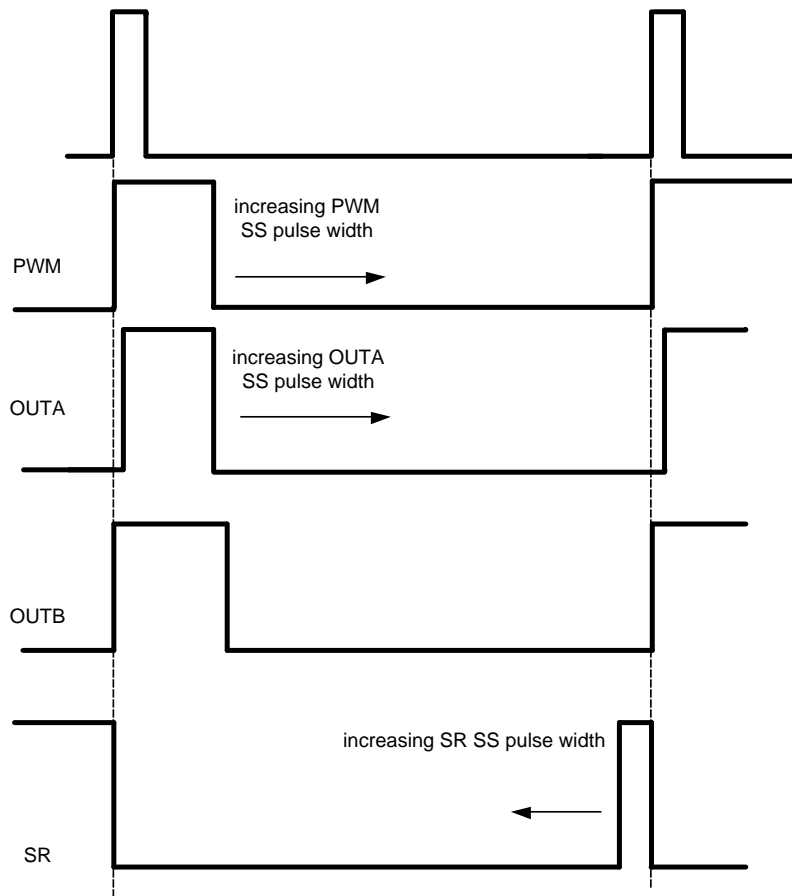


Figure 6. LM5027A Drive Timing

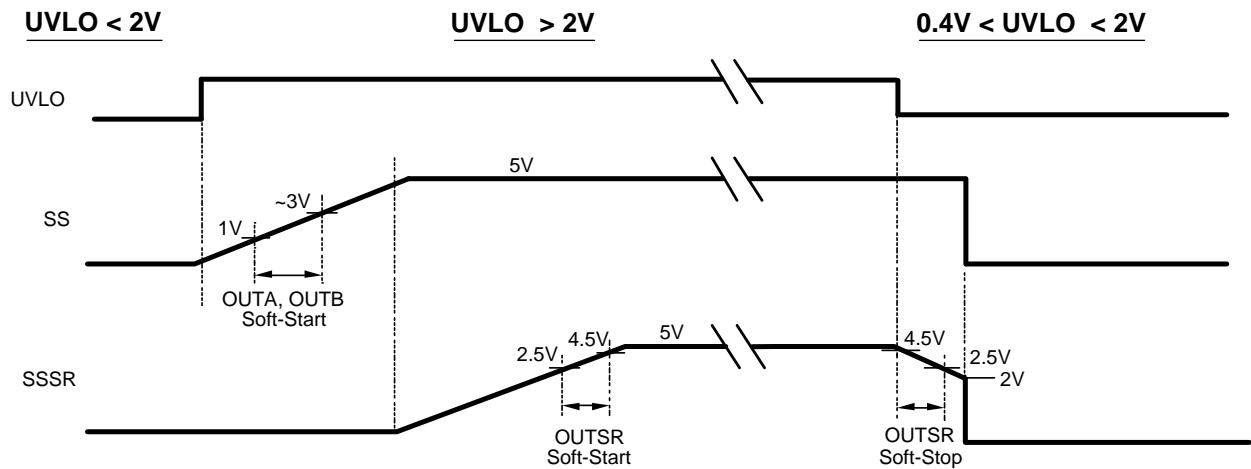


Figure 7. LM5027A Soft-Start Waveforms

8 Secondary Side Soft-Start

In a typical DC-DC converter with a 3.3 V output the voltage reference for the error amplifier is 1.2 V. Prior to the power supply being turned-on and if there is a pre-bias load, the secondary side soft-start capacitor (CSS) will be pre-charged to the voltage reference level of 1.2 V (if the pre-bias load > 1.2 V), refer to Figure 8. On start-up the primary side soft-start begins and the output voltage rises from the pre-bias voltage level to 3.3 V, refer to Figure 9. At the end of the primary side soft-start period the controller will be at maximum duty cycle and the output voltage will overshoot until the feedback error amplifier has a chance to respond and reduce the output voltage to the regulation set point.

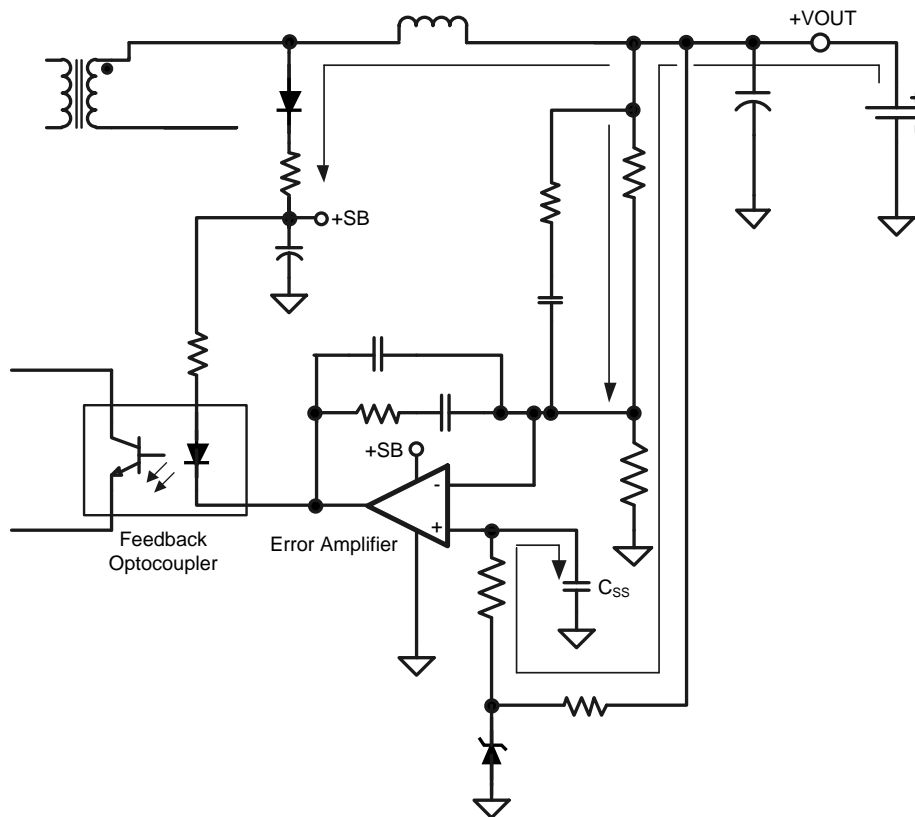


Figure 8. V_{REF} with Pre-Bias Load

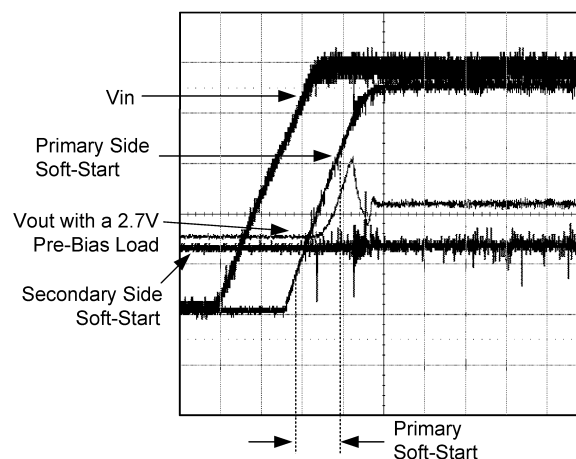


Figure 9. Pre-Bias Secondary Side Soft-Start

9 Secondary Side Soft-Start Reset

When input power is supplied to the LM5027A Evaluation Board the LM5027A's internal VCC Regulator turns-on providing power to the VCC pin, the primary side soft-start voltage increases, and the output drives are enabled. When the drive outputs are enabled the voltage on the transformer secondary increases, the Secondary Bias rises supplying voltage to the reference and error amplifier, refer to Figure 10. During this time FET Q1 is turned-on holding the reference voltage at the positive input to the error amplifier low (zero volts). When the voltage on the secondary bias capacitor (C_{BIAS}) rises above the Zener diode > 3.6 V, the Secondary Bias Power Good (the collector of Q2) goes high. This turns-off FET Q1 allowing the secondary soft-start capacitor to charge up. This solution of resetting the soft-start capacitor to zero (0 V) on start-up works for pre-bias loads as well as loads that do not need to start into a pre-biased condition. This allows for a monotonic start-up under both operating modes.

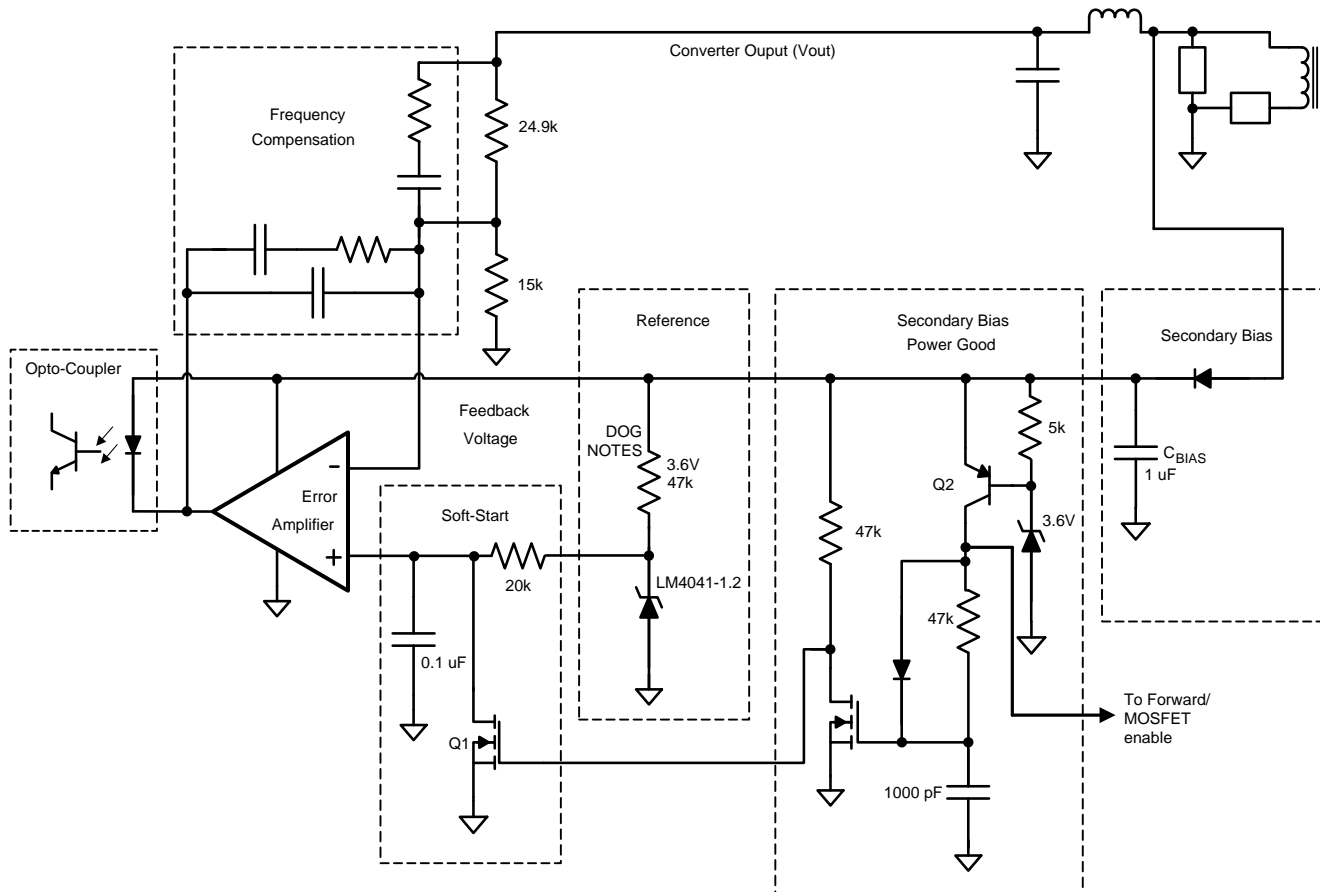


Figure 10. Pre-Bias Schematic

10 Pre-Bias Load-Synchronous Forward MOSFET Enabled

The self driven synchronous rectification topology has an issues starting into a pre-bias load. When a pre-bias load is connected across the power supply output, refer to [Figure 11](#), the pre-bias source will conduct current through the output inductor and the self driven gate drive resistors R1 and R2. If the pre-bias voltage is greater than the V_{gs} of the synchronous MOSFET (M1), the MOSFET will be turned-on sinking current into the power supply.

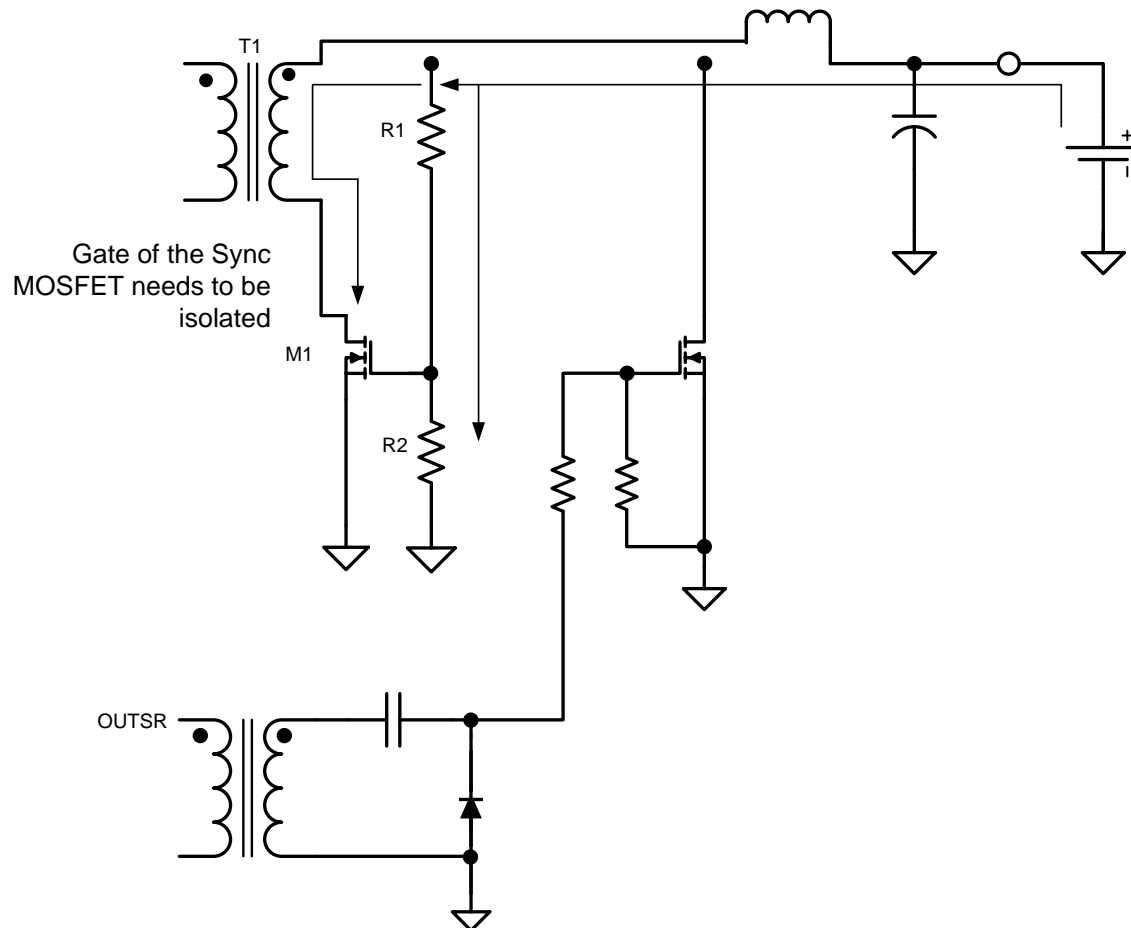


Figure 11. Self Driven with Pre-Bias Load

11 Synchronous Forward MOSFET Enabled

For the LM5027A Evaluation board we used the Secondary Bias Power Good signal as a flag to indicate that the primary sides MOSFETs are switching providing power to the secondary of the transformer T1. When the flag goes high this indicates that it is time to turn-on the forward conducting MOSFET M1. The Secondary Bias Power Good signal drives the base of an NPN transistor (Q3), refer to [Figure 13](#). The NPN transistor is configured as a Cascod amplifier; when it is turned-on, the voltage on the secondary of the transformer T1 drives the gate of the synchronous MOSFET, M1. The MOSFET gate drive voltage is:

$$V\text{-GATE_DRIVE_M1} = V\text{-Secondary_Bias_Power_Good} - V_{BE_Q3} \quad (1)$$

An NPN transistor needs to be selected so that the transistors collector to emitter voltage under the worst case operating condition does not exceed it's VCE ratings, and that the collector current (I_c) can handle the maximum peak current to drive the gate of MOSFET M1. For the LM5027A Evaluation board the transistor is a 30 V, 1.5 ampere transistor. The maximum VCE is:

$$V_{CE} = \frac{V_{in_max}}{n} = \frac{100}{6} = 16.67 \text{ Vpk} \quad (2)$$

Where:

V_{in} = 100 V under transient conditions

n is the transformer turns ratio = 6

A diode D1 is connected from the collector to the emitter of Q3 to handle any voltage spikes as a result of circuit inductance. Without this diode inductive voltage spike may damage the Cascod amplifier Q3.

An NPN transistor was use instead of an N-Channel MOSFET because the V_{gs} drop, typically 4 to 5 V; this would reduce the gates drive voltage to M1. Under minimum input line conditions M1 may not be fully turned-on and there would be an increase in the I² × R_{DS(ON)} losses.

[Figure 12](#) shows the start-up waveforms for the Evaluation board. After the input power is supplied to the Evaluation board the secondary bias voltage rises, when the secondary bias is greater than 3.6 V, the Secondary Power Good output goes high. This turns-on M1 and enables the secondary side soft-start circuit allowing the output voltage to increase after V_{out} > V_{pre-bias}.

An alternative to using the circuit in [Figure 13](#) is shown in [Figure 14](#); an additional winding can be added to the power transformer which can be used to drive the Forward Synchronous Rectifier MOSFET (M1). This is a simple solution and should not add a lot of complexity to the transformer design.

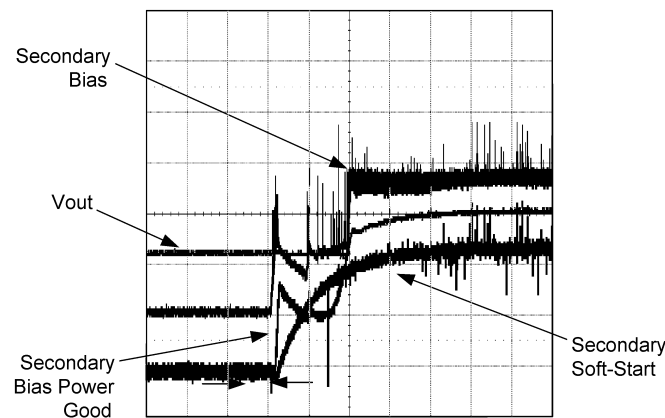


Figure 12. Pre-Bias Load Waveforms

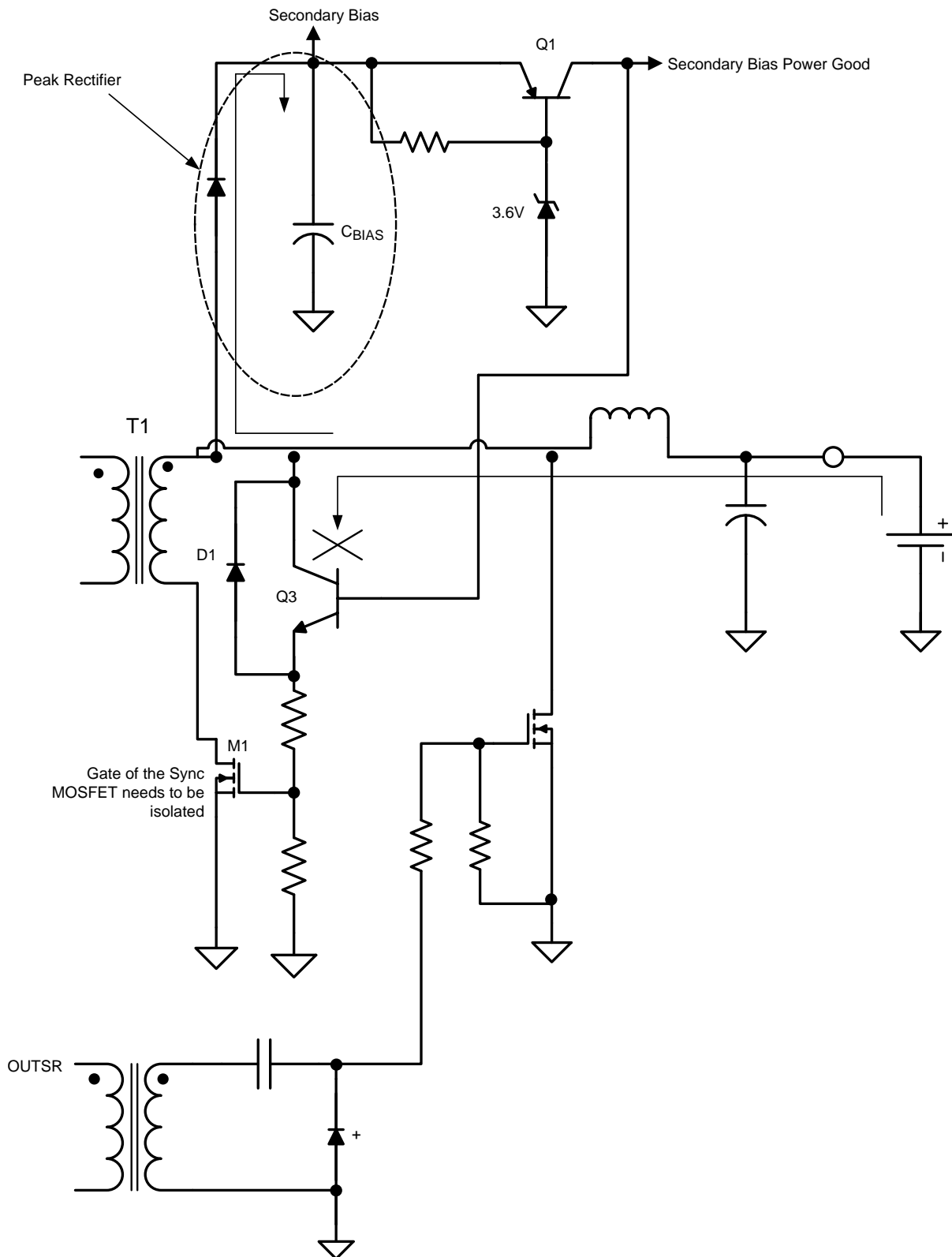


Figure 13. Isolated Synchronous MOSFET

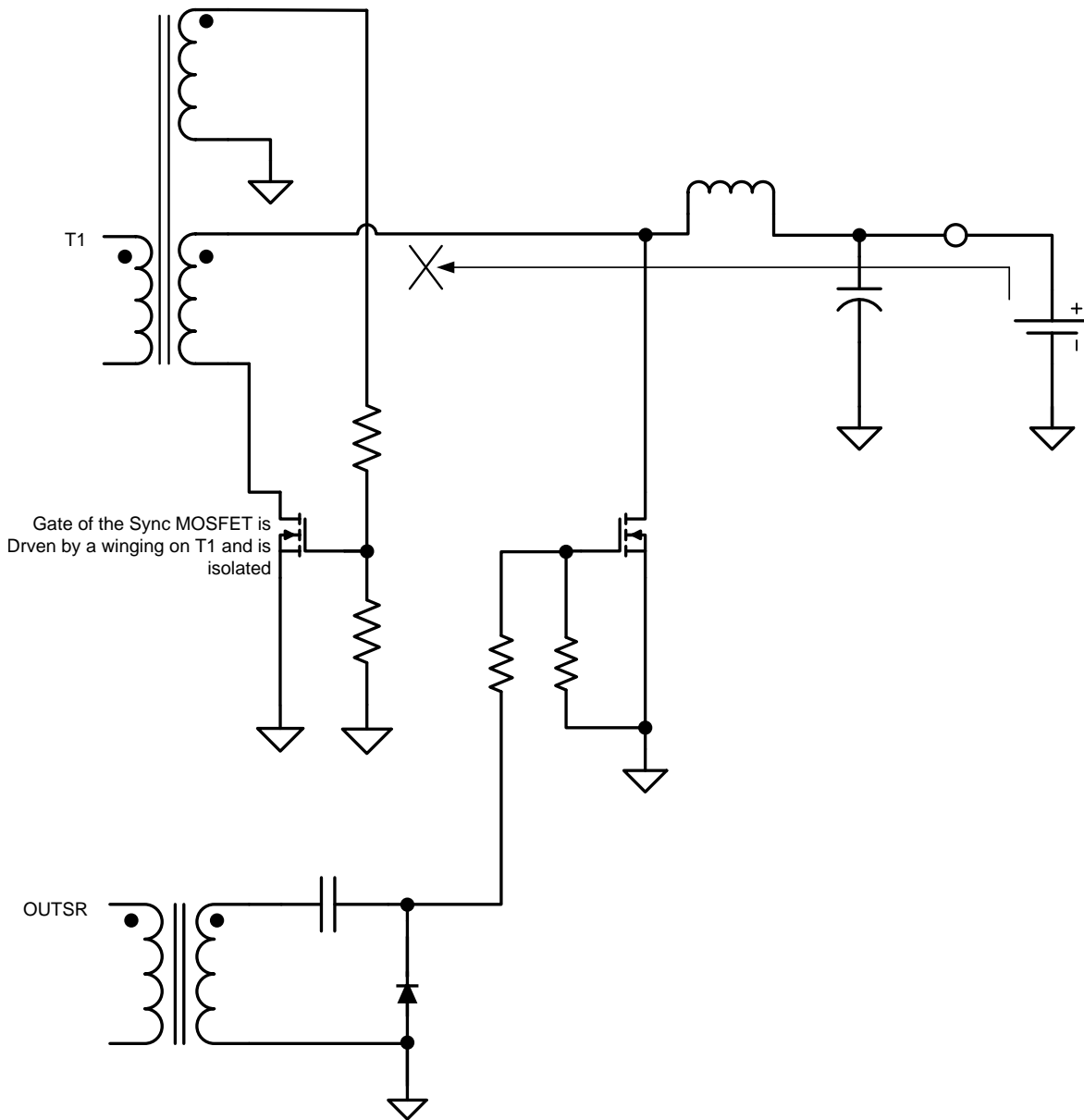


Figure 14. Isolated Synchronous MOSFET Drive Using a Transformer

12 Pre-Bias Load Test Set-Up

For the Pre-bias start-up test, the circuit in [Figure 15](#) was used. An external bias supply, through a $1.0\ \Omega$ resistor, was connected across the output terminals of the Evaluation Board.

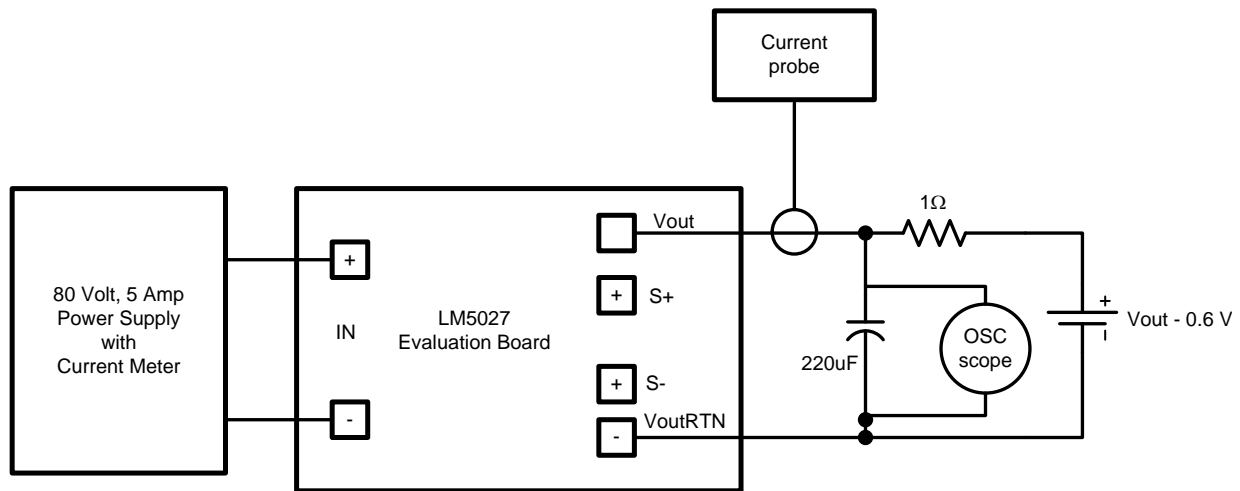


Figure 15. Pre-Bias Load Test Set-Up

13 Pre-Bias Load Start-Up Requirements

The Evaluation board Pre-Bias start-up requirement is that during converter start-up the output shall rise monotonically and not sink current (into the converter) of more than 50 mA .

14 Evaluation Board Results

[Figure 16](#) shows the output of the Evaluation Board starting with a pre-bias voltage of 2.7 V. Under these conditions the output voltage starts at 2.7 V and then increases monotonically to 3.3 V. The current into the Evaluation board (sinking) is less than 50 mA. When the output voltage rise above the pre-bias voltage there is approximately 400 mA of current out of (sourced) the Evaluation Board to charge the external 220 μF capacitor. After the external capacitor is charge to 3.3 V the current out of the power supply drop to approximately 50 mA.

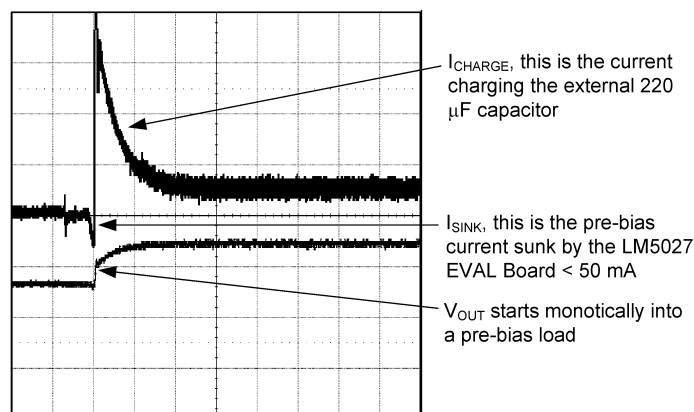
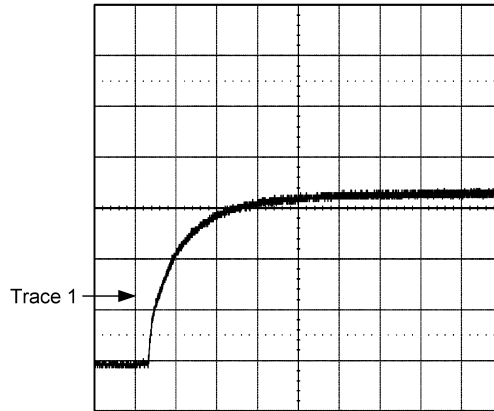


Figure 16. Pre-Bias StartUp

15 Performance Characteristics

15.1 Turn-On Waveforms

When applying power to the LM5027A evaluation board a certain sequence of events occurs. Soft-start capacitor values and other components allow for a minimal output voltage for a short time until the feedback loop can stabilize without overshoot. [Figure 17](#) shows the output voltage during a typical start-up with a 48 V input and a load of 5 A. There is no overshoot during startup.

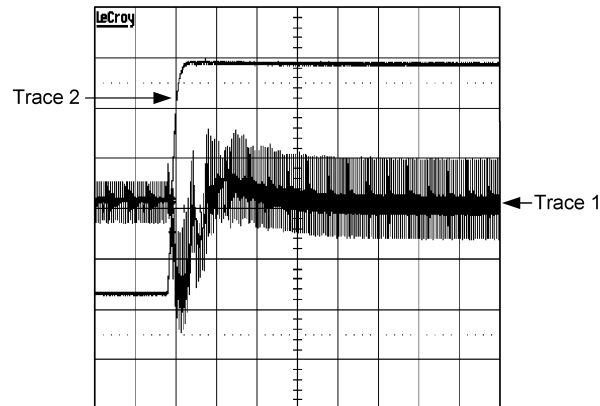


- (1) **Conditions:**
 Input Voltage = 48 VDC
 Output Current = 5 A
Trace 1: Volts/div = 1.0 V
 Output Voltage
Horizontal Resolution = 1 ms/div

Figure 17. Turn-On Waveforms

15.2 Transient Response Waveforms

Figure 18 shows the transient response for a load of change from 2 A to 25 A. The lower trace shows minimal output voltage droop and overshoot during the sudden change in output current shown by the upper trace.

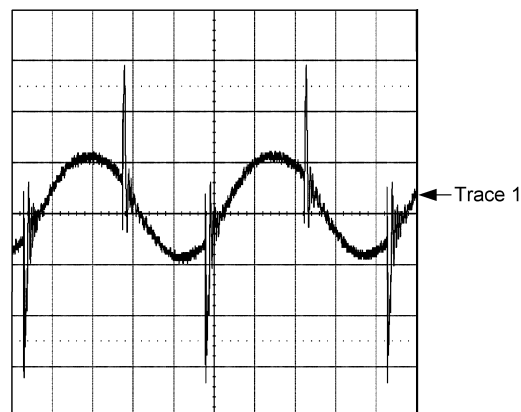


- (1) **Conditions:**
 Input Voltage = 48 VDC
 Output Current = 2 A to 25 A
Trace 1: Volts/div = 0.2 V
 Output Voltage
Trace 2: Amps/Div = 5.0 A
 Output Current
Horizontal Resolution = 1 ms/div

Figure 18. Transient Response Waveforms

15.3 Output Ripple Waveforms

Figure 19 shows typical output ripple seen directly across the output capacitor, for an input voltage of 48 V and a load of 30 A. This waveform is typical of most loads and input voltages.

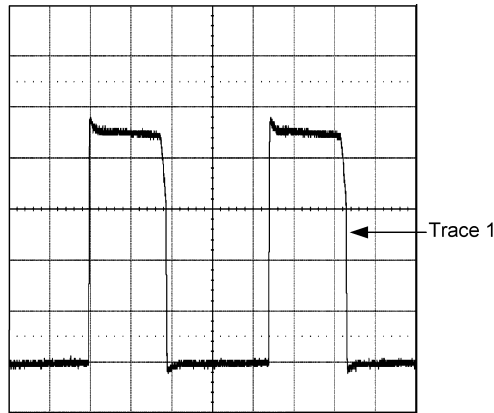


- (1) **Conditions:**
 Input Voltage = 48 VDC
 Output Current = 30 A
 Bandwidth Limit = 25 MHz
Trace 1: Volts/div = 50 mV
 Output Voltage
Horizontal Resolution = 2 μs/div

Figure 19. Output Ripple Waveform

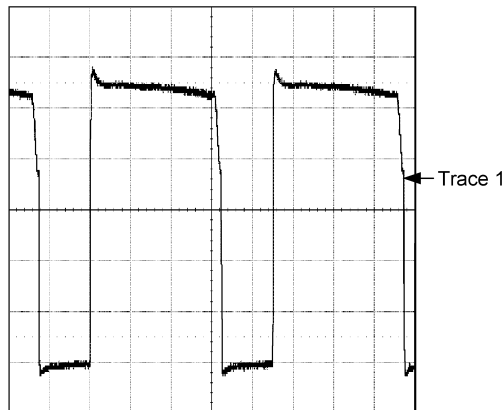
15.4 Drain Voltage of Q1 with a 25 A Load

Figure 20 and Figure 21 show the drain voltage of Q1 with a 25 A load. Figure 20 represents an input voltage of 38 V and Figure 21 represents an input voltage of 78 V.



- (1) **Conditions:**
 Input Voltage = 38 VDC
 Output Current = 25 A
Trace 1: Volts/Div = 20 V
 Q1 Drain Voltage
 Horizontal Resolution = 1 μ s/div

Figure 20. Drain Voltage of Q1 with a 25 A Load - Input Voltage of 38 V

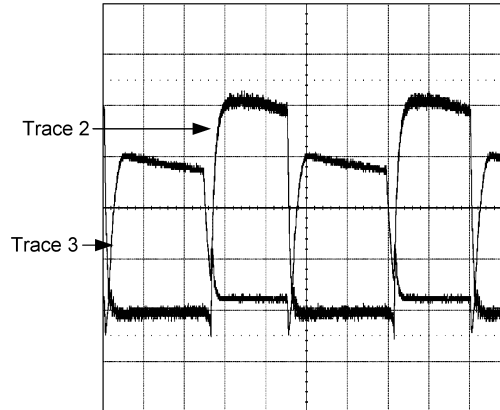


- (1) **Conditions:**
 Input Voltage = 78 VDC
Trace 1: Volts/Div = 20 V
 Q1 Drain Voltage
 Horizontal Resolution = 1 μ s/div

Figure 21. Drain Voltage of Q1 with a 25 A Load - Input Voltage of 78 V

15.5 Gate Voltages

Figure 22 shows the gate voltages of the synchronous rectifiers. The drive from the main power transformer is delayed slightly at turn-on by a resistor interacting with the gate capacitance. This provides improved switching transitions for optimum efficiency. The difference in drive voltage is inherent in the topology and varies with line voltage



- (1) **Conditions:**
 Input Voltage = 48 VDC
 Output Current = 5 A
Trace 3: (gate) Volts/Div = 2 V
 Synchronous Rectifier, Q3/Q4
Trace 2: (gate) Volts/Div = 2 V
 Synchronous Rectifier, Q5/Q6
Horizontal Resolution = 1 μ s/div

Figure 22. Gate Voltages

15.6 Efficiency

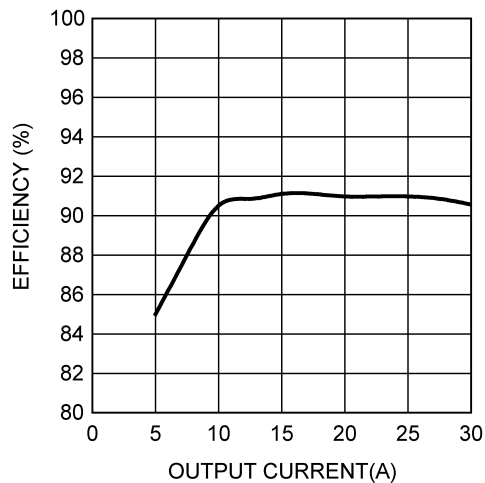


Figure 23. Efficiency

Bill of Materials

Item		Part Number	Description	Value
C	1	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2 μ , 100 V
C	2	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2 μ , 100 V
C	3	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2 μ , 100 V
C	4	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2 v, 100 V
C	5	APXE4R0ARA681MH80G	CAPACITOR, CER, United Chemi-Con	680 μ , 4 V
C	6	C1210C476M8PACTU	CAPACITOR,CER,KEMET	47 μ , 10 V
C	7	C1210C476M8PACTU	CAPACITOR,CER,KEMET	47 μ , 10 V
C	8	C0603C471J5GAC	CAPACITOR, CER, KEMET	470 p, 50 V
C	9	C0603C103K3RAC	CAPACITOR, CER, KEMET	0.01 μ , 25 V
C	10	C0603C223K3RAC	CAPACITOR, CER, KEMET	0.022 μ , 25 V
C	11	C0603C473K3RAC	CAPACITOR, CER, KEMET	0.047 μ , 25 V
C	12	C1608X7R1H104K	CAPACITOR, CER, TDK	0.1 μ , 50 V
C	13	C0603C101J5GAC	CAPACITOR, CER, KEMET	100 p, 50 V
C	14	C0603C104K3RAC	CAPACITOR, CER, KEMET	0.1 μ , 25 V
C	15	C3216X7R2E104K	CAPACITOR, CER, TDK	0.1 μ , 250 V
C	16	C1608X7R1H104K	CAPACITOR, CER, TDK	0.1 μ , 50 V
C	17	C1210C476M8PACTU	CAPACITOR, CER, TDK	47 μ , 10 V
C	18	C1210C476M8PACTU	CAPACITOR, CER, TDK	47 μ , 10 V
C	19	C0603C221J3GAC	CAPACITOR, CER, KEMET	220 p, 25 V
C	20	OPEN		
C	21	C3216X7R2E104K	CAPACITOR, CER, TDK	0.1 μ , 250 V
C	22	C1608X7R1H104K	CAPACITOR, CER, KEMET	0.1 μ , 25 V
C	23	C0603C103K3RAC	CAPACITOR, CER, KEMET	0.01 μ , 25 V
C	24	C0603C473K3RAC	CAPACITOR, CER, KEMET	0.047 μ , 25 V
C	25	C0603C473K3RAC	CAPACITOR, CER, KEMET	0.047 μ , 25 V
C	26	C4532X7R3D222K	CAPACITOR, CER, TDK	2200 p, 2000 V
C	27	GRM188R61E105KA12D	CAPACITOR, CER, MURATA	1.0 μ , 25 V
C	28	C0603C224K3RAC	CAPACITOR, CER, TDK	0.22 μ , 25 V
C	29	C0603C102K3RAC	CAPACITOR, CER, KEMET	1000 p, 25 V
C	30	C0603C102K3RAC	CAPACITOR, CER, KEMET	1000 p, 25 V
C	31	C0805C471J5GAC	CAPACITOR, CER, KEMET	470 p, 50 V
C	32	C0805C471F5GAC	CAPACITOR, CER, KEMET	470 p, 50 V
C	33	C2012X7R2A332K	CAPACITOR, CER, TDK	3300 p, 100 V
C	34	OPEN		
C	71	C4532X7R1E156M	CAPACITOR, CER, TDK	15 μ , 25 V
C	35	C0603C102K3RAC	CAPACITOR, CER, KEMET	1000 p, 25 V
C	36	GRM188R61E105KA12D	CAPACITOR, CER, MURATA	1.0 u, 25 V
D	1	ZHCS350	DIODE, SIGNAL, ZETEX	40 V, 500 mA
D	2	ZHCS350	DIODE, SIGNAL, ZETEX	40 V, 500 mA
D	3	ZHCS350	DIODE, SIGNAL, ZETEX	40 V, 500 mA
D	4	ZHCS350	DIODE, SIGNAL, ZETEX	40 V, 500 mA
D	5	ZHCS350	DIODE, SIGNAL, ZETEX	40 V, 500 mA
D	6	CMD2836	DIODE, DUAL SIGNAL, CENTRAL	120 V, 200 mA
D	7	ZHCS350	DIODE, SIGNAL, ZETEX	40 V, 500 mA
D	8	ZHCS350	DIODE, SIGNAL, ZETEX	40 V, 500 mA
D	9	ZHCS350	DIODE, SIGNAL, ZETEX	40 V, 500 mA

Item	Part Number	Description	Value	
J	1	3104-2-00-01-00-00-08-0	PIN, BRICK, 0.040D, MILL-MAX	MOUNT ON SOLDER SIDE OF PCB
J	2	3104-2-00-01-00-00-08-0	PIN, BRICK, 0.040D, MILL-MAX	MOUNT ON SOLDER SIDE OF PCB
J	4	3104-2-00-01-00-00-08-0	PIN, BRICK, 0.040D, MILL-MAX	MOUNT ON SOLDER SIDE OF PCB
J	5	3231-2-00-01-00-00-08-0	PIN, BRICK, 0.080D, MILL-MAX	MOUNT ON SOLDER SIDE OF PCB
J	6	3104-2-00-01-00-00-08-0	PIN, BRICK, 0.040D, MILL-MAX	MOUNT ON SOLDER SIDE OF PCB
J	8	3104-2-00-01-00-00-08-0	PIN, BRICK, 0.040D, MILL-MAX	MOUNT ON SOLDER SIDE OF PCB
J	9	3231-2-00-01-00-00-08-0	PIN, BRICK, 0.080D, MILL-MAX	MOUNT ON SOLDER SIDE OF PCB
L	1	SRU1048-6R8Y	INPUT CHOKE, Bourns	6.8 uH, 4.8 Arms
L	2	7443556130	CHOKE, WURTH	1.2 uH, 37 A
L	3	SDR0503-332JL	CHOKE, Bourns	3.3 mH, 0.045 A
Q	1	SI7846DP	N-FET, SILICONIX	150 V, 50 m
Q	2	SI3475	P-FET, IR	200 V, 1.6
Q	3	SI7866DP	FET, SILICONIX	20 V, 3 m
Q	4	SI7866DP	FET, SILICONIX	20 V, 3 m
Q	5	SI7866DP	FET, SILICONIX	20 V, 3 m
Q	6	SI7866DP	FET, SILICONIX	20 V, 3 m
Q	7	MMBT2907A	Bipolar, PNP, 60 V, 600 mA	
Q	8	QSX6	Bipolar, NPN, 30 V, 1.5 A	ROHM
Q	9	2N7002VA	FET, N_Channel, Fairchild	60 V 280 mA
Q	10	MMBT2907A	Bipolar, PNP, 60 V, 600 mA	
R	1	CRCW120610R0F	RESISTOR	10
R	2	CRCW08059093F	RESISTOR	90.9 k
R	3	CRCW06032002F	RESISTOR	20 k
R	4	CRCW06034992F	RESISTOR	49.9 k
R	5	CRCW06034991F	RESISTOR	4.99 k
R	6	CRCW08059093F	RESISTOR	90.9 K
R	7	CRCW06031001F	RESISTOR	1 K
R	8	CRCW06036191F	RESISTOR	6.19 K
R	9	CRCW06035R60F	RESISTOR	5.6
R	10	CRCW060352302F	RESISTOR	52.3 K
R	11	CRCW06032002F	RESISTOR	20 K
R	12	CRCW06031001F	RESISTOR	1 K
R	13	CRCW06035R60F	RESISTOR	5.6
R	14	CRCW120649R9F	RESISTOR	49.9
R	15	CRCW06036R34F	RESISTOR	6.34
R	16	OPEN		
R	17	CRCW06032200F	RESISTOR	220
R	18	CRCW06031002F	RESISTOR	10 k
R	19	CRCW06034R70F	RESISTOR	4.7
R	20	SHORT (0 Ω)	RESISTOR, 0 Ω	0 Ω
R	21	CRCW06031001F	RESISTOR	1 K
R	22	CRCW06032000F	RESISTOR	200
R	23	CRCW06031002F	RESISTOR	10 k
R	24	CRCW06031502F	RESISTOR	15 k

Item		Part Number	Description	Value
R	25	CRCW06032492F	RESISTOR	24.9 k
R	26	CRCW060310R0F	RESISTOR	10
R	27	CRCW060310R0F	RESISTOR	10
R	28	CRCW06031001F	RESISTOR	1 k
R	29	CRCW06032002F	RESISTOR	20.0 k
R	30	CRCW06031002F	RESISTOR	10.0 k
R	31	CRCW06034990F	RESISTOR	499
R	32	OPEN		
R	33	SHORT (0 Ω)	RESISTOR, 0 Ω	0 Ω
R	34	CRCW1218110ROFKEK	RESISTOR	10, 1 W
R	35	CRCW1218110ROFKEK	RESISTOR	10, 1 W
R	36	CRCW06031001F	RESISTOR	1 k
R	37	CRCW06033011F	RESISTOR	3.01 k
R	38	CRCW06034990F	RESISTOR	499
R	39	CRCW06034702F	RESISTOR	47 k
R	40	CRCW06034702F	RESISTOR	47 k
R	41	CRCW06034702F	RESISTOR	47 k
R	42	CRCW06031002F	RESISTOR	10 k
R	T1	NTCG164BH103H	NTC, 10k@25°C, 1k@100°C, TDK	10 k
T	1	HA4000-AI	POWER XFMR W/AUX, COILCRAFT	12:2
T	2	DA2319-ALB	Gate Drive, Coilcraft	
T	3	P8208T, Pulse	CURRENT XFR, PULSE ENG	100:1
U	1	LM5027	CONTROLLER, TEXAS INSTRUMENTS	
U	2	PS2811-1M	OPTO-COUPLER, NEC	
U	3	LM8261	OPAMP, TEXAS INSTRUMENTS	
U	4	LM4040	REFERENCE, TEXAS INSTRUMENTS	
U	5	LM4041	REFERENCE, TEXAS INSTRUMENTS	
Z	2	MM5Z3V6	DIODE, ZENER 3.6 V	Fairchild

16 Printed Circuit Layout

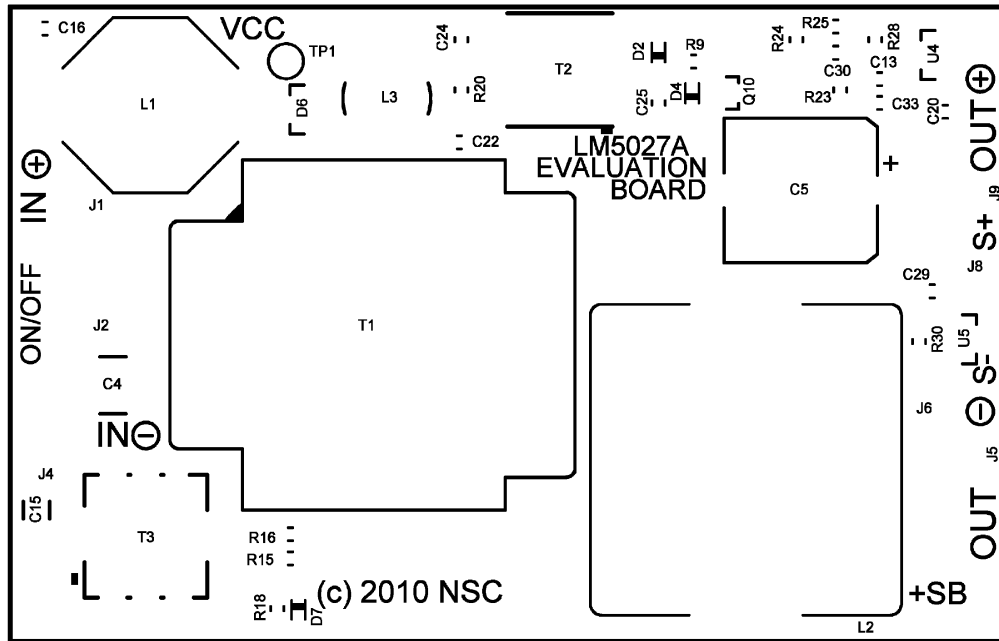


Figure 24. Top Assembly Layer

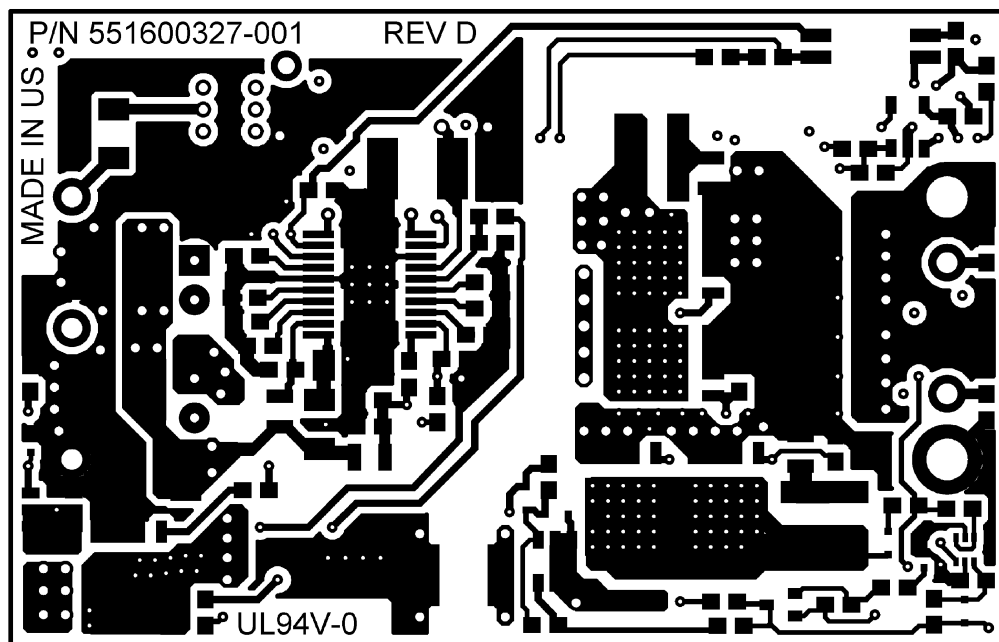


Figure 25. Bottom Layer



Figure 26. Bottom Silk Layer

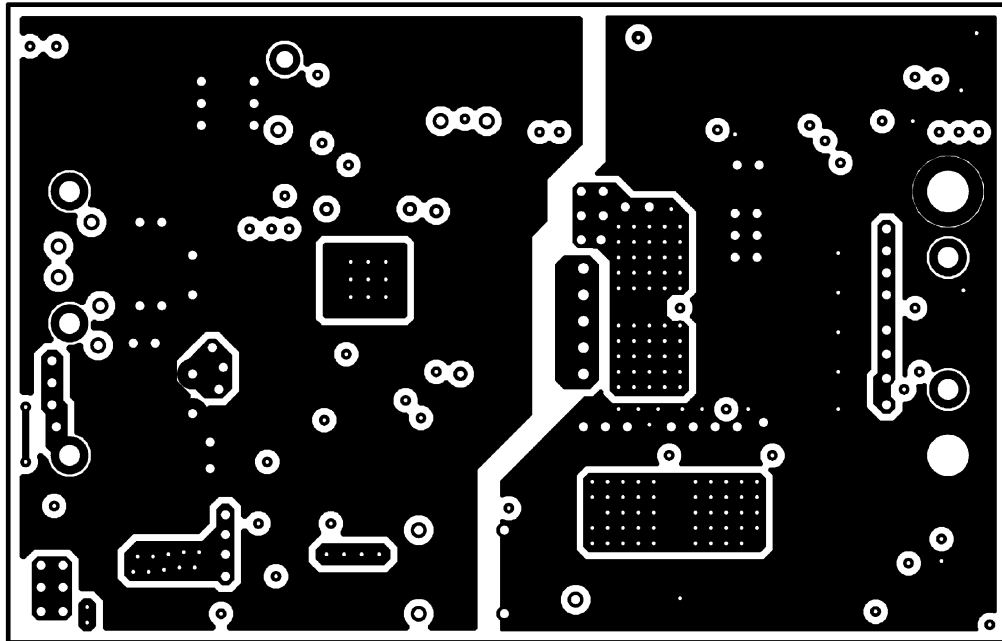


Figure 27. Mid 1 Layer

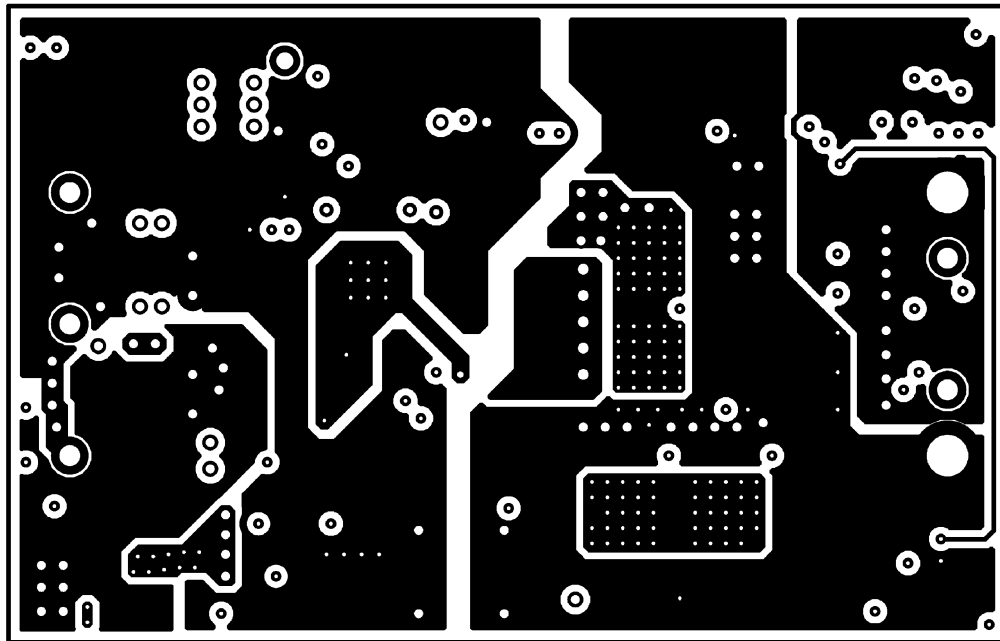


Figure 28. Mid 2 Layer

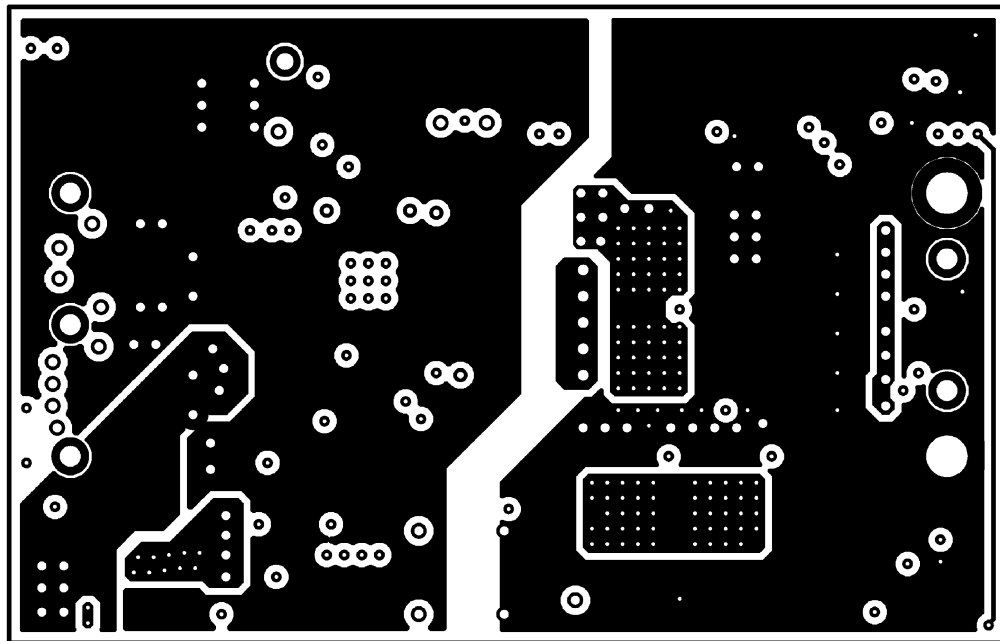


Figure 29. Mid 3 Layer

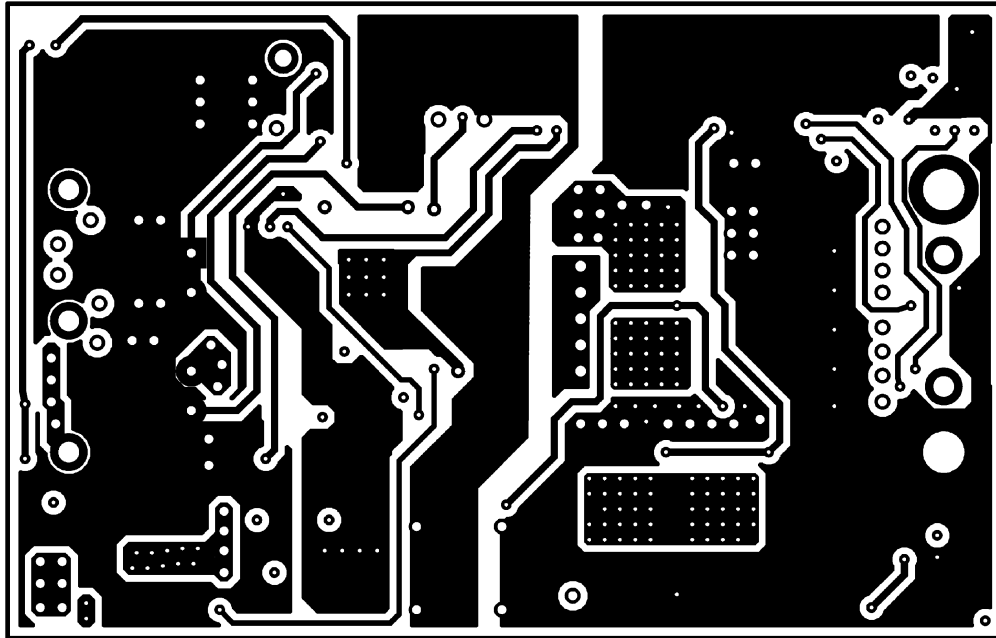


Figure 30. Mid 4 Layer

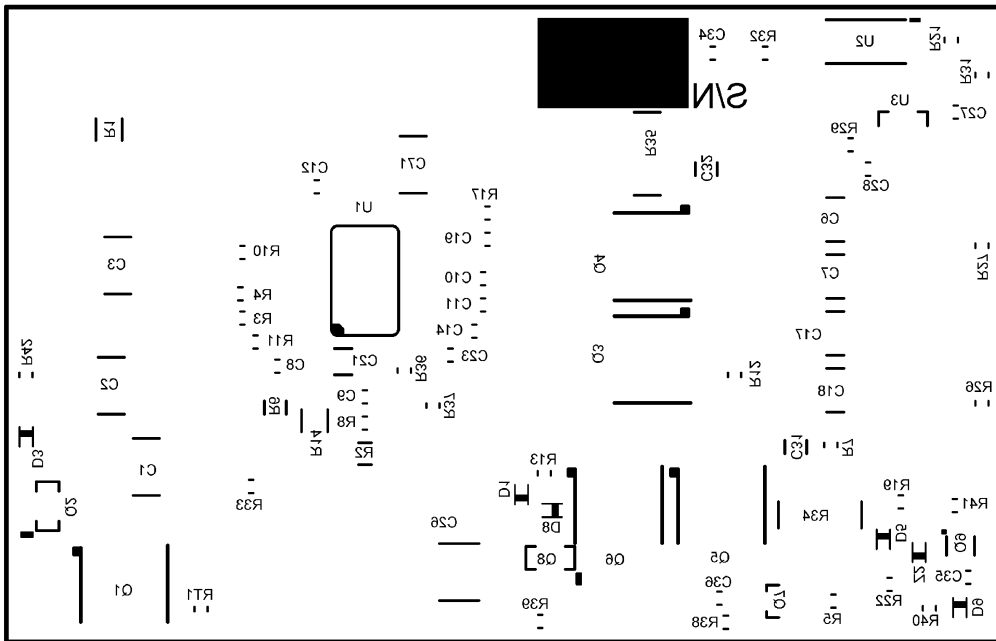


Figure 31. Bottom Assembly Layer

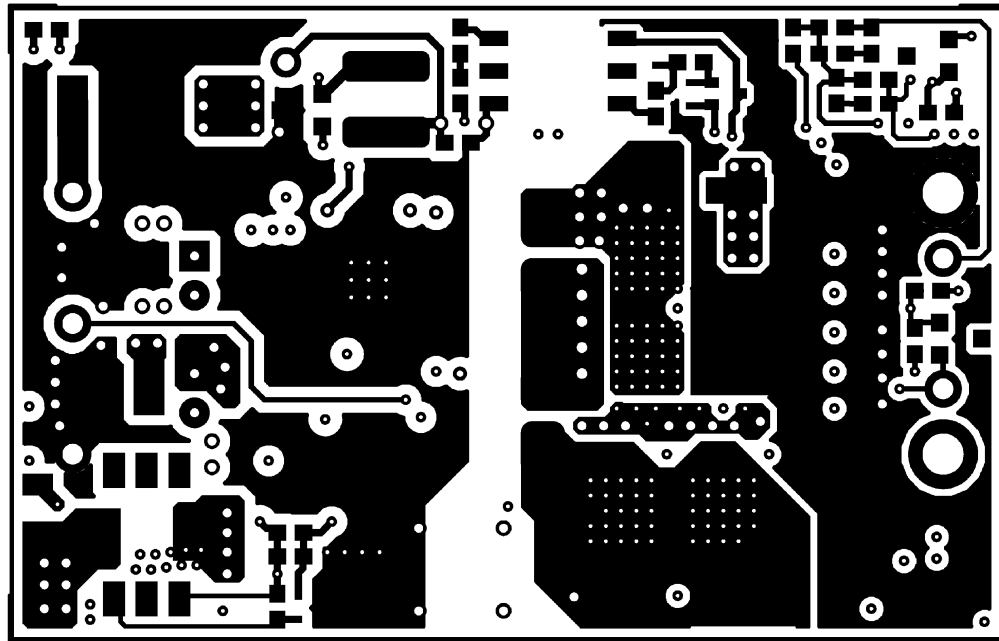


Figure 32. Top Layer

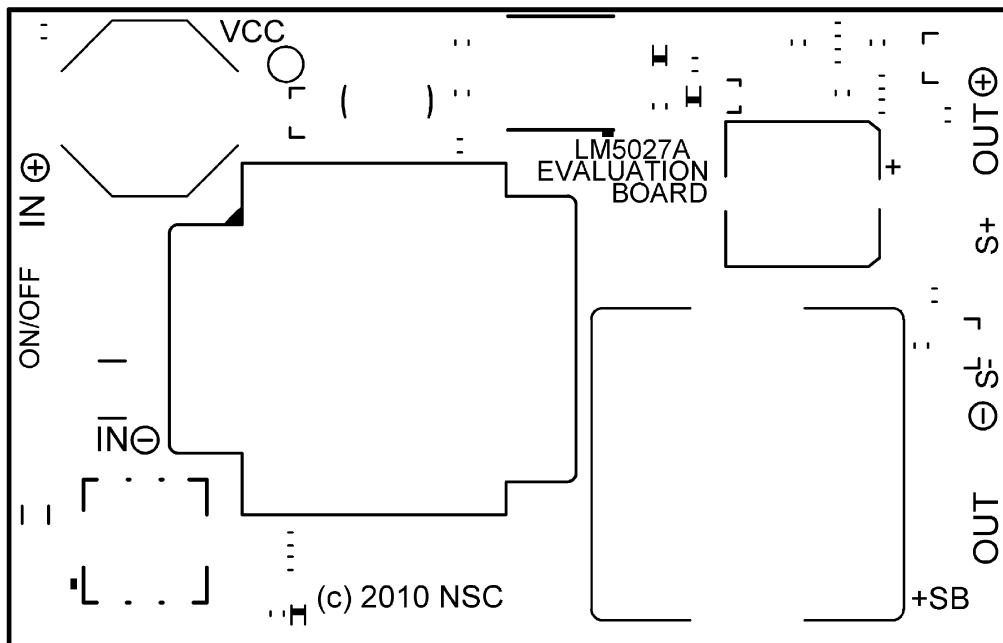


Figure 33. Top Silk Layer

17 Application Schematic

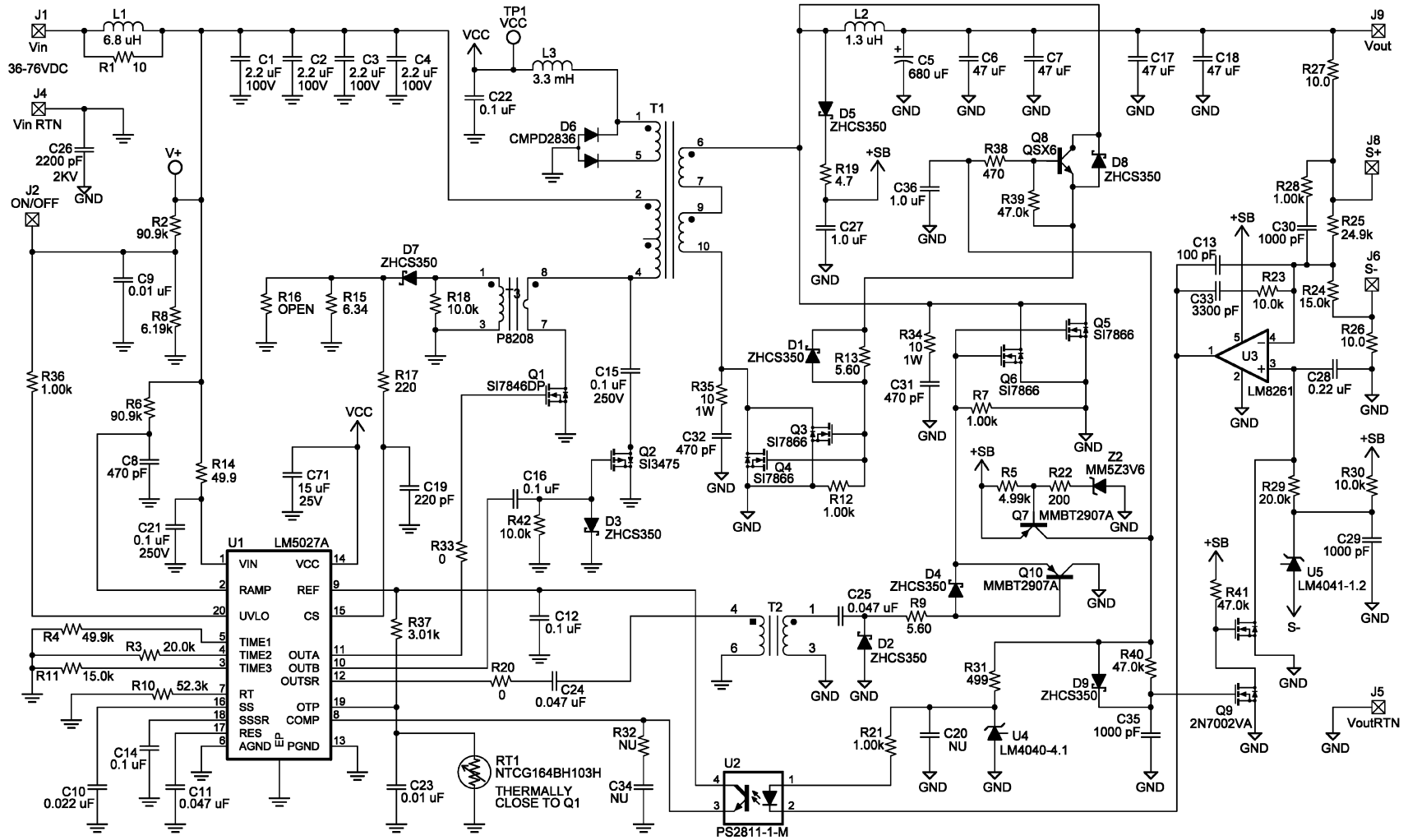


Figure 34. Application Schematic: Input 36-76, Voutput 6.3 A, 30 A

Revision History

Changes from A Revision (May 2013) to B Revision	Page
• Changed Top Layer Assy to Bottom Assy, since Top was in twice.	22

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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