AN-1589 LM48821 Evaluation Board

1 Quick Start Guide

1. Connect the I^2C signal generation and interface board to a computer's parallel port.
2. Install LM48821 control software: "LM48821_Software."
3. Amplifier output mode:
4. Apply a 2.0V to 4.0V power supply's positive voltage output to the "VDD" pin on jumper J6. Apply the power supply's ground return to the "GND" pin on J6.
5. Connect the supplied 5-wire cable between the I^2C signal generation and interface board and the 5-pin connector (I2C Interface) on the LM48821 demonstration board.
6. Apply a stereo audio signal to jumpers JP2 (Left) and JP3 (Right). Apply the source's +input and -input to the "+" pin and the "-" pin, respectively.
7. Connect a load (≥ 16Ω) to JP (Right) and another load to JP5 (Left). JP4's "+" pin and JP's "+" pin carries the output signals from the two amplifiers found on pins OUTR and OUTL, respectively.
8. Apply power. Make measurements. Plug in a pair of headphones. Enjoy.

2 Introduction

To help the user investigate and evaluate the LM48821's performance and capabilities, a fully populated demonstration board is available from the Texas Instruments Audio Products Group. This board is shown in Figure 1. Connected to an external power supply (2.0V to 4.0V), a signal source and an I^2C controller (or signal source), the LM48821 demonstration board easily demonstrate the amplifier's features.

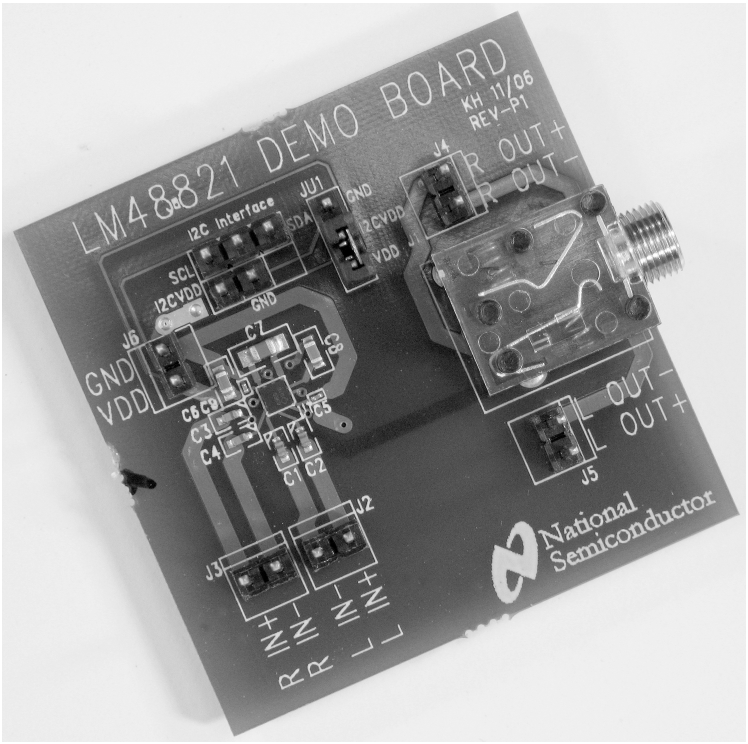

Figure 1. LM48821 Demonstration Board

3 General Description

The LM48821 is a fully differential input stereo headphone audio amplifier with an internal digitally controlled volume control. The LM48821 is optimized to operate over a power supply voltage range of 2.0V to 4.0V. This amplifier is capable of delivering 53mW$_{RMS}$ per channel into a 32Ω load at 1% THD when powered by a 3.0V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. To that end, the LM48821 features two functions that optimize system cost and minimize PCB area: an integrated, digitally controlled (I^2C bus) volume control and an amplifier generated negative power supply voltage that eliminates output signal-coupling capacitors. Since the LM48821 does not require bootstrap capacitors, snubber networks, or output coupling capacitors, it is optimally suited for low-power, battery powered potable systems.

The LM48821 includes separate shutdown controls for each stereo channel for micropower dissipation, an internal thermal shutdown protection mechanism, and is unity gain stable.

4 Operating Conditions

- Temperature Range –40°C ≤ T_A ≤ 85°C
- Amplifier Power Supply Voltage 2.0V ≤ V_{DD} ≤ 5.0V ≤ 4.0V

5 Schematic

Figure 2 shows the LM48821 Demonstration Board schematic. Refer to Table 1 for a list of the connections and their functions.

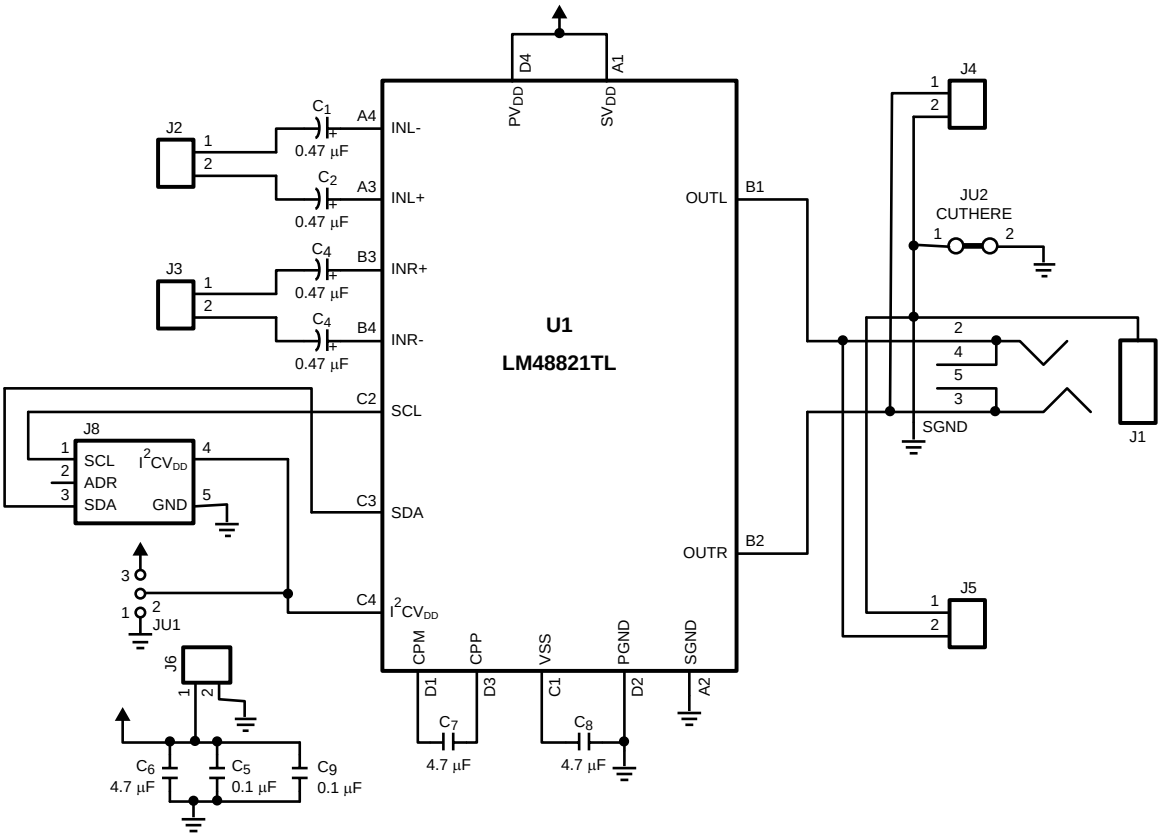

Figure 2. LM48821 Demonstration Board Schematic

6 Board Features

The LM48821 demonstration board has all of the necessary connections, using 0.100" headers, to apply the power supply voltage, the audio input signals, and the I^2C signal inputs. The amplified audio signal is available on both a stereo headphone jack and auxiliary output connections.

Also included with the demonstration board is an I^2C signal generation board and software. With this board and the software, the user can easily control the LM48821's, shutdown function, mute, and stereo volume control. Figure 3 shows the software's graphical user interface.

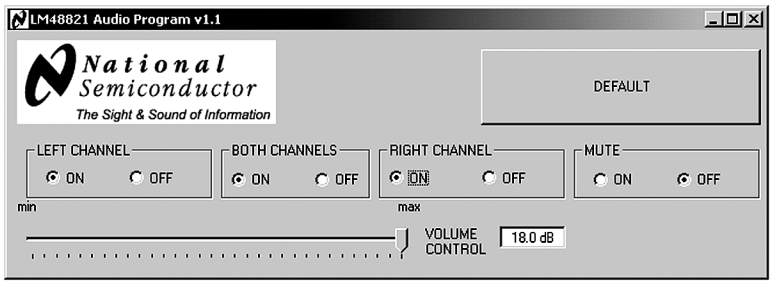

Figure 3. LM48821 Software User's Interface

7 Connections

Connecting to the world is accomplished through the 0.100” headers on the LM48821 demonstration board. The functions of the different headers are detailed in Table 1.

Table 1. LM48821 Demonstration Board Connections

Jumper Designation	Function or Use
J1	Stereo, 0.125” headphone jack. Left channel is on the tip connector and the right channel is on the ring connector. Ground is on the sleeve connector.
J2	This is the connection to the amplifier’s differential left channel input. Apply an external differential signal source’s positive voltage to the J2 pin labeled “L IN+” and the signal source’s negative input to the pin labeled “L IN-.”
J3	This is the connection to the amplifier’s differential right channel input. Apply an external differential signal source’s positive voltage to the J3 pin labeled “R IN+” and the signal source’s negative input to the pin labeled “R IN-.”
J4	This is the connection to the amplifier’s single-ended, ground- referenced right channel output. Connect the J4 pin labeled “R OUT+” and the pin labeled “R OUT-” to the positive and ground inputs, respectively, of an external signal measurement device. J4’s pin labeled “R OUT+” corresponds to the headphone jack’s “ring” connection. J4’s pin labeled “R OUT-“ corresponds to the headphone jack’s “sleeve” (or ground) connection.
J5	This is the connection to the amplifier’s single-ended, ground- referenced left channel output. Connect the J5 pin labeled “L OUT+” and the pin labeled “L OUT-” to the positive and ground inputs, respectively, of an external signal measurement device. J5’s pin labeled “L OUT+” corresponds to the headphone jack’s “tip” connection. J5’s pin labeled “L OUT-“ corresponds to the headphone jack’s “sleeve” (or ground) connection.
J6	Power supply connection. Connect an external power supply’s positive voltage source (2.0V to 4.0V) to the J6 pin labeled “V_{DD}” and the supply’s ground source to the pin labeled “GND.”
J8 (I^2C Interface)	This is the input connection for the I^2C serial clock and serial data signals. J8-pin 1 is for the SCL signal, JP8-pin 2 is not used. J8-pin 3 is for the SDA signal. J8-pin 4 is for an I^2C V_{DD} supply voltage supplied by the I^2C signal source. J8-pin 5 is for ground.
JU1	If an external I^2C power supply voltage is used, connect this supply’s positive voltage source to the JU1 pin labeled “I^2CV_{DD}” and the supply’s ground source to the pin labeled “GND.” If the external V_{DD} power supply is used for the I^2CV_{DD}voltage, place a jumper between the JU1 pin labeled “V_{DD}” and the JU1 pin labeled “I^2CV_{DD}.”

8 Power Supply Sequencing

The LM48821 uses two power supply voltages: V_{DD} for the analog circuitry and I^2CV_{DD}, which defines the digital control logic high voltage level. To ensure proper functionality, apply V_{DD} first, followed by I^2CV_{DD}. If one power supply is used, V_{DD} and I^2CV_{DD} can be connected together. The part will power-up with both channels shutdown, the volume control set to minimum, and the mute function active.

9 I^2C Signal Generation Board and Software

The I^2C signal generation and interface board, along with the LM48821 software, will generate the address byte and the data byte used in the I^2C control data transaction. To use the I^2C signal generation and interface board, please plug it into a PC’s parallel port (on either a notebook or a desktop computer).

The software comes with an installer. To install, unzip the file titled “LM48821_Software.” After the file unzips, double-click the “setup.exe” file. After it launches, please follow the installer’s instructions. Setup will create a folder named “LM48821” in the “Program” folder on the “C” disk (if the default is used) along with a shortcut of the same name in the “Programs” folder in the “Start” menu.

The LM48821 program includes controls for the amplifier’s volume control, individual channel shutdown, and the mute function. The control program's on-screen user interface is shown in Figure 3.

The Default button is used to return the LM48821 to its power-on reset state: minimum volume setting, shutdown on both amplifiers active, and mute active.

The LM48821’s stereo **VOLUME CONTROL** has 32 steps and a gain range of –76dB to 18dB. It is controlled using the slider located at the bottom of the program’s window. Each time the slider is moved from one tick mark to another, the program updates the amplifier’s volume control.

LEFT CHANNEL, BOTH CHANNELS, and RIGHT CHANNEL controls each have two buttons. For the left and right channel control, the “ON” button activates its respective channel, whereas the “OFF” button places its respective channel in shutdown mode. Selecting the **BOTH CHANNELS** “ON” button simultaneously activates both channels, whereas selecting the “OFF” button places channels in shutdown mode.

10 PCB Layout Guidelines

This section provides general practical guidelines for PCB layouts that use various power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results are predicated on the final layout.

10.1 Power and Ground Circuits

Star trace routing techniques (returning individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major positive impact on low-level signal performance. Star trace routing refers to using individual traces that radiate from a signal point to feed power and ground to each circuit or even device. This technique may require greater design time, but should not increase the final price of the board.

For good THD + N and low noise performance and to ensure correct power-on behavior at the maximum allowed supply voltage, a local 4.7µF power supply bypass capacitor should be connected as physically close as possible to the PV_{DD} pin.

10.2 Avoiding Typical Design/Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other, do so at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and crosstalk.

11 Bill of Materials

Designator	Part Description	Value	Tolerance	Rating	Package Type	Manufacturer	Manufacturer's Part Number
C1–C4	TACmicrochip tantalum capacitor	0.47µF	±20%	10V	0402	AVX	TACK474M010PTA
C5, C9	Multilayer Ceramic Capacitor	0.1µF	±10%	6.3V	0201	TDK	C0603X5R1A104M
C6, C8	Multilayer Ceramic Capacitor	4.7µF	±20%	6.3V	0603	TDK	C1608X5R1A475M
C7	Multilayer Ceramic Capacitor	4.7µF	±20%	10V	0805	TDK	C2012X5R1A475M
J1	Headphone Jack						
J2–J6	2-pin header, 100mil lead pitch						
J8	5-pin header, 100mil lead pitch						
JU1	3-pin header, 100mil lead pitch						
U1	LM48821Direct Coupled Tru-GND, Ultra Low Noise, 80mW Differential Inputs Stereo Headphone Amplifier with I^2C Volume Control					Texas Instruments	LM48821

12 Demonstration Board PCB Layout

Figure 4 through Figure 9 show the different layers used to create the LM48821 four-layer demonstration board. Figure 4 is the silkscreen that shows parts location, Figure 5 is the top layer, Figure 6 is the upper middle layer, Figure 7 is the lower middle layer, Figure 8 is the bottom layer, and Figure 9 is the bottom silkscreen layer.

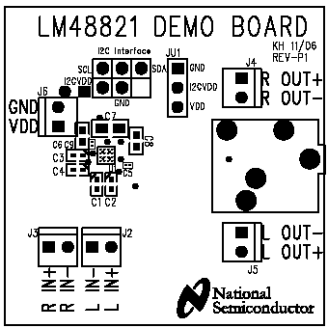

Figure 4. Top Silkscreen (Shown 2.6X actual size)

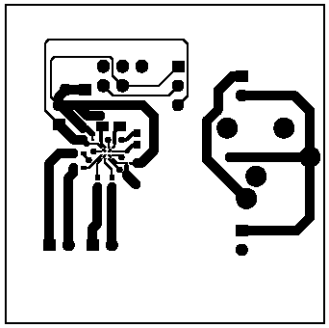

Figure 5. Top Layer (Shown 2.6X actual size)

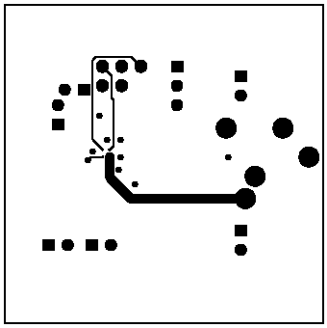

Figure 6. Upper Middle Layer (Shown 2.6X actual size)

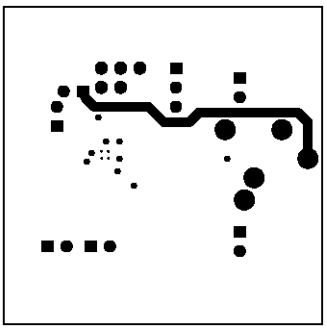

Figure 7. Lower Middle Layer (Shown 2.6X actual size)

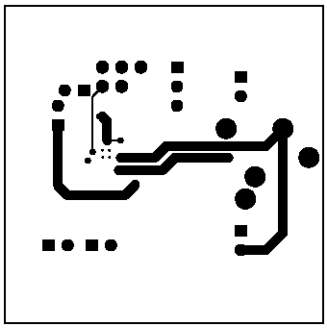

Figure 8. Bottom Layer (Shown 2.6X actual size)

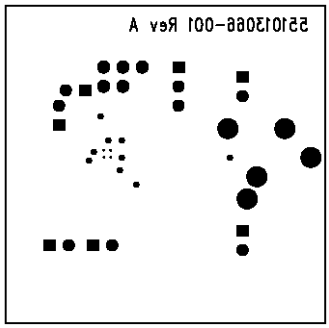

Figure 9. Bottom Silk Layer (Shown 2.6X actual size)

13 Typical Performance

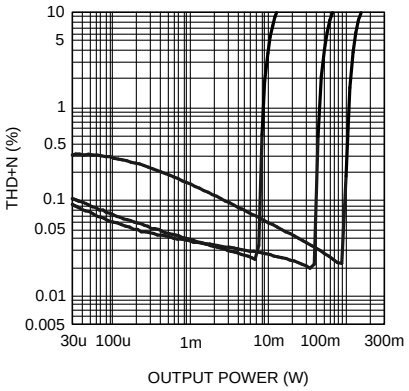

Figure 10. Stereo THD+N vs Output Power
R_L = 16Ω, A_V = 0dB, f = 100Hz
at (from left to right at 1% THD+N):
V_{DD} = 2V, V_{DD} = 3V, V_{DD} = 4V,
both channels driven and measured

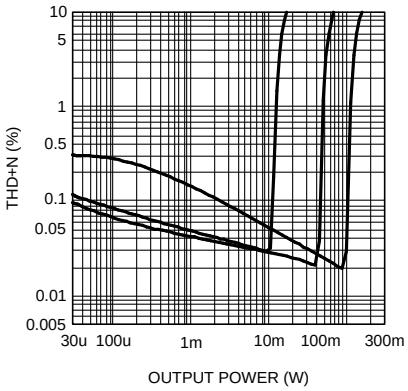

Figure 11. Stereo THD+N vs Output Power
R_L = 16Ω, A_V = 0dB, f = 1kHz
at (from left to right at 1% THD+N):
V_{DD} = 2V, V_{DD} = 3V, V_{DD} = 4V,
both channels driven and measured

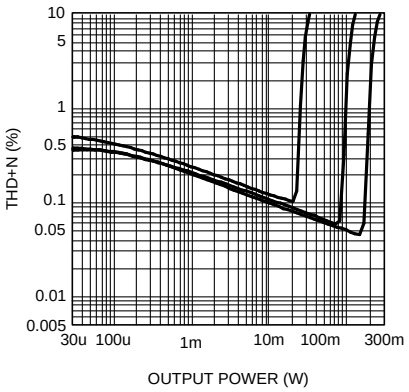

Figure 12. Stereo THD+N vs Output Power
R_L = 16Ω, A_V = 0dB, f = 10kHz
at (from left to right at 1% THD+N):
V_{DD} = 2V, V_{DD} = 3V, V_{DD} = 4V,
both channels driven and measured

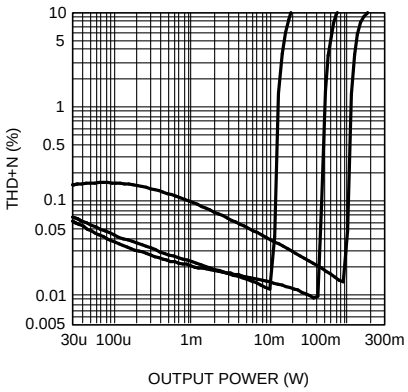

Figure 13. Stereo THD+N vs Output Power
R_L = 32Ω, A_V = 0dB, f = 100Hz
at (from left to right at 1% THD+N):
V_{DD} = 2V, V_{DD} = 3V, V_{DD} = 4V,
both channels driven and measured

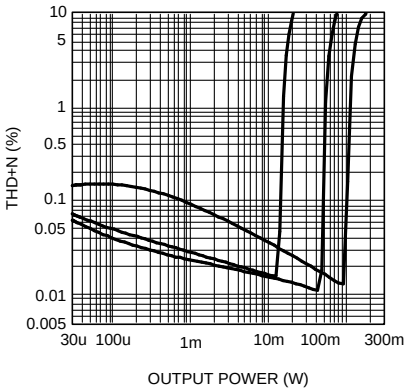

Figure 14. Stereo THD+N vs Output Power
R_L = 32Ω, A_V = 0dB, f = 1kHz
at (from left to right at 1% THD+N):
V_{DD} = 2V, V_{DD} = 3V, V_{DD} = 4V,
both channels driven and measured

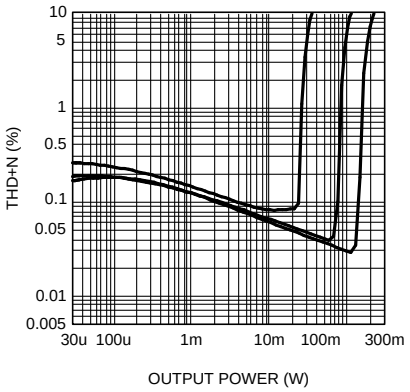

Figure 15. Stereo THD+N vs Output Power
R_L = 32Ω, A_V = 0dB, f = 10kHz
at (from left to right at 1% THD+N):
V_{DD} = 2V, V_{DD} = 3V, V_{DD} = 4V,
both channels driven and measured

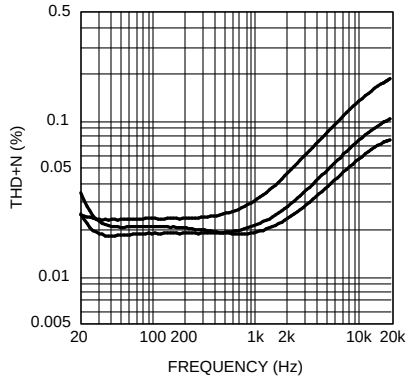

Figure 16. Stereo THD+N vs Frequency
R_L = 16Ω, A_V = 0dB
at (from left to bottom at 10kHz):
V_{DD} = 2V, P_{OUT} = 7mW;
V_{DD} = 3V, P_{OUT} = 36mW;
V_{DD} = 4V, P_{OUT} = 92mW;
both channels driven and measured

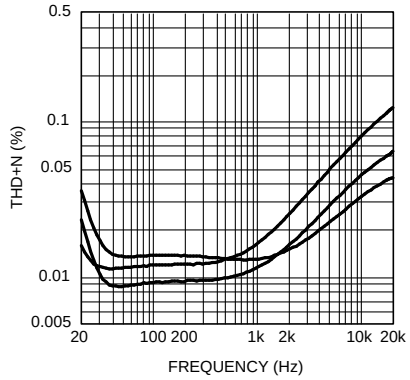

Figure 17. Stereo THD+N vs Frequency
R_L = 32Ω, A_V = 0dB
at (from left to bottom at 10kHz):
V_{DD} = 2V, P_{OUT} = 10mW;
V_{DD} = 3V, P_{OUT} = 38mW;
V_{DD} = 4V, P_{OUT} = 85mW;
both channels driven and measured

Appendix A LM48821 I²C Control Register

Table 2 shows the actions that are implemented by manipulating the bits within the internal I²C control register.

Table 2. LM48821 I²C Control Register Addressing and Data Format Chart

	D7	D6	D5	D4	D3	D2	D1	D0
I²C Address	1	1	1	0	1	1	0	0
Control Register	V4	V3	V2	V1	V0	MUTE	LEFT ENABLE	RIGHT ENABLE

Appendix B Volume Control Settings Binary Values

The minimum volume setting is set to –76dB when 00000 is loaded into the volume control register. Incrementing the volume control register in binary fashion increases the volume control setting, reaching full scale at 11111. Table 3 shows the value of the gain for each of the 32 binary volume control settings.

Table 3. Binary Values for the Different Volume Control Gain Settings

Gain	B4	B3	B2	B1	B0
18	1	1	1	1	1
17	1	1	1	1	0
16	1	1	1	0	1
15	1	1	1	0	0
14	1	1	0	1	1
13	1	1	0	1	0
12	1	1	0	0	1
10	1	1	0	0	0
8	1	0	1	1	1
6	1	0	1	1	0
4	1	0	1	0	1
2	1	0	1	0	0
0	1	0	0	1	1
–2	1	0	0	1	0
–4	1	0	0	0	1
–6	1	0	0	0	0
–8	0	1	1	1	1
–10	0	1	1	1	0
–12	0	1	1	0	1
–14	0	1	1	0	0
–16	0	1	0	1	1
–18	0	1	0	1	0
–21	0	1	0	0	1
–24	0	1	0	0	0
–27	0	0	1	1	1
–30	0	0	1	1	0
–34	0	0	1	0	1
–38	0	0	1	0	0
–44	0	0	0	1	1
–52	0	0	0	1	0
–62	0	0	0	0	1

Table 3. Binary Values for the Different Volume Control Gain Settings (continued)

Gain	B4	B3	B2	B1	B0
–76	0	0	0	0	0

Appendix C Micro SMD Wafer Level Chip Scale Package, PCB, Layout, and Mounting Considerations

Please refer to *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009) for possible updates to the µSMD package information.

Appendix D Revision History

Rev	Date	Description
1.0	05/14/07	Initial release.

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