AN-1992 LM27402 Evaluation Board

1 Introduction

The LM27402 is a feature-rich, synchronous, single phase PWM DC/DC buck controller. A wide input voltage range of 3V to 20V, input voltage feed-forward, and dual high current integrated N-channel MOSFET drivers make the LM27402 appropriate for high current intermediate bus system rails in point-of-load applications. A 0.6V ±1% internal voltage reference enables high accuracy and low voltage capability at the output. Inductor DCR current sensing provides an accurate current limit detection method and promotes high output current and high system efficiency by eliminating resistive current sense elements.

This application note describes the steps taken in selecting the external components to build a fully functional DC/DC converter. Diagrams of the evaluation board layout and bill of materials are included at the end of this application note. The evaluation board represents a typical application circuit and can be modified if different specifications are desired. Please refer to the ***Design Guide*** section of the *LM27402 High Performance Synchronous Buck Controller with DCR Current Sensing* (SNVS615) data sheet for additional design equations.

2 Evaluation Board

The LM27402 evaluation board represents a 20A typical application circuit. The application circuit is optimized for an input voltage of 12V. However, input voltage feed-forward technology allows the evaluation board to operate up to 20V while maintaining a stable output voltage of 1.5V at 20A. Temperature compensated inductor DCR current limit circuitry provides a steady current limit set point. Extra MOSFET and input/output capacitor footprints are included to accommodate higher currents if desired. An externally set soft-start time of 10 ms provides a controlled monotonic startup. The LM27402 evaluation board also supports pre-biased startup and provides a tracking connection for power supply sequencing. An external clock can be applied to change the switching frequency through an on board synchronization connection. PGOOD is externally pulled up to VDD and can be monitored via an on board terminal. Two extra terminals are included to provide a network analyzer connection for control loop stability analysis. The PCB measures 1.3” x 1.8” and includes input/output banana connectors for the input supply and load.

3 Evaluation Board Operating Specifications

- Input Voltage = 4.5V to 20V
- Output Voltage = 1.5V
- Output Current = 0A to 20A

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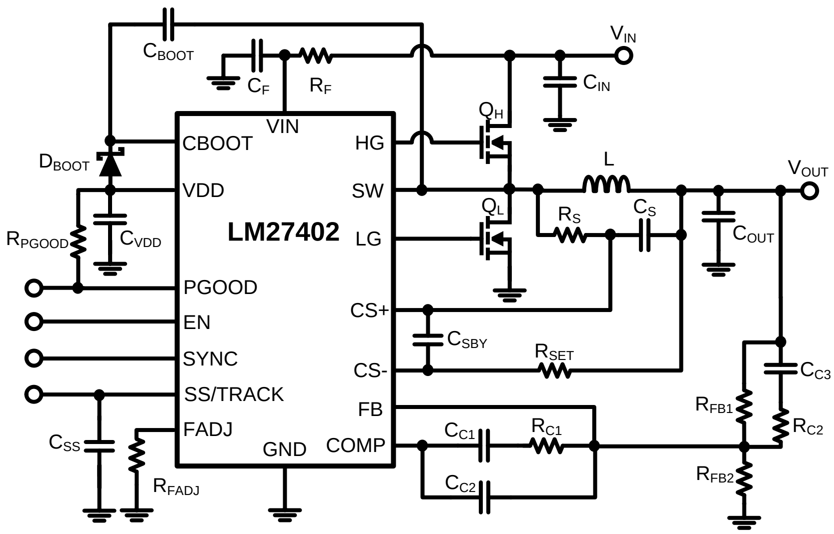

Figure 1. Simplified Application Schematic

4 Evaluation Board Schematic

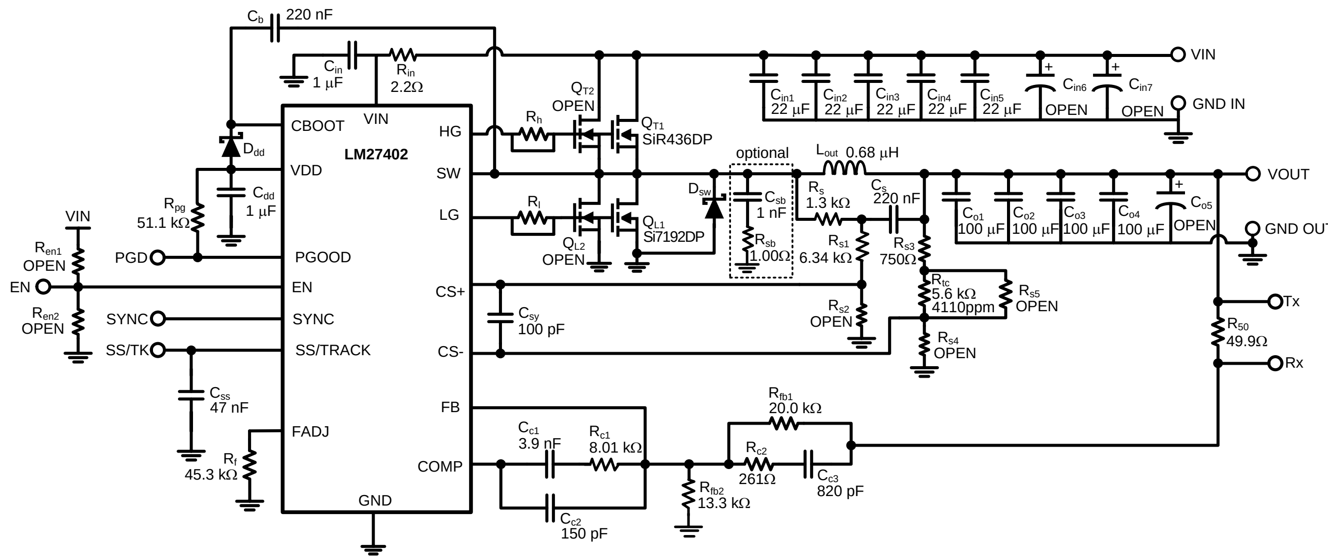

Figure 2. V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V, I_{OUT} = 20A

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5 Connection Descriptions

PCB Silkscreen	Description
VIN	VIN is the input voltage terminal to the PCB and is equipped to handle a 1/4" banana jack or can be unbolted to accept a ring connector. The LM27402 will operate over the input voltage range of 3.0V to 20V. However, the evaluation board is optimized for an input voltage of 12V and will operate from 4.5V to 12V. The absolute maximum voltage rating for this pin is 22V.
GND IN	GND IN is the input ground terminal to the PCB and is equipped to handle a 1/4" banana jack or can be unbolted to accept a ring connector. There are two GND connections on the PCB. GND IN should be used for the input supply only.
VOUT	VOUT is the output voltage terminal of the PCB and is equipped to handle a 1/4" banana jack or can be unbolted to accept a ring connector. VOUT should be connected to the load through a low impedance line to minimize any line drop.
GND OUT	GND OUT is the output ground terminal of the PCB and is equipped to handle a 1/4" banana jack or can be unbolted to accept a ring connector. There are two GND connections on the PCB. GND OUT should be used for the output load only.
VDD	VDD is the output of the internal 4.5V sub regulator.
PGD	PGOOD output. This connection allows the user to monitor PGOOD during fault conditions. PGOOD is pulled up to VDD and should not exceed 5.5V under normal operating conditions and the absolute maximum voltage rating is 6V.
EN	EN is connected to the EN pin of the LM27402. A voltage typically greater than 1.17V will enable the IC. A hysteresis of 100mV on EN provides noise immunity. The LM27402 will self enable by a 2 µA internal current source to EN if no control signal is applied to EN. The enable threshold can be set with an optional external resistor divider from VIN. The EN pin should not exceed the voltage on VDD. The operating voltage for this pin should not exceed 5.5V and the absolute maximum voltage rating is 6V.
SS/TK	SS/TK provides access to the SS/TRACK pin of the LM27402. Connections to this terminal are not needed for most applications. The feedback pin of the LM27402 will track the voltage on the SS/TRACK pin if driven with an external voltage source that is less than the 0.6V internal reference. The operating voltage for this pin should not exceed 5.5V and the absolute maximum voltage rating on this pin is 6V. The SS/TRACK pin should not exceed the voltage on VDD.
SYNC	SYNC connects to the SYNC pin of the LM27402. An external clock signal can be connected to the SYNC connection to set the switching frequency. If a SYNC signal is not present, the switching frequency will fall back to the frequency set by the FADJ resistor. The SYNC frequency must be greater than the frequency set by the FADJ resistor and can sync up to 400 kHz above the free running frequency. This pin should not exceed the voltage on VDD.
RX and TX	The RX and TX terminals provide the connections to measure the loop response with a network analyzer. Rx refers to an applied reference signal and Tx refers to the test voltage or in this case the output voltage. Between Rx and Tx exists a 50Ω termination resistor.

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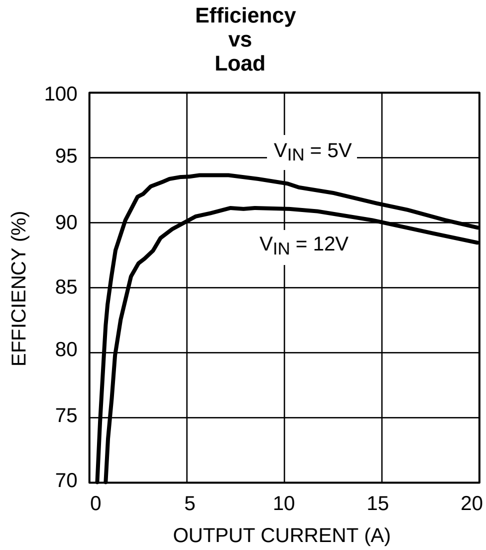
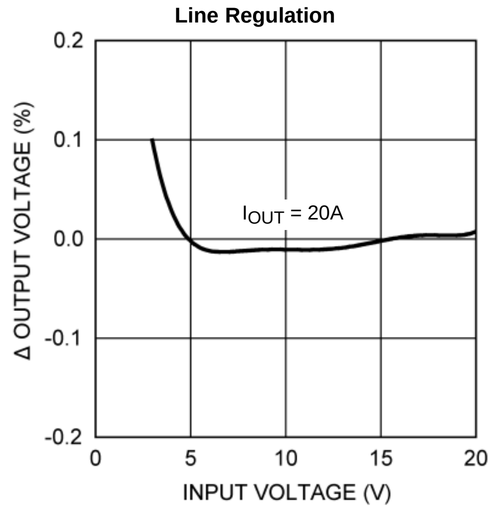
6 Performance Characteristics





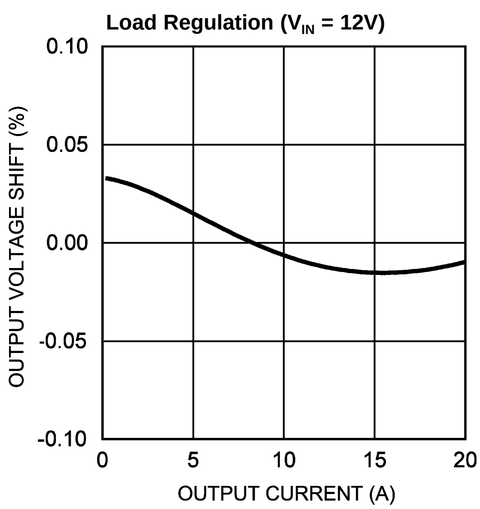


Figure .

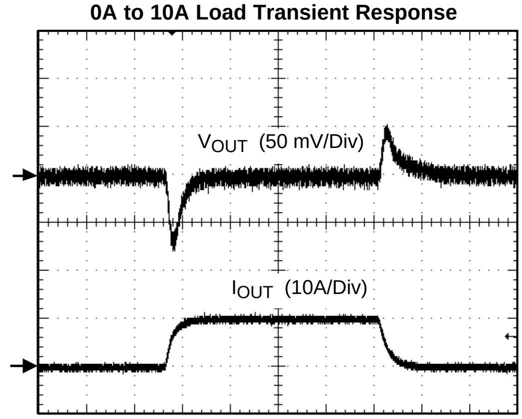


Figure . Figure 3. 100 µs/DIV

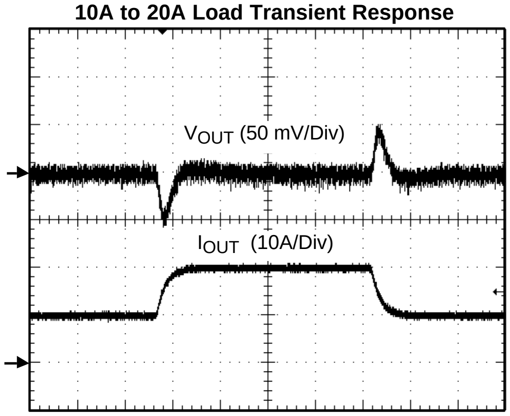


Figure . Figure 4. 100 µs/DIV

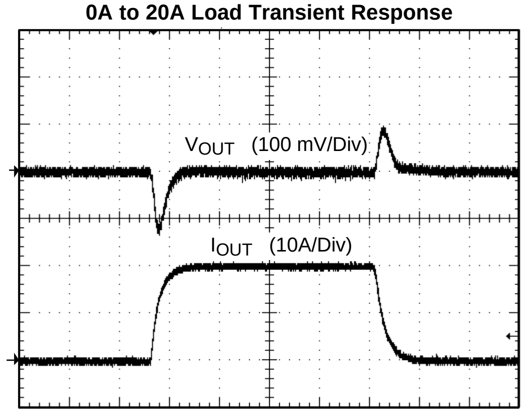


Figure . Figure 5. 100 µs/DIV

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Startup Waveform (No Load)

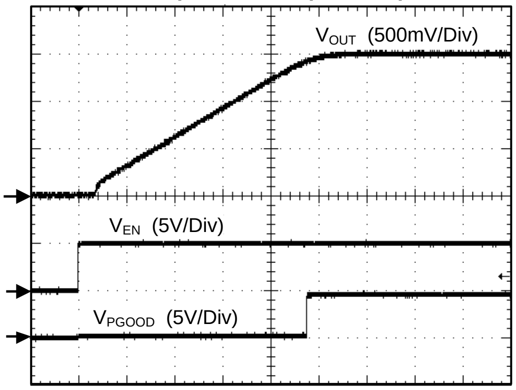

Figure . Figure 6. 2 ms/DIV

Startup Waveform (15A Electronic Load)

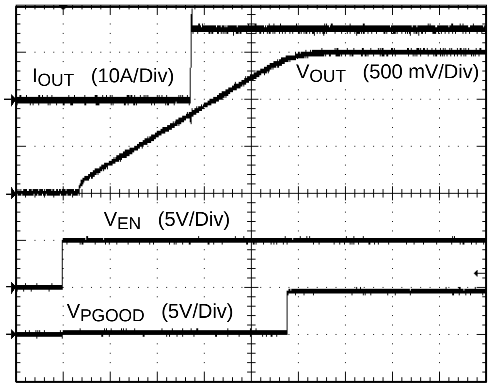

Figure . Figure 7. 2 ms/DIV

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7 LM27402 Evaluation Board

The LM27402 evaluation board is designed to support multiple applications and modifications and is optimized for a 4.5V to 12V input voltage range. The maximum steady state output current is set at 20A and will typically current limit at 24A. The PCB features bolt-on banana connections if heavy duty connectors are needed.

8 Setup Procedure

1. Set the input power supply voltage to 12V. Adjust the input supply current limit level to 10A to protect from any unanticipated shorts.
2. Turn the input power supply off. Connect the input supply positive terminal to the VIN terminal and the input supply ground terminal to the GND IN terminal.
3. Turn the output electronic load off. Connect the electronic load positive terminal to the VOUT terminal and the ground terminal to the GND OUT terminal of the LM27402 evaluation board
4. Turn the input supply on. The part will self enable and the output voltage should be 1.5V. Slowly increase the load current to 20A. The input voltage can now be adjusted as well.

CAUTION: If the input voltage is below 5V, the internal LDO will be in a drop out state. The output of the LDO provides the driving voltage across the gates of the MOSFETs. If the voltage at VDD decreases enough, the efficiency may suffer if the MOSFETs are not fully enhanced in the on-state. The output should maintain regulation.

9 Evaluation Board Component Selection

This section describes the design process for the LM27402 evaluation board. Unless otherwise indicated, all formulae assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance, and Volts (V) for voltage.

The first equation to calculate for any buck converter is duty ratio:

$$D = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta} \tag{1}$$

Due to the resistive powertrain losses, the duty ratio will increase based on the overall efficiency, η. Setting η = 1 yields an approximate result for D.

9.1 *Input Filter, R_{in}, C_{in}*

An RC filter is added to prevent any switching noise from interfering with the internal analog circuitry connected to VIN. The RC filter can be seen in the evaluation board schematic as components R_{in} and C_{in}. There is a practical limit to the value of resistor R_{in} as the VIN pin of the LM27402 will draw large bias currents to switch the gate of each MOSFET. If R_{in} is too large, the resulting voltage drop can disrupt normal operation. For the evaluation board, a 2.2Ω resistor in conjunction with a 1.0 µF 25V X5R ceramic capacitor is used for the input RC filter.

9.2 *Input Capacitors, C_{in1} - C_{in5}*

Input capacitors should be selected based on the required input voltage ripple and maximum RMS current rating. The required RMS current rating of the input capacitor for a buck regulator can be estimated by the following equation:

$$I_{CIN(RMS)} = I_{OUT}\sqrt{D(1 - D)} \tag{2}$$

From this equation, it follows that the maximum $I_{CIN(RMS)}$ requirement will occur at a full 20A load current with the system operating at 50% duty cycle. Under this condition, the maximum $I_{CIN(RMS)}$ is given by:

$$I_{CIN(RMS)} = 20A\sqrt{0.5 \times 0.5} = 10A \tag{3}$$

The voltage ripple can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{C_{IN} \times f_{SW}} + \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \times R_{ESR\_CIN} \tag{4}$$

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Ceramic capacitors feature a very large I_{RMS} rating in a small footprint, making a ceramic capacitor ideal for this application. Five 22 µF X5R 25V ceramic capacitors were selected to provide the necessary input capacitance for the evaluation board. Neglecting the effects of ESR, at 12V V_{IN} and 20A I_{OUT} the selected input capacitors yield an input voltage ripple of:

$$\Delta V_{IN} = \frac{20A \times 0.125 \times (1 - 0.125)}{110\ \mu F \times 300\ kHz} = 66\ mV \tag{5}$$

If desired, two extra capacitors can be added in the C_{in6} and C_{in7} footprints.

9.3 Inductor, L_{out}

As per datasheet recommendations, the inductor value should initially be chosen to produce a peak to peak ripple current between 20% and 40% of the maximum operating output current. A 30% current ripple was chosen for the LM27402 evaluation board. The minimum inductance required is calculated by:

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}} = \frac{(12V - 1.5V) \times 0.125}{(0.3 \times 20A) \times 300\ kHz} = 0.73\ \mu H \tag{6}$$

An actual inductor is selected based on a trade-off between physical size, efficiency, and current carrying capability. A Vishay IHLP5050 0.68 µH inductor results in a peak to peak current ripple of 6.4A and offers a balance between efficiency (2.34 mΩ DCR), size (12.9 mm x 13.2 mm), and saturation current rating (49A I_{SAT}).

9.4 Output Capacitor, C_{o1}- C_{o4}

The value of the output capacitor in a buck regulator influences the steady state voltage ripple as well as the output voltage response to a load transient. Given the peak-to-peak inductor current ripple (ΔI_L) the output voltage ripple can be approximated by:

$$\Delta V_{OUT} = \Delta I_L \times \sqrt{R_{ESR}^2 + \left(\frac{1}{8 \times f_{SW} \times C_{OUT}}\right)^2} \tag{7}$$

where ΔV_{OUT} (V) is the amount of peak-to-peak voltage ripple at the power supply output, R_{ESR} (Ω) is the series resistance of the output capacitor, f_{SW} (Hz) is the switching frequency, and C_{OUT} (F) is the output capacitance used in the design and is the sum of C_{o1} through C_{o4}. For the evaluation board, four 100 µF 6.3V X5R ceramic capacitors were selected for the output capacitance to provide adequate transient and DC bias performance in a relatively small package. From the technical specifications of this capacitor, the ESR is approximately 3 mΩ and the effective in-circuit capacitance is approximately 60 µF (reduced from 100 µF due to the 1.5V DC bias and worst case tolerance). With these values, the peak-to-peak voltage ripple when operating from a VIN of 12V is:

$$6.4A \times \sqrt{(0.75\ m\Omega)^2 + \left(\frac{1}{8 \times 300\ kHz \times 240\ \mu F}\right)^2} = 12\ mV_{p\text{-}p} \tag{8}$$

9.5 Soft-Start Capacitor, C_{ss}

A soft-start capacitor can be used to control the startup time of the LM27402. The startup time is estimated by the following equation:

$$t_{SS} = \frac{0.6V \times C_{SS}}{I_{SS}} \tag{9}$$

I_{SS} is nominally 3 µA. For the evaluation board, the soft-start time has been designed to be approximately 10 ms, resulting in a C_{ss} capacitor value of 47 nF. The LM27402 defaults to a 1.28 ms startup ramp time if C_{ss} is not used.

9.6 Internal LDO Bypass Capacitor, C_{dd}

The C_{dd} capacitor is necessary to bypass an internal 4.5V subregulator. This capacitor should be sized equal to or greater than 1 µF but less than 10 µF. A value of 1 µF is sufficient for most applications and is used in the LM27402 evaluation board.

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9.7 Frequency Adjust Resistor, R_f

The LM27402 switching frequency can be adjusted from 200 kHz to 1.2 MHz using an external resistor labeled on the evaluation board as R_f.The frequency of the LM27402 evaluation board was selected to be 300 kHz. A 300 kHz switching frequency enables the LM27402 to deliver high currents by reducing the MOSFET related losses while maintaining the ability to achieve satisfactory transient response. To find the value of resistance needed for a given frequency use the following equation: (f_{SW} (kHz), R_f (kΩ))

$$R_f = \frac{100}{\frac{f_{SW}}{100} - 1} - 5 = \frac{100}{\frac{300}{100} - 1} - 5 = 45\ k\Omega \tag{10}$$

A value of 45.7 kΩ was chosen for the R_f resistor on the LM27402 evaluation board.

9.8 Current Limit Circuitry, R_s, C_s, R_{s1}, R_{s5}, R_{tc}

The current limit circuitry included on the LM27402 evaluation board sets the current limit at 24A. Components R_s and C_s connect directly under the inductor pads and create an RC filter. The time constant of R_sC_s should match the time constant of the inductance and DCR of the inductor:

$$R_S C_S = \frac{L}{R_{DCR}} \tag{11}$$

A typical range of capacitance used in the R_sC_s network is 100 nF to 1 µF. A 220 nF capacitor was chosen for the C_s filter capacitor resulting in an R_s resistor of:

$$R_s = \frac{L_{out}}{C_s R_{DCR}} = \frac{0.68\ \mu H}{220\ nF \times 2.34\ m\Omega} = 1.32\ k\Omega \tag{12}$$

A standard value resistor of 1.3 kΩ was selected for R_s. The current limit level is set through a resistor from CS- to the VOUT pad of the inductor. The LM27402 evaluation board is set to current limit at 24A I_{OUT}. The maximum inductor current is $I_{OUT} + \Delta I_L/2 = 24 + 6.4/2 = 27.2A$. The next equation describes the current limit resistor calculation:

$$R_{SET} = \frac{I_{LIMIT} R_{DCR}}{I_{cs-}} = \frac{27.2A \times 2.34\ m\Omega}{10\ \mu A} = 6.36\ k\Omega \tag{13}$$

Copper resistance changes by about 3900 ppm/°C and can cause a significant error in the current limit setpoint. The LM27402 evaluation board is equipped with a 5.6 kΩ positive temperature coefficient resistor (R_{tc}) to compensate the effects of copper resistance and a 750Ω resistor R_{s3} in series with R_{tc} to approximately provide the 6.36 kΩ needed for R_{SET}. R_{tc} was chosen to be a Vishay TFPT1206L5601F 5.6 kΩ resistor which has a temperature coefficient of 4110 ppm/°C. An optional 6.34 kΩ resistor (R_{s1}) was placed between CS+ and the R_sC_s filter to mirror the impedance of the CS- pin in addition to a 100 pF capacitor placed between CS+ and CS- near the IC to reduce the effects of noise.

The internal 10 µA current source is powered from VIN. If the voltage between VIN and CS- is below 1V, the current source will supply less than 10 µA. If this happens, the common mode voltage of the current sense comparator inputs (CS+ and CS-) can be decreased to ensure 10 µA of current. Extra resistor pads (R_{s1}, R_{s2}, R_{s4}) are included in the LM27402 evaluation board to lower the common mode voltage. Please refer to *AN-2060 LM27402 Current Limit Application Circuits* (SNVA441) for design guidelines to adjust the common mode voltage of the current sense comparator.

9.9 Enable Resistors, R_{en1}, R_{en2}

The LM27402 evaluation board is equipped with an enable connection tied directly to EN. Resistor footprints R_{en1} and R_{en2} provide an optional voltage divider network from VIN to GND to program the LM27402 to enable at a certain input voltage. The following equation will guide the user in choosing resistors values to create a resistor divider for EN:

$$R_{en1} = \frac{R_{en2}(V_{IN} - 1.17V)}{1.17V - I_{EN} \times R_{en2}} \tag{14}$$

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9.10 Tracking

The LM27402 evaluation board is setup with a tracking connection (SS/TK). The SS/TK terminal is also the soft-start pin. If a voltage source is connected to the SS/TK connection of the board, the output can be controlled up to 1.5V (voltage set by the feedback resistors). The LM27402 will stop tracking when the SS/TK voltage exceeds 0.6V. Please refer to the datasheet for more details of the tracking function.

9.11 Compensation and Feedback, R_{fb1}, R_{c1}, R_{c2}, C_{c1}, C_{c2}, C_{c3}

In order for the LM27402 to regulate, the feedback loop must be closed and compensated. The LM27402 employs voltage mode control to regulate the output voltage. Voltage mode control requires the LC complex double pole caused by L_{out} and C_{o1}- C_{o5} to be compensated to reduce the likelihood of oscillation. The evaluation board incorporates type III compensation which adds three poles and two zeros to the open loop transfer function. The evaluation board is conservatively compensated to grant the user the freedom to make small changes to the powertrain circuitry while maintaining adequate stability. Please refer to the *LM27402 High Performance Synchronous Buck Controller with DCR Current Sensing* (SNVS615) data sheet for the type III compensator design equations. The compensation components include R_{fb1}, R_{fb2}, R_{c1}, R_{c2}, C_{c1}, C_{c2}, C_{c3}.

9.12 R_{fb1} and R_{fb2}

The resistors labeled R_{fb1} and R_{fb2} create a voltage divider from V_{OUT} to FB and FB to GND that is used to set the nominal output voltage of the regulator. Nominally, the output of the LM27402 evaluation board is set to 1.5V using resistor values of R_{fb1} = 20.0 kΩ and R_{fb2} = 13.3 kΩ. If a different output voltage is required, the value of R_{fb2} can be adjusted according to the equation:

$$R_{fb2} = \frac{R_{fb1}}{\left(\frac{V_{OUT}}{0.6} - 1\right)} \tag{15}$$

R_{fb1} does not need to be changed from its value of 20.0 kΩ.

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10 Bill of Materials

Designator	Type	Parameters	Part Number	Qty	Manufacturer
U_1	Synchronous Buck Controller		LM27402S	1	Texas Instruments
C_b	Capacitor	0.22 µF, Ceramic, X7R, 25V, 10%	GRM188R71E224KA88D	1	Murata
C_{c1}	Capacitor	3900 pF, Ceramic, X7R, 50V, 10%	GRM188R71H392KA01D	1	Murata
C_{c2}	Capacitor	150 pF, Ceramic, C0G, 50V, 5%	GRM1885C1H151JA01D	1	Murata
C_{c3}	Capacitor	820 pF, Ceramic, C0G, 50V, 5%	GRM1885C1H821JA01D	1	Murata
C_{dd}	Capacitor	1 µF, Ceramic, X5R, 25V, 10%	GRM188R61E105KA12D	1	Murata
C_{in}	Capacitor	1 µF, Ceramic, X5R, 25V, 10%	GRM188R61E105KA12D	1	Murata
C_{in1}, C_{in2}, C_{in3}, C_{in4}, C_{in5}	Capacitor	22 µF, Ceramic, X5R, 25V, 10%	GRM32ER61E226KE15L	5	Murata
C_{o1}, C_{o2}, C_{o3}, C_{o4}	Capacitor	100 µF, Ceramic, X5R, 6.3V, 20%	C1210C107M9PACTU	4	Kemet
C_s	Capacitor	0.22 µF, Ceramic, X7R, 25V, 10%	GRM188R71E224KA88D	1	Murata
C_{sb}	Capacitor	1000 pF, Ceramic, X7R, 50V, 10%	GRM188R71H102KA01D	1	Murata
C_{ss}	Capacitor	47000 pF, Ceramic, X7R, 16V, 10%	GRM188R71C473KA01D	1	Murata
C_{sy}	Capacitor	100 pF, Ceramic, C0G/NP0, 50V, 5%	GRM1885C1H101JA01D	1	Murata
D_{dd}	Diode	Schottky Diode, Average I = 100mA, Max Surge I = 750 mA	CMOSH-3	1	Central Semi
D_{sw}	Diode	Schottky Diode, Average I = 3A, Max Surge I = 80A	CMSH3-40M	1	Central Semi
L_{out}	Inductor	0.68 µH, 2.34 mΩ	IHLP5050CEERR68M06	1	Vishay
Q_{L1}	N-CH MOSFET	30V, 60A, 43.5 nC, $R_{DS(ON)}$ @ 4.5V = 1.85 mΩ	Si7192DP	1	Vishay
Q_{T1}	N-CH MOSFET	25V, 40A, 13 nC, $R_{DS(ON)}$ @ 4.5V = 6.2 mΩ	SiR436DP	1	Vishay
R_{50}	Resistor	49.9Ω, 1%, 0.1W	CRCW060349R9FKEA	1	Vishay
R_{c1}	Resistor	8.06 kΩ, 1%, 0.1W	CRCW06038k06FKEA	1	Vishay
R_{c2}	Resistor	261Ω, 1%, 0.1W	CRCW0603261RFKEA	1	Vishay
R_f	Resistor	45.3 kΩ, 1%, 0.1W	CRCW060345k3FKEA	1	Vishay
R_{fb1}	Resistor	20.0 kΩ, 1%, 0.1W	CRCW060320k0FKEA	1	Vishay
R_{fb2}	Resistor	13.3 kΩ, 1%, 0.1W	CRCW060313k3FKEA	1	Vishay
R_{in}	Resistor	2.2Ω, 5%, 0.1W	CRCW06032R20JNEA	1	Vishay
R_{pg}	Resistor	51.1 kΩ, 1%, 0.1W	CRCW060351k1FKEA	1	Vishay
R_s	Resistor	1.3 kΩ, 1%, 0.1W	CRCW06031k30FKEA	1	Vishay
R_{s1}	Resistor	6.34 kΩ, 1%, 0.1W	CRCW06036k34FKEA	1	Vishay
R_{s3}	Resistor	750Ω, 1%, 0.1W	CRCW0603750RFKEA	1	Vishay
R_{sb}	Resistor	1.0Ω, 1%, 0.125W	CRCW08051R00FNEA	1	Vishay
R_{tc}	Resistor	5.6 kΩ, 1%, 4110 ppm/°C	TFPT1206L5601F	1	Vishay
GND IN, GND OUT, VOUT, VIN	Power Terminal		3267	4	Panoma
VDD, PGD, SS/TK, SYNC, Rx, Tx	Turret Terminal		5002	6	Keystone

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11 PCB Component Placement

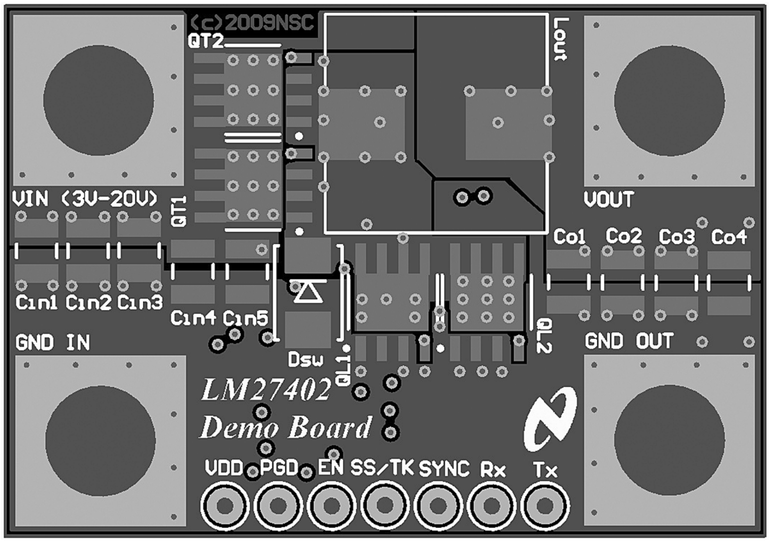

Figure 8. Top Layer

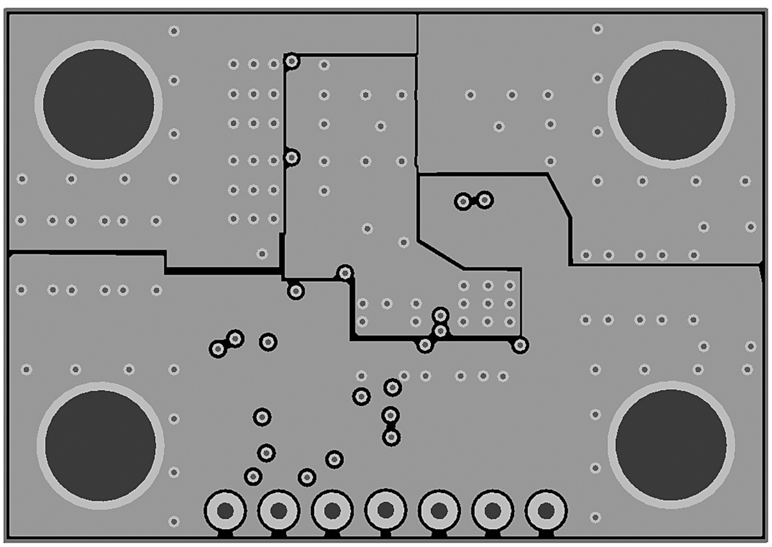

Figure 9. Mid Layer 1

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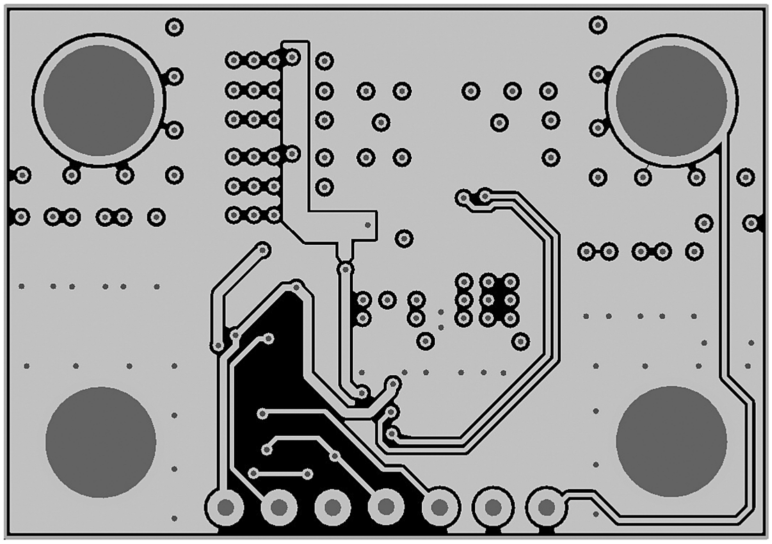

Figure 10. Mid Layer 2

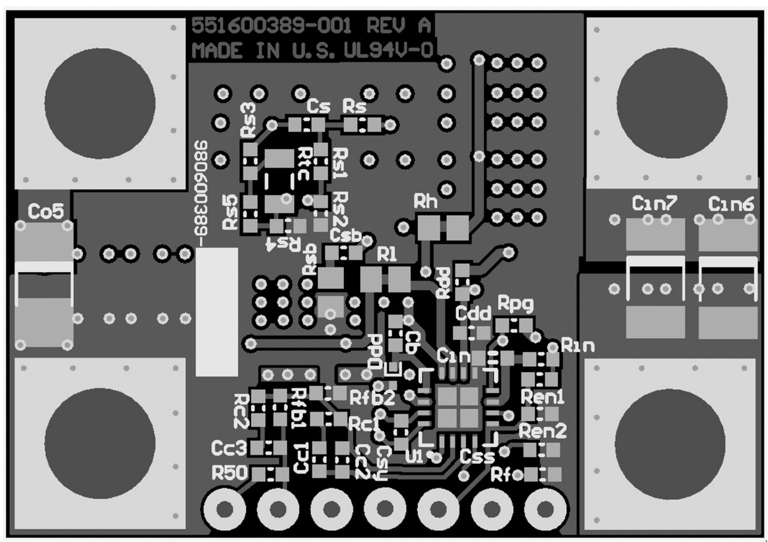

Figure 11. Bottom Layer (View From the Bottom)

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