IWR1642 Device Errata

1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (IWR1642).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / milli-meter Wave sensor devices. Each of the Radar devices has one of the two prefixes: XI or IWR (for example: **XI**1642QGABL). These prefixes represent evolutionary stages of product development from engineering prototypes (XI) through fully qualified production devices (IWR).

Device development evolutionary flow:

XI — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

IWR — Production version of the silicon die that is fully qualified.

XI devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 1 shows an example of the IWR1642 Radar Device's package symbolization.
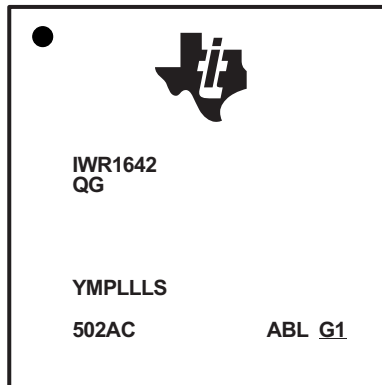

Figure 1. Example of Device Part Markings

This identifying number contains the following information:
- **Line 1:** Device Number
- **Line 2:** Temperature and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Code
  - PLLL = Assembly Lot
  - S = Assembly Site Code
- **Line 4:**
  - 502AC = IWR1642 Identifier
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Usage Notes

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These usage notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

4.1 MSS: SPI Speed in 3-Wire Mode Usage Note

The maximum SPI speed under 3-wire operation was only tested up to 33 MHz. This affects IWR1642 ES1.0.

5 Advisory to Silicon Variant / Revision Map

Table 1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	IWR16xx	
		ES1.0	ES2.0
Master Subsystem			
MSS#10	Partial Write After a Full Data Width Write Fails to Mailbox Memory if ECC is Enabled	X	
MSS#11	Clock Monitoring Logic Core Clock Comparator (CCCB) for CPU Clock Cannot be Used	X	
MSS#12	MCAN Filter Event Interrupt not Connected to DMA	X	
MSS#14	Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock	X	
MSS#16	Delay Time, ETM Trace Clock to ETM Data Valid does not Meet Datasheet Specification	X	
MSS#17	Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR	X	X
MSS#18[1]	Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application	X	X
MSS#19	DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario	X	X
Analog / Millimeter Wave			
ANA#06	Return Loss Measurement on TX: S11 < –9dB, RX S11 < –6.5dB (Accepted Value of < –10dB)	X	
ANA#08	Doppler Spur Observed for Narrow Chirps Spanning 79.2 GHz	X	X
ANA#09[1]	Synthesizer Frequency Nonlinearity at 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled	X	X
ANA#10[1]	Unreliable Readings from Synthesizer Supply Voltage Monitor	X	X
DSP Subsystem			
DSS#01	Access to L3 Region Above Allocated Region may Result in Double Bit ECC Error if ECC is Enabled	X	
DSS#02	L1P Parity Error not Connected to ESM	X	
DSS#03	Different Number of Chirps in ADC Buffer's Ping and Pong Memory is not Supported	X	
DSS#04	Partial Write After Full Data Width Write Fails to HS RAM, ADC Buffer and Data Transfer Memory if ECC is Enabled for that Memory	X	
DSS#05	Byte Writes not Supported to L3 If ECC is Enabled	X	
DSS#06	Available L3 RAM for Customer Application is Lesser by 128KB	X	
DSS#07	Temperature Sensor Located Near DSP not Working	X	

[1] Applies to SIL Targeted devices.

6 Known Design Exceptions to Functional Specifications

Table 2. Advisory List

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MSS#11 — Clock Monitoring Logic Core Clock Comparator (CCCB) for CPU Clock Cannot be Used	6
MSS#12 — MCAN Filter Event Interrupt not Connected to DMA	6
MSS#14 — Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock	6
MSS#16 — Delay Time, ETM Trace Clock to ETM Data Valid does not Meet Datasheet Specification	7
MSS#17 — Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR	7
MSS#18 — Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application	8
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DSS#05 — Byte Writes not Supported to L3 If ECC is Enabled	10
DSS#06 — Available L3 RAM for Customer Application is Lesser by 128KB	10
DSS#07 — Temperature Sensor Located Near DSP not Working	10

MSS#10   *Partial Write After a Full Data Width Write Fails to Mailbox Memory if ECC is Enabled*

Revision(s) Affected: IWR1642 ES1.0

Description: Partial data write after a full data width write would result is wrong data being written into the Mailbox memory if ECC is enabled.

Workaround(s):   None. Silicon update will be provided by TI.

MSS#11   *Clock Monitoring Logic Core Clock Comparator (CCCB) for CPU Clock Cannot be Used*

Revision(s) Affected: IWR1642 ES1.0

Description: Clock used for the Watchdog Timer (WDT) is same as the CPU clock. CCCB can be dedicated to monitor CPU clock against a reference clock like XTAL/RCOSC to generate a WDT reset if CPU clock fails. However, CCCB does not consistently generate an error if the CPU clock stops ticking

Workaround(s):   None. Silicon update will be provided by TI.

MSS#12   *MCAN Filter Event Interrupt not Connected to DMA*

Revision(s) Affected: IWR1642 ES1.0

Description: MCAN filter event interrupt is only connected to MSS VIM and not connected to MSS DMA. If a DMA transfer operation is expected to happen on this interrupt , MSS CR4 will have to trigger the DMA

Workaround(s):   None. Silicon update will be provided by TI.

MSS#14   *Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock*

Revision(s) Affected: IWR1642 ES1.0

Description: Asynchronous assertion of SoC warm reset through WARM_RESET pin, SW reset, watchdog reset, or Debug reset may not reliably work and may also result in a system hang scenario.

Workaround(s):   MSS VCLK must be switched from PLL clock to REFCLK by following the prescribed software sequence before a warm reset is issued.

MSS#16   *Delay Time, ETM Trace Clock to ETM Data Valid does not Meet Datasheet Specification*

Revision(s) Affected: IWR1642 ES1.0

Description: Delay time, ETM trace clock to ETM data valid does not meet datasheet specification below:

PARAMETER	MIN	MAX	UNIT
Delay time, ETM trace clock high to ETM data valid	1	7	ns
Delay time, ETM trace clock low to ETM data valid	1	7	ns

In IWR1642 ES1.0, Delay time, ETM trace clock to ETM data timing that is being met is as given below:

PARAMETER	MIN	MAX	UNIT
Delay time, ETM trace clock high to ETM data valid	−0.5	7	ns
Delay time, ETM trace clock low to ETM data valid	−0.5	7	ns

Workaround(s):   None.

MSS#17   *Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR*

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: The CR4 processor may perform an invalid pre-fetch access due to speculative TCM read leading to an invalid address access. This can result in a TCERROR and also a 2-bit ECC fatal error. The TCERROR is ignored by the processor since these correspond to instructions that are pre-fetched but never executed. However, the invalid MSS_TCMA_FATAL_ERR is generated on the ESM group3 channel-7.

Implication: In case of a genuine TCMA ECC fatal error, nERROR will not be generated directly through ESM.

Workaround(s):   Mask Group 3 channel 7: MSS_TCMA_FATAL_ERR to ESM can be masked by writing into MSS_RCM:ESMGATE0 register. CR4F abort handler should handle the nERROR generation

OR

Disable branch prediction for MSS-CR4F

MSS#18   ***Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application***

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: The CCM-R4F module compares the outputs of the two Cortex-R4F CPU cores and generates an error on any mis-compare. This ensures the lock-step operation of the two Cortex-R4F CPUs. The nERROR signal should only be set by the CCM-R4 module by a valid core mismatch. At power-on, some uninitialized circuits may cause the CCMR4-F to falsely detect a mis-compare.

Workaround(s):   The anomalous nERROR toggle would need to be ignored by the external monitoring circuit (if deployed).

MSS#19   ***DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario***

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: The MSS DMA generates a BER (Bus Error) interrupt when the DMA detects a bus error due to a read from unimplemented address space. This interrupt is available on VIM Interrupt Channel-70 for DMA1 and VIM Interrupt Channel-51 for DMA2 .This read from unimplemented address space results in a hang condition in the DMA infrastructure bridge that connects it to the main interconnect.

Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.

Workaround(s):   The MSS CR4F processor will have to invoke a warm reset or generate an nERROR if it receives a DMA BER error.

ANA#06   ***Return Loss Measurement on TX: S11 < −9dB, RX S11 < −6.5dB (Accepted Value of < −10dB)***

Revision(s) Affected: IWR1642 ES1.0

Description: The return loss measurement on TX S11 is < −9dB and the return loss measurement on RX S11 is < −6.5dB. The accepted value is < −10dB.

Workaround(s):   None. TI expects to provide an update along with the next silicon revision.

ANA#08   ***Doppler Spur Observed for Narrow Chirps Spanning 79.2 GHz***

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: There is a nonlinearity of the synthesizer when crossing 79.2 GHz due to coupling from its reference to the VCO.

Implication: There is a spur in non-zero Doppler bin if the synthesizer crosses 79.2 GHz during a chirp. The exact Doppler bin depends on the slope of the ramp. This is not observed for wide bandwidth or higher ramp slopes.

Workaround(s):   Avoid narrow, slow ramps near 79.2 GHz.

ANA#09   *Synthesizer Frequency Nonlinearity at 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled*

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: When the synthesizer (chirp) frequency monitor is enabled and the synthesizer chirp reaches 76.8 GHz, the frequency error can be as high as 500 kHz due to coupling between the monitor and the synthesizer.

Implication: Increased nonlinearity in the chirp can lead to up to 20 dB degradation in the noise floor surrounding large objects, including the bumper reflection. This leads to potential loss of dynamic range when large and small objects are present simultaneously.

Workaround(s):

1. Disable the synthesizer frequency monitor during profiles where the LO crosses 76.8GHz.
2. Use non-functional chirps to detect nonlinearities in the synthesizer.

ANA#10   *Unreliable Readings from Synthesizer Supply Voltage Monitor*

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: During monitoring, the thresholds used to determine if the synthesizer supply voltage is within limits are much stricter than necessary for proper circuit operation. This can lead to occasional, erroneous reporting of supply failures even when there is no adverse impact on circuit or system behavior.

Implication: The user cannot rely on supply failure indication from the supply monitors of PM, Clock and LO subsystems. The affected field is STATUS_SUPPLY_PMCLKLO in the monitoring report message: AWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.

Workaround(s):   Ignore the field STATUS_SUPPLY_PMCLKLO in the monitoring report message: AWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.

DSS#01   *Access to L3 Region Above Allocated Region may Result in Double Bit ECC Error if ECC is Enabled*

Revision(s) Affected: IWR1642 ES1.0

Description: Access to L3 region above allocated region may result in a Double Bit ECC error in addition to the data abort if ECC is enabled.

Workaround(s):   None. Silicon update will be provided by TI.

DSS#02   *L1P Parity Error not Connected to ESM*

Revision(s) Affected: IWR1642 ES1.0

Description: L1P parity error is only connected to DSP and not connected to MSS ESM.

Workaround(s):   None. Silicon update will be provided by TI.

DSS#03   *Different Number of Chirps in ADC Buffer's Ping and Pong Memory is not Supported*

Revision(s) Affected:	IWR1642 ES1.0
Description:	Different number of chirps in ADC buffer's ping and pong memory is not supported. They need to be programmed to a same value and the configuration for number of chirps in Ping and Pong can only be changed at Sub-Frame boundary.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#04   *Partial Write After Full Data Width Write Fails to HS RAM, ADC Buffer and Data Transfer Memory if ECC is Enabled for that Memory*

Revision(s) Affected:	IWR1642 ES1.0
Description:	Partial data write after a full data width write would result is wrong data being written into HS RAM , ADC buffer and Data Transfer memory if ECC is enabled for that memory.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#05   *Byte Writes not Supported to L3 If ECC is Enabled*

Revision(s) Affected:	IWR1642 ES1.0
Description:	Byte writes are not supported to L3 memory when ECC is enabled. ECC invalidation does not work correctly in this scenario.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#06   *Available L3 RAM for Customer Application is Lesser by 128KB*

Revision(s) Affected:	IWR1642 ES1.0
Description:	Due to available RAM being used for Radar block development, RAM available for user application is limited to 640 KB instead of 768 KB.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#07   *Temperature Sensor Located Near DSP not Working*

Revision(s) Affected:	IWR1642 ES1.0
Description:	The temperature sensor that is located near the DSP is not working in IWR1642 ES1.0. This is a known bug that will be fixed in ES2.0. There are eight temperature sensors located throughout the analog, all of which are working and accessible via an API call.
Workaround(s):	None. Silicon update will be provided by TI.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.