TEXAS INSTRUMENTS

ISO7220A, ISO7220B
ISO7220C, ISO7220M, ISO7221A
ISO7221B, ISO7221C, ISO7221M

SLLS755M – JULY 2006 – REVISED OCTOBER 2014

ISO722x Dual Channel Digital Isolators

1 Features

- 1, 5, 25, and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1-ns max
  - Low Pulse-Width Distortion (PWD); 1-ns max
  - Low Jitter Content; 1 ns Typ at 150 Mbps
- 50 kV/μs Typical Transient Immunity
- Operates with 2.8-V (C-Grade), 3.3-V or 5-V Supplies
- 4-kV ESD Protection
- High Electromagnetic Immunity
- –40°C to 125°C Operating Range
- Typical 28-Year Life at Rated Voltage (see application report *High-Voltage Lifetime of the ISO72x Family of Digital Isolators* (SLLA197) and Figure 23)
- VDE Basic Insulation with 4000-V_{PK} V_{IOTM}, 560 V_{PK} V_{IORM} per DIN EN 60747-5-5 (VDE 0884-5) and DIN EN 61010-1 (VDE 0411-1)
- 2500 V_{RMS} Isolation per UL 1577
- CSA Approved for Component Acceptance Notice 5A and IEC 60950-1

2 Applications

- Industrial Fieldbus
  - Modbus
  - Profibus™
  - DeviceNet™ Data Buses
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

3 Description

The ISO7220 and ISO7221 are dual-channel digital isolators. To facilitate PCB layout, the channels are oriented in the same direction in the ISO7220 and in opposite directions in the ISO7221. These devices have a logic input and output buffer separated by TI's silicon-dioxide (SiO_2) isolation barrier, providing galvanic isolation of up to 4000 V_{PK} per VDE. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

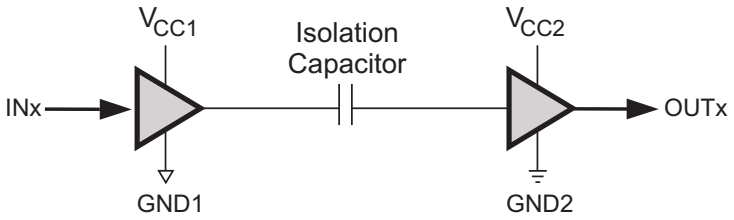
A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received every 4 μs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7220A	SOIC (8)	4.90 mm x 3.91 mm
ISO7220B		
ISO7220C		
ISO7220M		
ISO7221A		
ISO7221B		
ISO7221C		
ISO7221M		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision L (January 2012) to Revision M **Page**

- Changed the title of this data sheet to *ISO722x Dual Channel Digital Isolators* ... 1
- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Dissipation Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section, changed *Thermal Information* table ... 1
- Updated the Features section ... 1
- Added per VDE to 4000 V_{PK} in second sentence of Description ... 1
- Changed location of Device I/O Schematics to Feature Description section and replaced with new Simplified Schematic ... 1
- Updated the *Regulatory Information* Table ... 6
- Added the min and max values ... 6
- Changed in ROC table Max col, V_{IH} row from VCC to 5.5 ... 7
- Changed the Device Options table, Input Threshold column from ≠ symbol to ~ symbol 6 places ... 21
- Changed the 7.4 title from IEC 60747 ~2 Insulation Characteristics to DIN EN ~ 5 Insulation Characteristics ... 21
- Changed Isolation Glossary ... 27

Changes from Revision K (January 2010) to Revision L **Page**

- Changed Feature From: Operates with 3.3-V or 5-V Supplies To: Operates with 2.8-V (C-Grade), 3.3-V or 5-V Supplies . 1
- Changed Feature From: 4000-V_{peak} Isolation, 560 V_{peak} V_{IORM} To: 4000-V_{PK} V_{IOTM}, 560 V_{PK} V_{IORM} per IEC 60747-5-2 (VDE 0884, Rev2) 1
- Added device options to V_{CC} in the RECOMMENDED OPERATING CONDITIONS table 7
- Changed Note: (1) in the RECOMMENDED OPERATING CONDITIONS table 7
- Changed I_{CC1} and I_{CC2} test conditions in the 5-V table 8
- Changed Table Note: (1) 8
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} at 5 V, V_{CC2} at 3.3 V table 9
- Changed Table Note: (1) 9
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} at 3.3 V, V_{CC2} at 5 V table 10
- Changed Table Note (1) 10
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} and V_{CC2} at 3.3 V table 11
- Changed Table Note (1) 11
- Added ELECTRICAL and Switching CHARACTERISTICS table for V_{CC1} and V_{CC2} at 2.8 V (ISO722xC-Only) 12
- Changed Figure 9 17
- Changed Figure 14 19
- Changed the CTI MIN value From: ≥175 V To: ≥400 V 22
- Changed the REGULATORY INFORMATION table 23

Changes from Revision J (May 2009) to Revision K **Page**

- Changed the RECOMMENDED OPERATING CONDITIONS so that Note (2) is associated with all device options in the Input pulse width and Signaling rate 7
- Changed Note (2) From: Typical signaling rate under ideal conditions at 25°C. To: Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C. 7
- Changed column 2 of the AVAILABLE OPTIONS table From: Signaling Rate To: Max Signaling Rate 21

Changes from Revision I (December 2008) to Revision J **Page**

- Changed ISO7221C Marked As column From: TI7221C To: I7221C in the AVAILABLE OPTIONS table 21

Changes from Revision H (May 2008) to Revision I **Page**

- Added "IEC 61010-1, IEC 60950-1 and CSA Approved" to the UL 1577 FEATURES bullet 1

Changes from Revision G (March 2008) to Revision H **Page**

- Added Note: (1) to the RECOMMENDED OPERATING CONDITIONS table 7
- Added Note: (1) to the ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V table 8
- Added Note: (1) to the ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V table 9
- Added Note (1): to the ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V table 10
- Added Note (1): to the ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V 11

Changes from Revision F (August 2007) to Revision G **Page**

- Added Part Numbers ISO7220B and ISO7221B to the data sheet ... 1
- Added 5-Mbps Signaling rate to the FEATURES list ... 1
- Added Part Numbers ISO7220B and ISO7221B to the ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V table ... 8
- Added Part Numbers ISO7220B and ISO7221B to the ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V table ... 9
- Added Part Numbers ISO7220B and ISO7221B to the ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V table ... 10
- Added Part Numbers ISO7220B and ISO7221B to the ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V ... 11
- Added PROPAGATION DELAY vs FREE-AIR TEMPERATURE, ISO722xB, Figure 4 ... 17
- Added Part Numbers ISO7220B and ISO7221B to the AVAILABLE OPTIONS table ... 21

Changes from Revision E (July 2007) to Revision F **Page**

- Added $t_{sk(pp)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION table ... 13
- Added $t_{sk(o)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION table ... 13
- Added $t_{sk(pp)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION table ... 14
- Added $t_{sk(o)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION table ... 14
- Added $t_{sk(pp)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERATION table ... 15
- Added $t_{sk(o)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERTAION table ... 15
- Added $t_{sk(pp)}$ footnote to the SWITCHING CHARACTERISTICS table ... 16
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- Changed Figure 1 - Re-scaled the Y-axis ... 17
- Changed Figure 2 - New Curves ... 17

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- Changed Figure 1 - New Curves ... 17
- Changed Figure 2- Re-scaled the Y-axis ... 17

Changes from Revision C (May 2007) to Revision D **Page**

- Changed Figure 21 - Pin 2 (INA) label From: OUTPUT to INPUT ... 25

Changes from Revision B (May 2007) to Revision C **Page**

- Added the Signaling rate values to the RECOMMENDED OPERATING CONDITIONS table ... 7
- Added Figure 12 cross reference to the Peak-to-peak eye-pattern jitter of the SWITCHING CHARACTERISTICS table ... 13
- Added Figure 12 cross reference to the Peak-to-peak eye-pattern jitter of the SWITCHING CHARACTERISTICS table ... 14
- Added Figure 12 cross reference to the Peak-to-peak eye-pattern jitter of the SWITCHING CHARACTERISTICS table ... 15
- Added Figure 12 cross reference to the Peak-to-peak eye-pattern jitter of the SWITCHING CHARACTERISTICS table ... 16
- Changed the IEC 60664-1 RATINGS TABLE - Specification I-III test conditions From: Rated mains voltage ≤150 VRMS To: Rated mains voltage ≤300 VRMS. Added a row for the I-II specifications ... 22
- Added Figure 23 - Time Dependent Dielectric Breakdown Test Results ... 25

Changes from Revision A (August 2006) to Revision B **Page**

Changes from Original (July 2006) to Revision A **Page**

6 Description Continued

The small capacitance and resulting time constant provide fast operation with signaling rates available from 0 Mbps (dc) to 150 Mbps. (1) The A-, B- and C-option devices have TTL input thresholds and a noise filter at the input that prevents transient pulses from being passed to the output of the device. The M-option devices have CMOS $V_{CC}/2$ input thresholds and do not have the input noise-filter and the additional propagation delay.

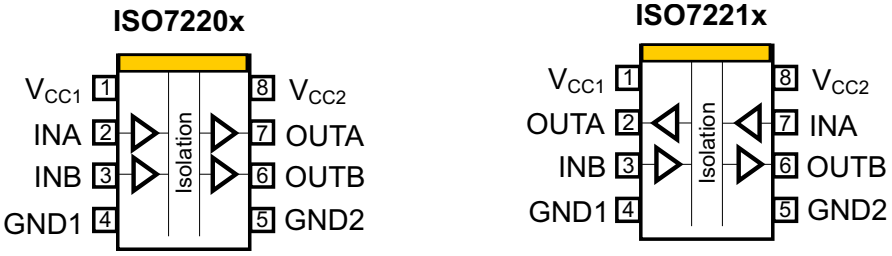
These devices require two supply voltages of 2.8 V (C-Grade), 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 2.8-V or 3.3-V supply and all outputs are 4-mA CMOS.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

7 Pin Configuration and Functions

D Package
8-Pin
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	ISO7220x	ISO7221x		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	8	8	—	Power supply, V_{CC2}

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at IN, OUT	–0.5	6	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		170	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground pin and are peak voltage values.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–4	4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1	1	
		Machine Model, ANSI/ESDS5.2-1996	–200	200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}	ISO722xA, ISO722xB, ISO722xM	3		5.5	V
		ISO722xC	2.8		5.5	
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width(2)	ISO722xA	1	0.67		µs
		ISO722xB	200	100		ns
		ISO722xC	40	33		
		ISO722xM	6.67	5		
$1/t_{ui}$	Signaling rate(2)	ISO722xA	0	1500	1000	kbps
		ISO722xB	0	10	5	Mbps
		ISO722xC	0	30	25	
		ISO722xM	0	200	150	
V_{IH}	High-level input voltage	ISO722xA, ISO722xB, ISO722xC	2		5.5	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IH}	High-level input voltage	ISO722xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.3 V_{CC}	V
T_J	Junction temperature		–40		150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 & IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.
For the 2.8-V operation, V_{CC1} or V_{CC2} is specified at 2.8 V.
(2) Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C.

8.4 Thermal Information

THERMAL METRIC(1)			ISO7220x, ISO7221x	UNIT
			D	
			8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Thermal Resistance(2)	212	°C/W
		High-K Thermal Resistance	122	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		69.1	
$R_{\theta JB}$	Junction-to-board thermal resistance		47.7	
ψ_{JT}	Junction-to-top characterization parameter		15.2	
ψ_{JB}	Junction-to-board characterization parameter		47.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).
(2) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

8.5 Dissipation Ratings

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device Power Dissipation	ISO722xM	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, Input a 150 Mbps 50% duty cycle square wave			390	mW

8.6 Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V[(1)] Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		1	2	mA
	ISO7221				8.5	17	
	ISO7220A, ISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		2	3	
	ISO7221A, ISO7221B				10	18	
	ISO7220C, ISO7220M	25 Mbps	12.5 MHz Input Clock Signal, no load		4	9	
	ISO7221C, ISO7221M				12	22	
I_{CC2}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		16	31	
	ISO7221x				8.5	17	
	ISO7220A, ISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		17	32	
	ISO7221A, ISO7221B				10	18	
	ISO7220C, ISO7220M	25 Mbps	12.5 MHz Input Clock Signal, no load		20	34	
	ISO7221C, ISO7221M				12	22	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 13	V_{CC} – 0.8	4.6		V
			I_{OH} = –20 µA, See Figure 13	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 13		0.2	0.4	V
			I_{OL} = 20 µA, See Figure 13		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 15	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.

8.7 Electrical Characteristics: V_{CC1} at 5 V, V_{CC2} at 3.3 V[1] Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		1	2	mA
	ISO7221x				8.5	17	
	ISO7220A, ISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		2	3	
	ISO7221A, ISO7221B				10	18	
	ISO7220C, ISO7220M	25 Mbps	12.5 MHz Input Clock Signal, no load		4	9	
	ISO7221C, ISO7221M				12	22	
I_{CC2}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		8	18	
	ISO7221x				4.3	9.5	
	ISO7220A, ISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		9	19	
	ISO7221A, ISO7221B				5	11	
	ISO7220C, ISO7220M	25 Mbps	12.5 MHz Input Clock Signal, no load		10	20	
	ISO7221C, ISO7221M				6	12	
V_{OH}	High-level output voltage	ISO7220x	I_{OH} = –4 mA, See Figure 13	V_{CC} – 0.4			V
		ISO7221x (5-V side)		V_{CC} – 0.8			
			I_{OH} = –20 µA, See Figure 13	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 13			0.4	V
			I_{OL} = 20 µA, See Figure 13			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 15	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

8.8 Electrical Characteristics: V_{CC1} at 3.3 V, V_{CC2} at 5 V[(1)] Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		0.6	1	mA
	ISO7221x				4.3	9.5	
	ISO7220A, ISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		1	2	
	ISO7221A, ISO7221B				5	11	
	ISO7220C, ISO7220M	25 Mbps	12.5 MHz Input Clock Signal, no load		2	4	
	ISO7221C, ISO7221M				6	12	
I_{CC2}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		16	31	
	ISO7221x				8.5	17	
	ISO7220A, ISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		18	32	
	ISO7221A, ISO7221B				10	18	
	ISO7220C, ISO7220M	25 Mbps	12.5 MHz Input Clock Signal, no load		20	34	
	ISO7221C, ISO7221M				12	22	
V_{OH}	High-level output voltage	ISO7220x	I_{OH} = –4 mA, See Figure 13	V_{CC} – 0.8			V
		ISO7221x (3.3-V side)		V_{CC} – 0.4			
			I_{OH} = –20 µA, See Figure 13	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		IOL = 4 mA, See Figure 13			0.4	
			IOL = 20 µA, See Figure 13		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 15	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

8.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V[1] Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		0.6	1	mA
	ISO7221x				4.3	9.5	
	ISO7220A, ISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		1	2	
	ISO7221A, ISO7221B				5	11	
	ISO7220C, ISO7220M	25 Mbps	12.5 MHz Input Clock Signal, no load		2	4	
	ISO7221C, ISO7221M				6	12	
I_{CC2}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		8	18	
	ISO7221x				4.3	9.5	
	ISO7220A, ISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		9	19	
	ISO7221A, ISO7221B				5	11	
	ISO7220C, ISO7220M	25 Mbps	12.5 MHz Input Clock Signal, no load		10	20	
	ISO7221C, ISO7221M				6	12	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 13	V_{CC} – 0.4	3		V
			I_{OH} = –20 µA, See Figure 13	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 13		0.2	0.4	
			I_{OL} = 20 µA, See Figure 13		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 15		15	40		kV/µs

(1) For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

8.10 Electrical Characteristics: V_{CC1} and V_{CC2} at 2.8 V (ISO722xC-Only)[1] Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220C	Quiescent	V_I = V_{CC} or 0 V, no load		0.4	0.9	mA
	ISO7221C				3.7	7.5	
	ISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		1.5	3.5	
	ISO7221C				4.5	10	
I_{CC2}	ISO7220C	Quiescent	V_I = V_{CC} or 0 V, no load		6.8	15	
	ISO7221C				3.7	7.5	
	ISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		9	17	
	ISO7221C				4.5	10	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 13	V_{CC} – 0.6	2.55		V
			I_{OH} = –20 µA, See Figure 13	V_{CC} – 0.1	2.8		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 13		0.25	0.6	
			I_{OL} = 20 µA, See Figure 13		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 15		10	30		kV/µs

(1) 2.8-V operation is only guaranteed for ISO722xC with production screening starting in January 2012. The first two digits of the Lot Trace Code (YMSLLLLG4) written on top of each device can be used to identify year and month of production respectively.

8.11 Switching Characteristics: V_{CC1} and V_{CC2} at 5 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA	See Figure 13	280	405	475	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xA	See Figure 13		1	14	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB	See Figure 13	42	55	70	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xB	See Figure 13		1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC	See Figure 13	22	32	42	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xC	See Figure 13		1	2	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM	See Figure 13	6	10	16	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xM	See Figure 13		0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				180	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xB				17	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xC				10	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xM				3	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xB			0.6	3	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xC/M			0.2	1	ns
t_r	Output signal rise time		See Figure 13		1		ns
t_f	Output signal fall time		See Figure 13		1		ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 14		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 16, Figure 12		1		ns
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps unrestricted bit run length data input, both channels, See Figure 16		2		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

8.12 Switching Characteristics: V_{CC1} at 5 V, V_{CC2} at 3.3 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA	See Figure 13	285	410	480	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xA	See Figure 13		1	14	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB	See Figure 13	45	58	75	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xB	See Figure 13		1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC	See Figure 13	25	36	48	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xC	See Figure 13		1	2	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM	See Figure 13	7	12	20	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xM	See Figure 13		0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				180	ns
		ISO722xB				17	
		ISO722xC				10	
		ISO722xM				5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	ns
		ISO722xB			0.6	3	
		ISO722xC/M			0.2	1	
t_r	Output signal rise time		See Figure 13		2		ns
t_f	Output signal fall time		See Figure 13		2		ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 14		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 16, Figure 12		1		ns
		ISO722xM	150 Mbps unrestricted bit run length data input, both channels, See Figure 16		2		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

8.13 Switching Characteristics: V_{CC1} at 3.3 V, V_{CC2} at 5 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA	See Figure 13	285	395	480	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xA	See Figure 13		1	18	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB	See Figure 13	45	58	75	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xB	See Figure 13		1	4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC	See Figure 13	25	36	48	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xC	See Figure 13		1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM	See Figure 13	7	12	21	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xM	See Figure 13		0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				190	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xB				17	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xC				10	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xM				5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xB			0.6	3	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220C/M			0.2	1	ns
t_r	Output signal rise time		See Figure 13		1		ns
t_f	Output signal fall time		See Figure 13		1		ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 14		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 16, Figure 12		1		ns
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps unrestricted bit run length data input, both channels, See Figure 16		2		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

8.14 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA	See Figure 13	290	400	485	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xA	See Figure 13		1	18	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB	See Figure 13	46	62	78	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xB	See Figure 13		1	4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC	See Figure 13	26	40	52	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xC	See Figure 13		1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM	See Figure 13	8	16	25	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xM	See Figure 13		0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				190	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xB				17	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xC				10	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xM				5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xB			0.6	3	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xC/M			0.2	1	ns
t_r	Output signal rise time		See Figure 13		2		ns
t_f	Output signal fall time		See Figure 13		2		ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 14		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 16, Figure 12		1		ns
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps unrestricted bit run length data input, both channels, See Figure 16		2		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

8.15 Switching Characteristics: V_{CC1} and V_{CC2} at 2.8 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC	See Figure 13	26	45	65	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)	ISO722xC	See Figure 13		1.5	5	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xC				12	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xC			0.2	5	ns
t_r	Output signal rise time		See Figure 13		2		ns
t_f	Output signal fall time		See Figure 13		2		ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 14		4.6		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

8.16 Typical Characteristics

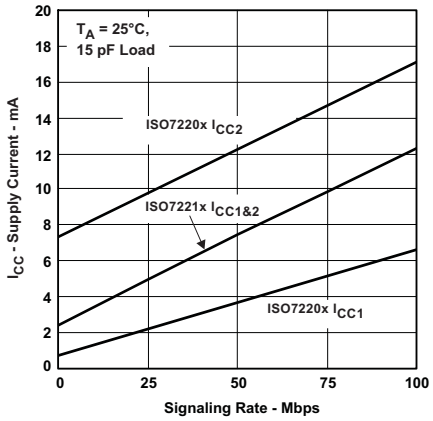


Figure 1. 3.3-V RMS Supply Current vs Signaling Rate (Mbps)

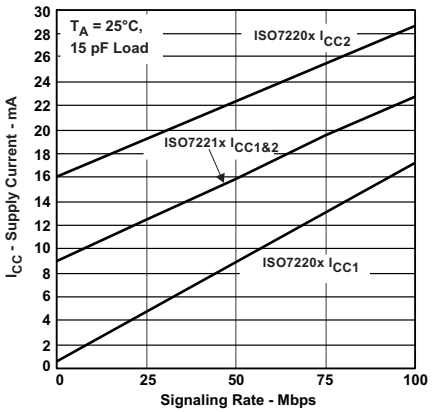


Figure 2. 5-V RMS Supply Current vs Signaling Rate (Mbps)

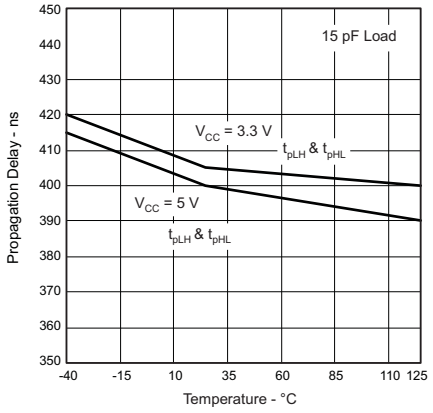


Figure 3. Propagation Delay vs Free-Air Temperature, ISO722xA

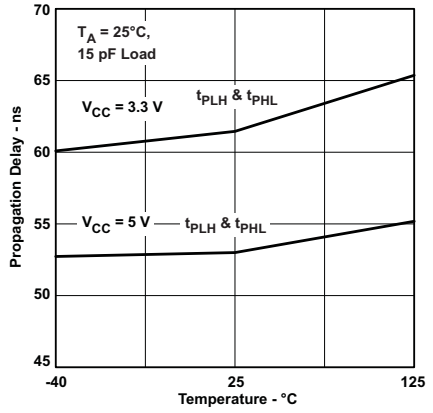


Figure 4. Propagation Delay vs Free-Air Temperature, ISO722xB

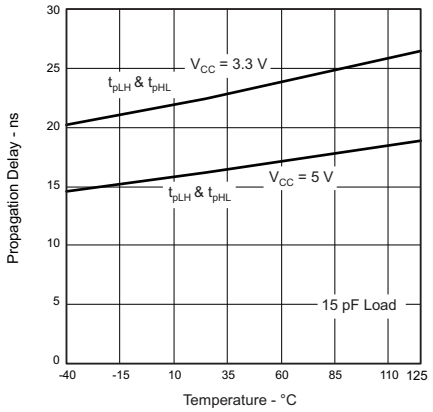


Figure 5. Propagation Delay vs Free-Air Temperature, ISO722xC

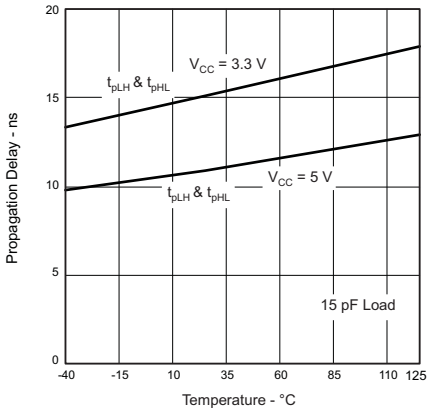


Figure 6. Propagation Delay vs Free-Air Temperature, ISO722xM

Typical Characteristics (continued)

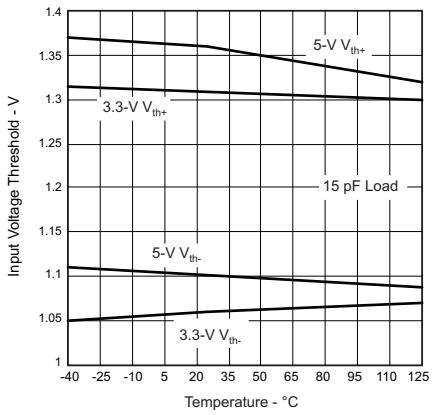


Figure 7. ISO722xA, ISO722xB and ISO722xC Input Voltage Low-to-High Switching Threshold vs Free-Air Temperature

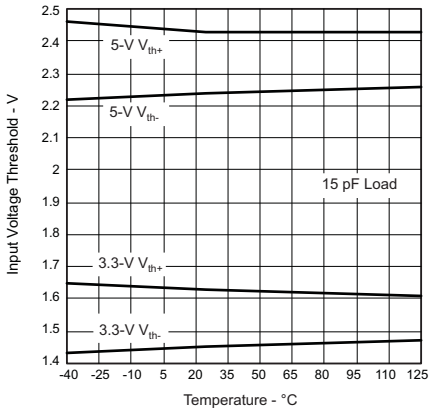


Figure 8. ISO722xM Input Voltage High-to-Low vs Free-Air Temperature

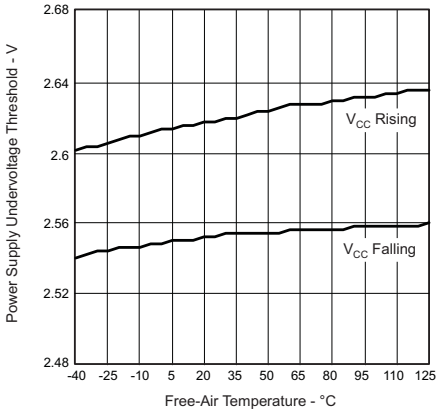


Figure 9. V_{CC} Undervoltage Threshold vs Free-Air Temperature

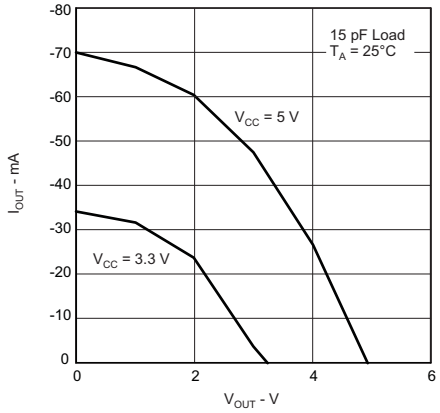


Figure 10. High-Level Output Current vs High-Level Output Voltage

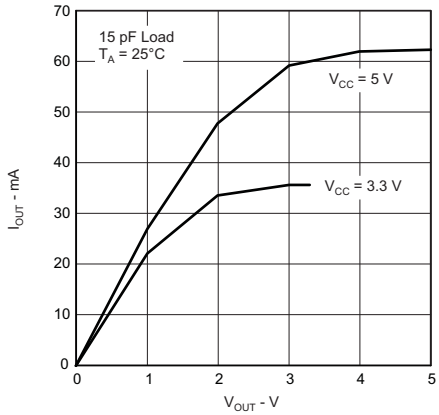


Figure 11. Low-Level Output Current vs Low-Level Output Voltage

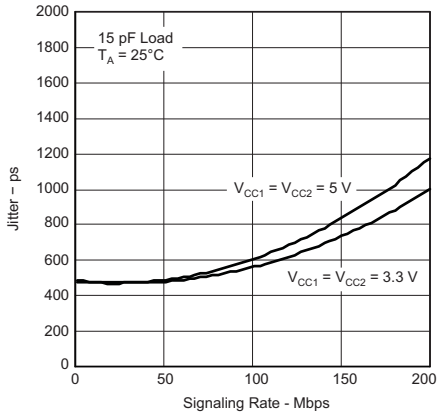
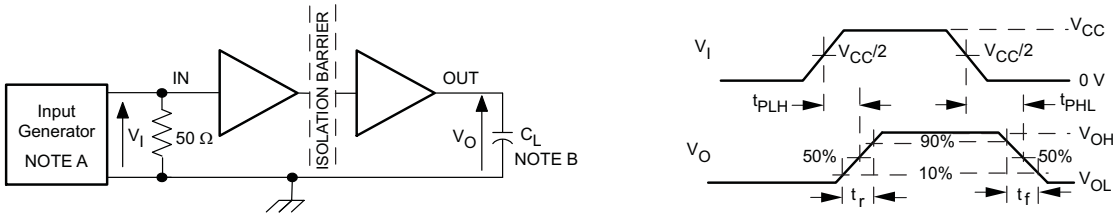


Figure 12. ISO722xM Jitter vs Signaling Rate

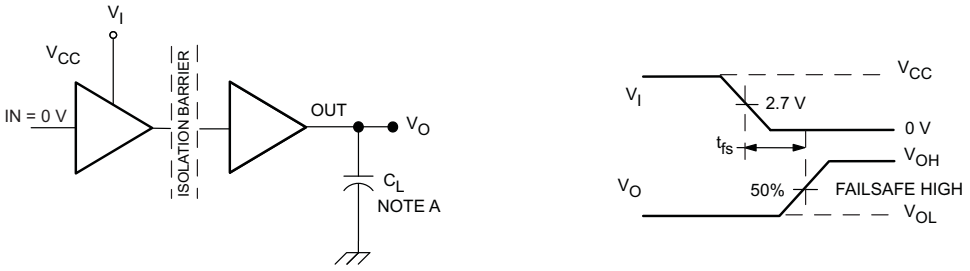
9 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

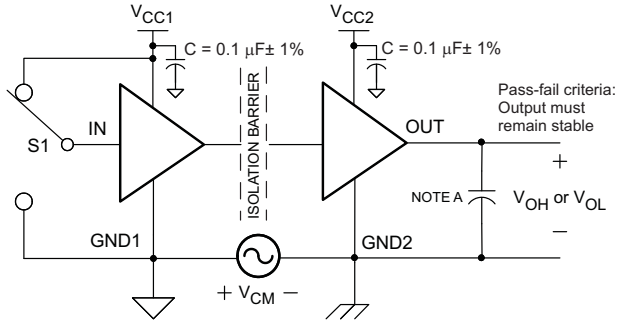
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

Figure 13. Switching Characteristic Test Circuit and Voltage Waveforms



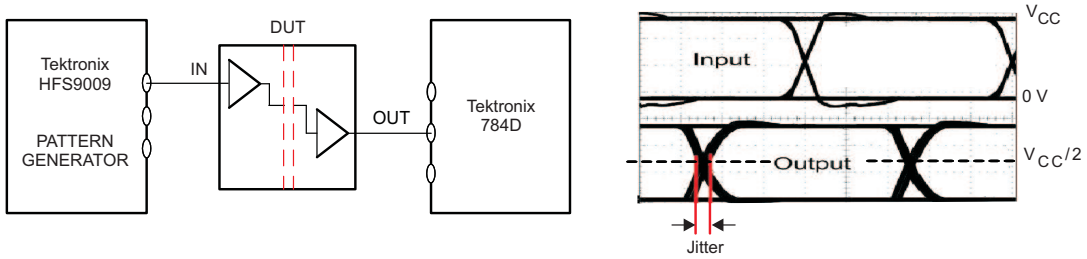
A. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

Figure 14. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

Figure 15. Common-Mode Transient Immunity Test Circuit



NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps.

Figure 16. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

10 Detailed Description

10.1 Overview

The isolator in Figure 17 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

10.2 Functional Block Diagram

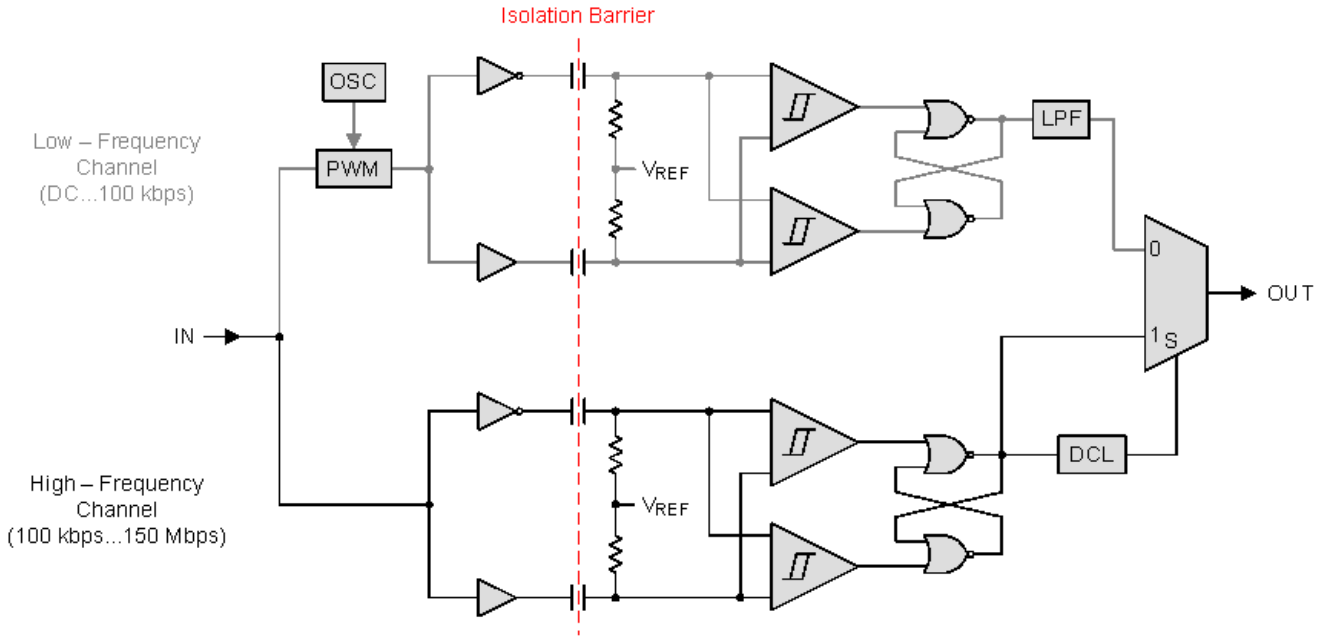


Figure 17. Conceptual Block Diagram of a Digital Capacitive Isolator

10.3 Feature Description

PRODUCT	MAX SIGNALING RATE	INPUT THRESHOLD	CHANNEL DIRECTION
ISO7220A	1 Mbps	~ 1.5 V (TTL) (CMOS compatible)	Same direction
ISO7220B	5 Mbps	~ 1.5 V (TTL) (CMOS compatible	
ISO7220C	25 Mbps	~ 1.5 V (TTL) (CMOS compatible)	
ISO7220M	150 Mbps	V_{CC}/ 2 (CMOS)	
ISO7221A	1 Mbps	~ 1.5 V (TTL) (CMOS compatible)	Opposite directions
ISO7221B	5 Mbps	~ 1.5 V (TTL) (CMOS compatible)	
ISO7221C	25 Mbps	~ 1.5 V (TTL) (CMOS compatible)	
ISO7221M	150 Mbps	V_{CC}/ 2 (CMOS)	

10.3.1 DIN EN 60747-5-5 Insulation Characteristics(1)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	V_{PK}
V_{PR}	Input to output test voltage	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	672	
		Method a, After environment tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial discharge < 5 pC	896	
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with t = 1 s, Partial discharge < 5 pC	1050	
V_{IOTM}	Transient overvoltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification) t = 1 s (100% production)	4000	
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the *Isolation Glossary*. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤150 V_{RMS}	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-III
	Rated mains voltage ≤400 V_{RMS}	I-II

10.3.2 IEC Package Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest pin-to-pin distance through air	SOIC-8	4.8			mm
L(I02)	Minimum external tracking (Creepage)	Shortest pin-to-pin distance across the package surface	SOIC-8	4.3			mm
CTI	Tracking resistance (Comparative Tracking Index)	IEC 60112 / VDE 0303 Part 1		400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation		0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-pin device, T_A = 25°C		10^{12}			Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ max		10^{11}			Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)			1		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			1		pF

10.3.3 IEC Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	SOIC-8	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			124	mA
			θ_{JA} = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			190	
T_S	Maximum case temperature	SOIC-8				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in *Absolute Maximum Ratings*. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in *Thermal Information* is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

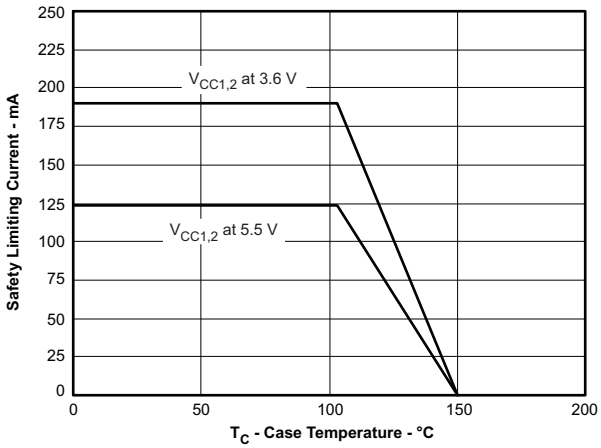


Figure 18. θ_{JC} Thermal Derating Curve per DIN EN 60747-5-5

10.3.4 Regulatory Information

VDE	CSA	UL
Certified according to DIN EN 60747-5-5 (VDE 0884-5) and DIN EN 61010-1 (VDE 0411-1)	Approved according to CSA Component Acceptance Notice 5A and IEC 60950-1	Recognized under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4000 V_{PK} Maximum Surge Voltage, 4000 V_{PK} Maximum Working Voltage, 560 V_{PK}	Evaluated to CSA 60950-1-07 and IEC 60950-1 (2nd Ed.) with 2000 V_{RMS} Isolation rating for products with working voltages ≤ 125 V_{RMS} for reinforced insulation and ≤ 390 V_{RMS} for basic insulation	Single Protection, 2500 V_{RMS} (1)
Certificate Number: 40016131	Master Contract Number: 220991	File Number: E181974

(1) Production tested ≥3000 V_{RMS} for 1 second in accordance with UL 1577.

10.4 Device Functional Modes

Table 2. ISO7220x or ISO7221x (1)

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up (V_{CC} ≥ 3.0 V), PD = Powered Down (V_{CC} ≤ 2.5 V), X = Irrelevant, H = High Level, L = Low Level

10.4.1 Device I/O Schematics

Internal schematics of input and output pins are shown in Figure 19.

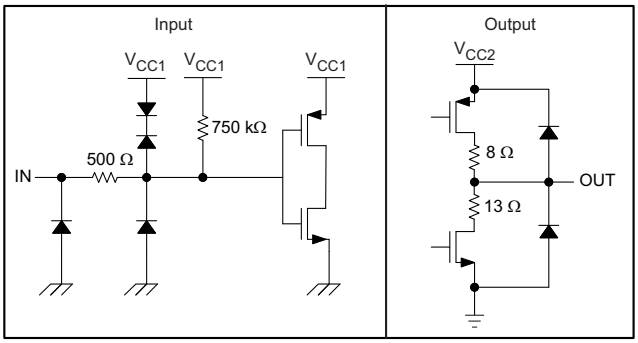


Figure 19. Device I/O Schematics

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

ISO722x use single-ended TTL or CMOS-logic switching technology. Its supply voltage range is from 3 V (2.8 V for C-grade) to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

11.2 Typical Application

ISO7221 can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-20 mA current loop.

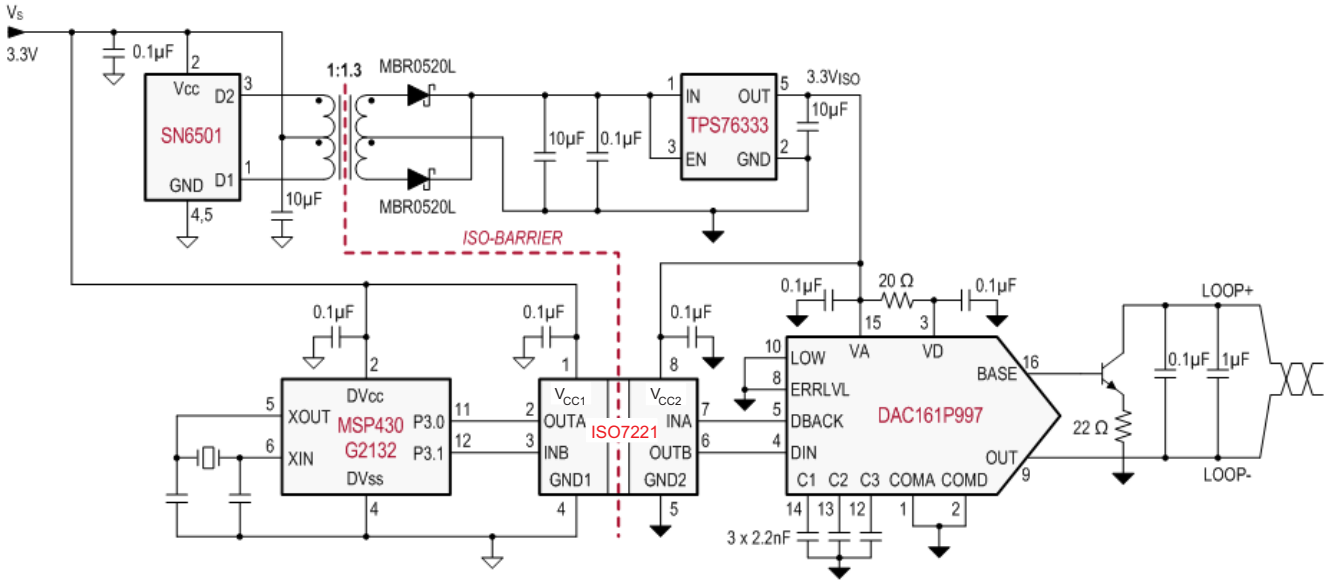


Figure 20. Isolated 4-20 mA Current Loop

11.2.1 Design Requirements

Unlike optocouplers, which need external components to improve performance, provide bias (or limit current), the ISO722x devices need only two external bypass capacitors to operate.

Typical Application (continued)

11.2.2 Detailed Design Procedure

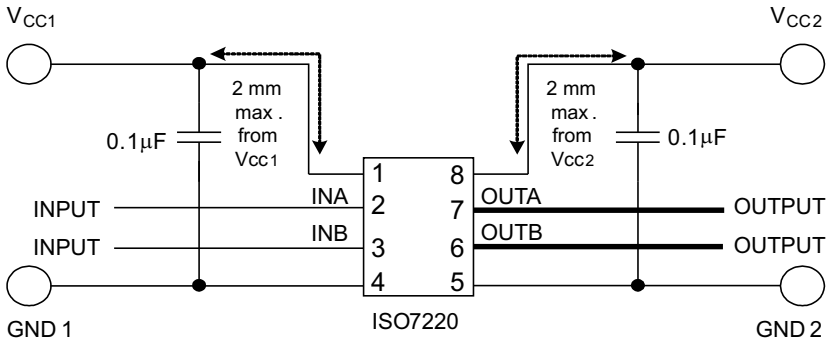


Figure 21. Typical ISO7220 Circuit Hook-Up

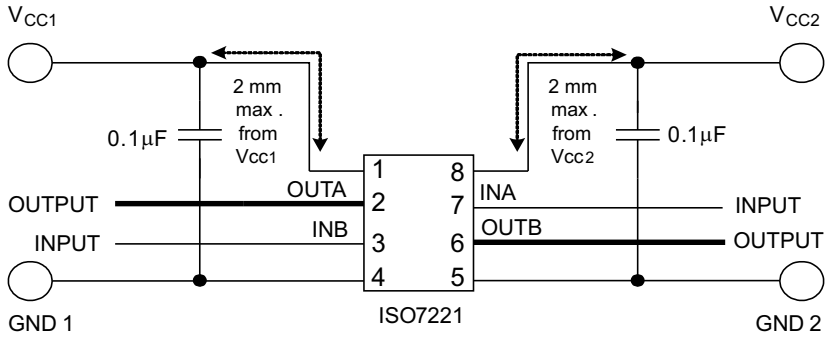


Figure 22. Typical ISO7221 Circuit Hook-Up

11.2.3 Application Curve

At maximum working voltage, ISO722x isolation barrier has more than 28 years of life.

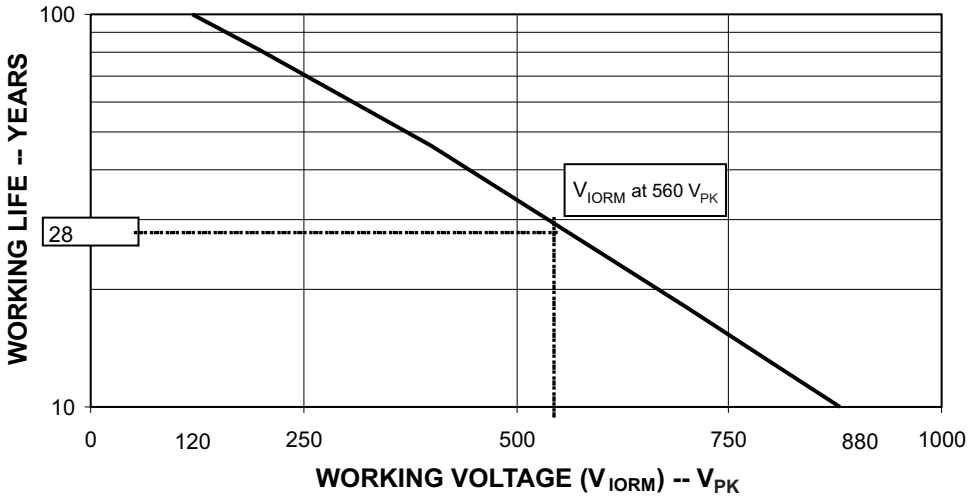


Figure 23. Time Dependent Dielectric Breakdown Test Results

12 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 data sheet. For such applications, detailed power supply design and transformer selection recommendations are available in the data sheet, *SN6501 Transformer Driver for Isolated Power Supplies* (SLLSEA0).

13 Layout

13.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 24). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. For detailed layout recommendations, see Application Note *Digital Isolator Design Guide* (SLLA284).

13.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

13.2 Layout Example

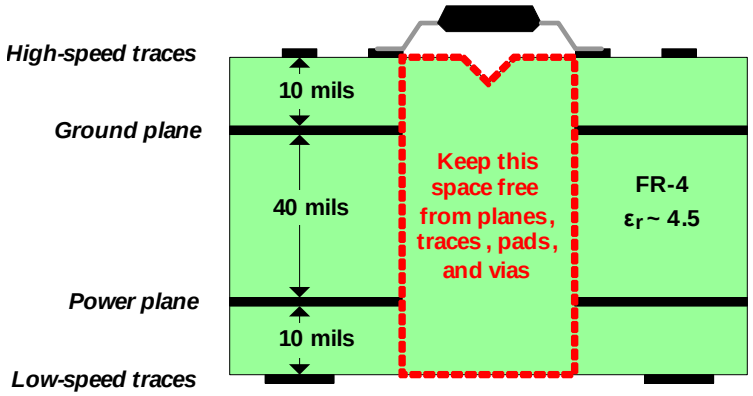


Figure 24. Recommended Layer Stack

14 Device and Documentation Support

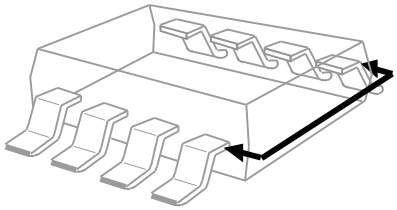
14.1 Device Support

14.1.1 Isolation Glossary

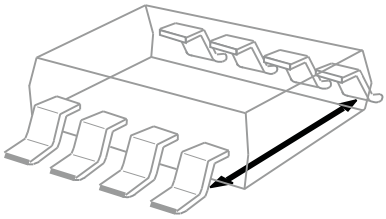
Primary Circuit — A circuit that is directly connected to an external mains supply for its power needs.

Secondary Circuit — A circuit that has no direct connection to a primary circuit and derives its power from a transformer, converter or equivalent isolation device, or from a battery.

Creepage — The shortest distance between two conductive parts measured along the surface of a solid insulation. The shortest path is typically found around the end of the package body.



Clearance — The shortest distance between two conductive parts measured through air.



Isolation Capacitance (C_{IO}) — The total capacitance between the terminals on a first side of the isolation barrier connected together and the terminals on a second side of the isolation barrier connected together forming a two-terminal device.

Isolation Resistance (R_{IO}) — The resistance between the terminals on a first side of the isolation barrier connected together and all the terminals on a second side of the isolation barrier connected together forming a two-terminal device.

Rated Isolation Voltages — The maximum voltage between all input terminals (connected together) and all output terminals (connected together) respectively.

Maximum Rated Isolation Working Voltage (V_{IOWM}) — An r.m.s or equivalent d.c. voltage assigned by the manufacturer, characterizing the specified long term withstand capability of its isolation.

Maximum Rated Repetitive Peak Isolation Voltage (V_{IORM}) — A peak voltage assigned by the manufacturer, characterizing the specified withstand capability of its isolation against repetitive peak voltages. It includes all repetitive transient voltages, but excludes all non-repetitive transient voltages.

Maximum Rated Transient Isolation Voltage (V_{IOTM}) — A peak impulse voltage assigned by the manufacturer, characterizing the specified withstand capability of its isolation against transient overvoltages.

Withstand Isolation Voltage (V_{ISO}) — Maximum AC r.m.s. isolation voltage for one minute.

Surge Isolation Voltage (V_{IOSM}) — The highest instantaneous value of an isolation voltage pulse with short time duration and of specified wave shape.

Partial Discharge — Localized electrical discharge which occurs in the insulation between all terminals of the first side and all terminals of the second side of the coupler.

Device Support (continued)

Comparative Tracking Index (CTI) — CTI is an index used for electrical insulating materials that is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher the CTI value of the insulating material, the smaller the minimum creepage distance required.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Material Groups — Materials are classified into four groups according to their CTI values. These values are determined in accordance with IEC 60112. The groups are as follows:

- Material group I: 600V ≤ CTI
- Material group II: 400V ≤ CTI < 600
- Material group II: 175V ≤ CTI < 400
- Material group II: 100V ≤ CTI < 175

14.1.1.1 Insulation:

Functional insulation — Insulation needed for the correct operation of the equipment.

Basic insulation — Insulation that provides basic protection against electric shock.

Supplementary insulation — Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation — Insulation comprising both basic and supplementary insulation.

Reinforced insulation — A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

14.1.1.2 Pollution Degree:

Pollution is any addition of foreign matter, solid, liquid, or gaseous that can result in a reduction of electric strength or surface resistivity of the insulation. There are four categories of pollution:

Pollution Degree 1 — No pollution or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 — Only nonconductive pollution occurs. However, a temporary conductivity caused by condensation is to be expected.

Pollution Degree 3 — Conductive pollution occurs or dry non-conductive pollution occurs which becomes conductive due to condensation which is to be expected.

Pollution Degree 4 – Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

14.1.1.3 Overvoltage Categories and Installation Classification:

Overvoltage Categories define transient overvoltage conditions. There are four different levels as indicated in IEC 60664.

I: Signal level — Special protected equipment or parts of equipment, for example, circuit board inside a DVD player.

II: Local level — Portable equipment that is supplied from the wall outlet, that is, a DVD player

III: Distribution level — Equipment in fixed installation such as HVAC system, Washers / Dryers, and so forth.

IV: Primary supply level — Equipment for use at the origin of the installations such as overhead lines, cable systems, and so forth.

Lower level category is subject to smaller transients than the category above.

14.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7220A	Click here	Click here	Click here	Click here	Click here
ISO7220B	Click here	Click here	Click here	Click here	Click here
ISO7220C	Click here	Click here	Click here	Click here	Click here
ISO7220M	Click here	Click here	Click here	Click here	Click here
ISO7221A	Click here	Click here	Click here	Click here	Click here
ISO7221B	Click here	Click here	Click here	Click here	Click here
ISO7221C	Click here	Click here	Click here	Click here	Click here
ISO7221M	Click here	Click here	Click here	Click here	Click here

14.3 Trademarks

DeviceNet is a trademark of Open DeviceNet Vendors Association.
Profibus is a trademark of Profibus.
All other trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7220AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A	Samples
ISO7220ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A	Samples
ISO7220ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A	Samples
ISO7220ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A	Samples
ISO7220BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B	Samples
ISO7220BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B	Samples
ISO7220BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B	Samples
ISO7220BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B	Samples
ISO7220CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220C	Samples
ISO7220CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220C	Samples
ISO7220CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220C	Samples
ISO7220CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220C	Samples
ISO7220MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M	Samples
ISO7220MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M	Samples
ISO7220MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M	Samples
ISO7220MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M	Samples
ISO7221AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7221ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A	Samples
ISO7221ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A	Samples
ISO7221ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A	Samples
ISO7221BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B	Samples
ISO7221BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B	Samples
ISO7221BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B	Samples
ISO7221BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B	Samples
ISO7221CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C	Samples
ISO7221CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C	Samples
ISO7221CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C	Samples
ISO7221CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C	Samples
ISO7221MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M	Samples
ISO7221MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M	Samples
ISO7221MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M	Samples
ISO7221MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7220A, ISO7221A, ISO7221C :

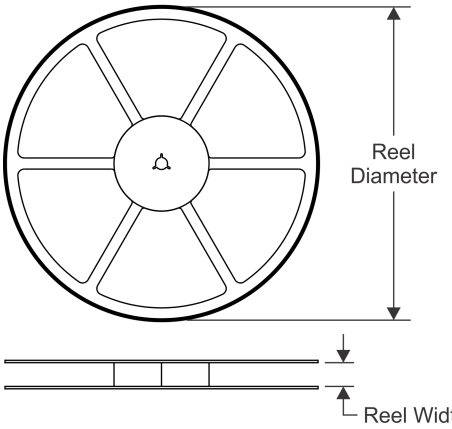
- Automotive: ISO7220A-Q1, ISO7221A-Q1, ISO7221C-Q1

NOTE: Qualified Version Definitions:

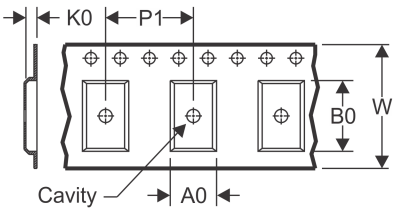
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

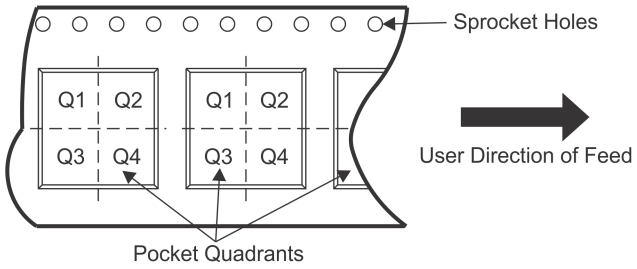


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

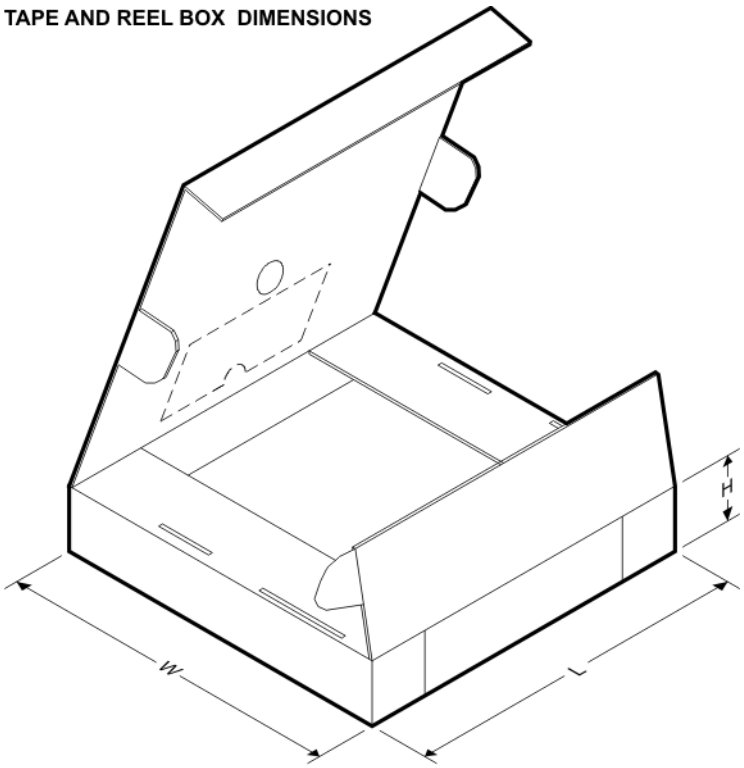
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7220ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

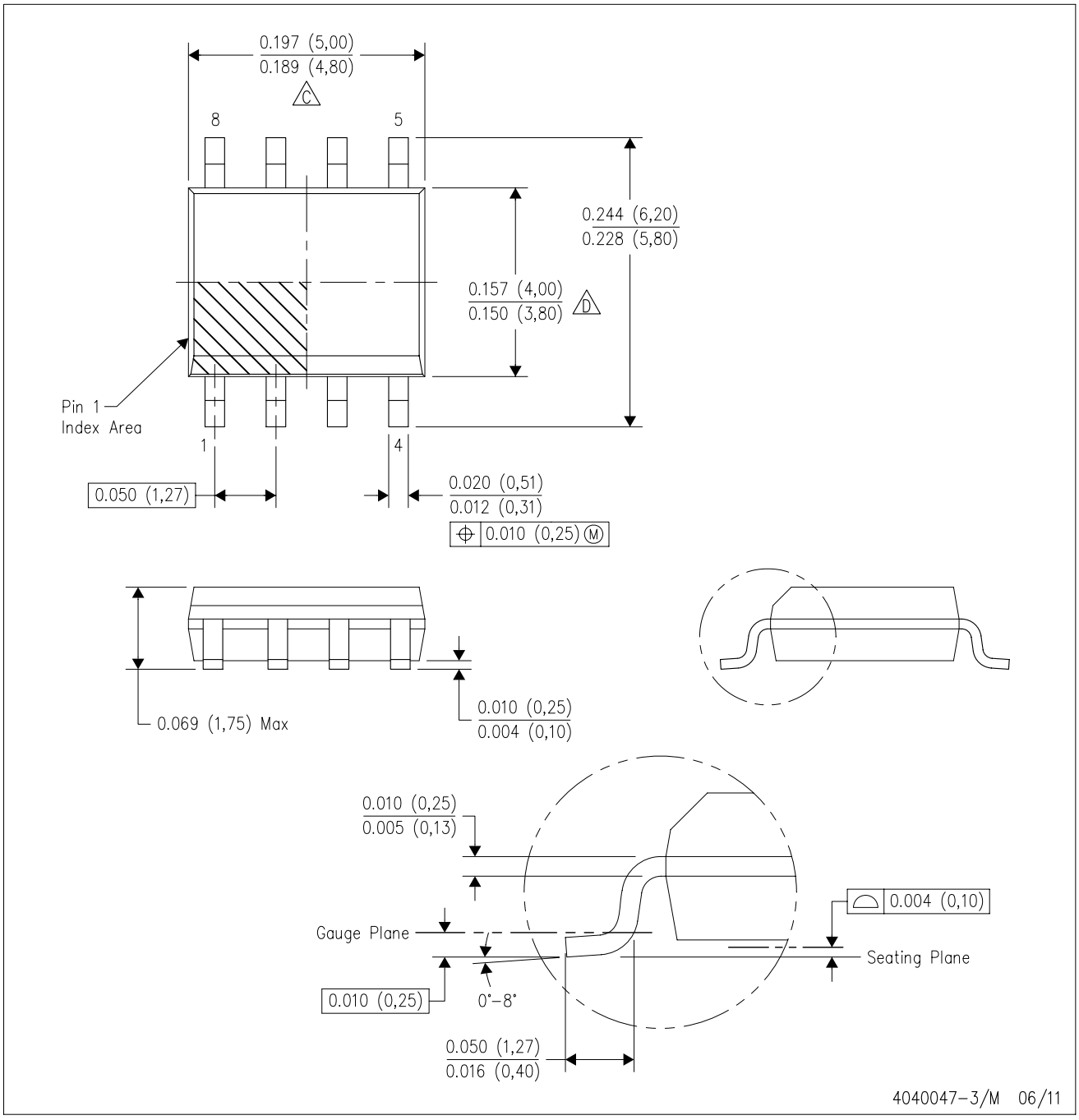
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

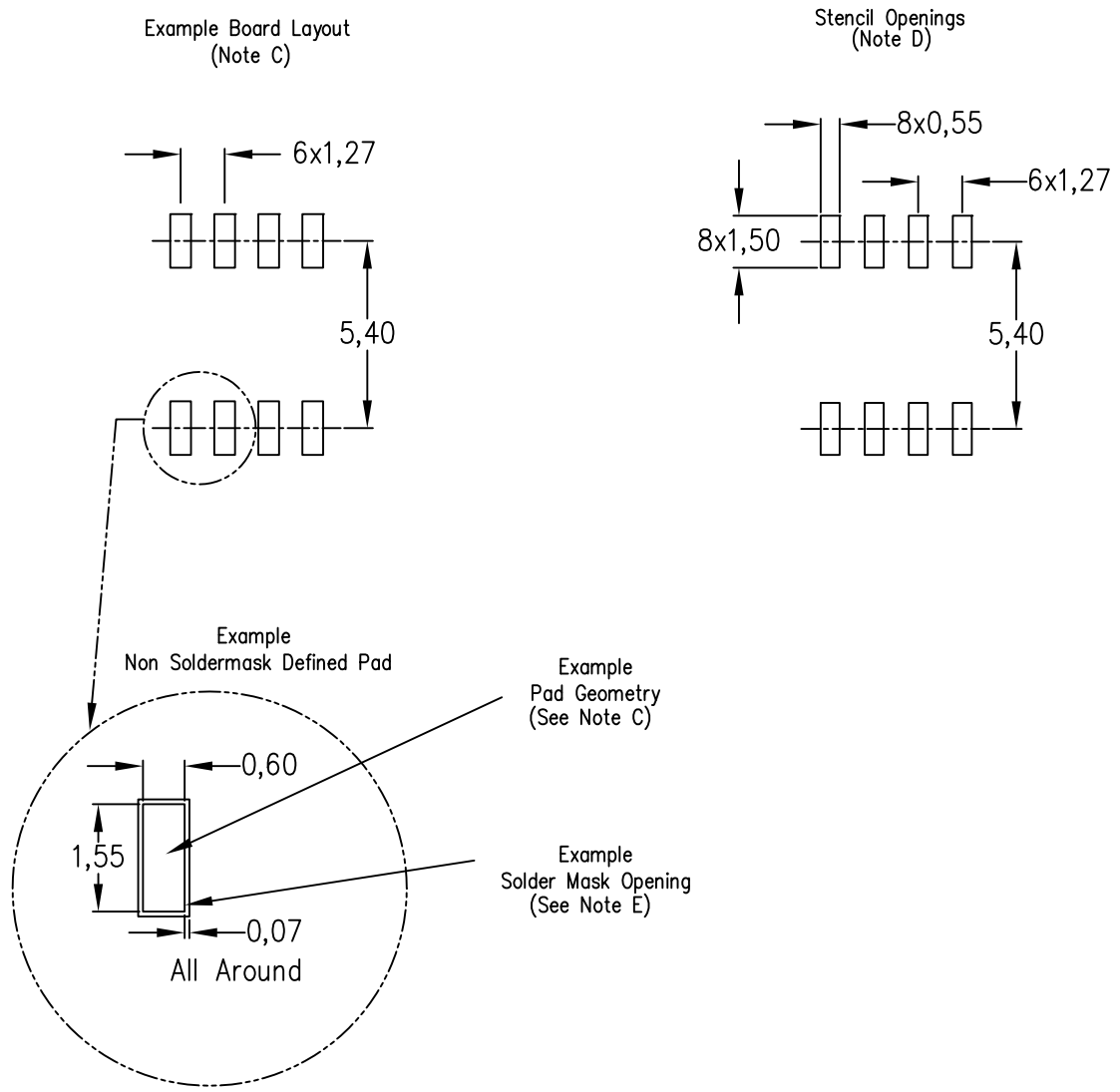
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7220ADR	SOIC	D	8	2500	367.0	367.0	35.0
ISO7220BDR	SOIC	D	8	2500	367.0	367.0	35.0
ISO7220CDR	SOIC	D	8	2500	367.0	367.0	35.0
ISO7220MDR	SOIC	D	8	2500	367.0	367.0	35.0
ISO7221ADR	SOIC	D	8	2500	367.0	367.0	35.0
ISO7221BDR	SOIC	D	8	2500	367.0	367.0	35.0
ISO7221CDR	SOIC	D	8	2500	367.0	367.0	35.0
ISO7221MDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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