

Data sheet acquired from Harris Semiconductor SCHS061C – Revised September 2003

CMOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

High-Voltage Types (20-Volt Rating)

CD4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/EXP input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/EXP is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig.10 and its associated explanation for applications where a capability greater than 4-wide is required.

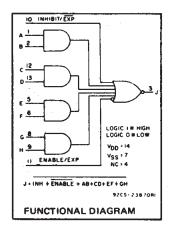
The CD4086B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

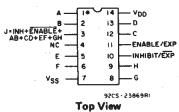
- Medium-speed operation tpHL = 90 ns; tpLH = 140 ns (typ.) at 10 V
- INHIBIT and ENABLE inputs
- Buffered outputs
- 100% tested for quiescent current at 20 V
- Maximum input leakage current of 18 V over full package-temperature range;
 100 nA at 18 V and 25°C
- Noise margin (over full package termperature range):

1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V

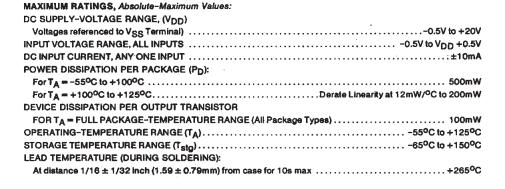
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4086B Types



TERMINAL ASSIGNMENT



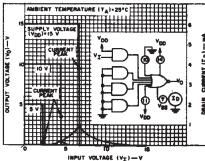


Fig. 1 — Typical voltage and current transfer characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

	LIM	LIMITS				
CHARACTERISTIC	MIN.	MAX.	UNITS			
Supply-Voltage Range (For T _A = Full Package- Temperature Range)	3	18	٧			

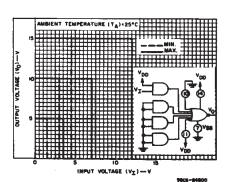


Fig. 2 — Minimum and maximum voltage transfer characteristics,

STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC		DITIO	NS	LIMI'	TS AT I	NDICAT	ED TE	TEMPERATURES (°C)				
LEMISTIC	v _o	VIN	V _{DD}						+25		1	
	(V).	(V)	(V)	55	-40	+85	+125	Min.	Тур.	Max.		
Quiescent		0,5	5	1	1	30	30		0.02	1	ı e	
Device		0,10	10	2	2	60	60		0.02	2	μА	
Current	_	0,15	15	4	4	120	120	_	0.02	4	μA	
IDD Max.	_	0,20	20	20	20	600	600	<u> </u>	0.04	20		
Output Low								1 9	: .		1	
(Sink)	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	387 a 1	54		
Current,	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6			
IOL Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	_		
Output High	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	_	mA	
(Source)	2.5	0,5	5	-2	-1.8	-1.3	-1,15	-1.6	-3.2			
Current,	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	_		
IOH Min.	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	_		
Output Volt-												
age:	_	0,5	5		0.0)5		_	0	0.05		
Low-Level,		0,10	10		0.0)5		-	0	0.05		
V _{OL} Max.	, 7 J	0,15	15		0.0)5	٠.	-	Q	0.05	v	
Output Volt-		F . 4. 1									V	
age:	_	0,5	5		4.9	95		4.95	5	_		
High-Level,	_	0,10	10		9.9	95		9.95	10	_		
V _{OH} Min.		0,15	15		14.	95		14.95	15	_		
Input Low	0.5,4.5		5		1.	5		_		1.5		
Voltage,	1,9	-	10		3	- L		_	_	3		
VIL Max.	1.5,13.5	-,	15		4				_	4		
Input High	0.5,4.5	_	5	3.5				3.5	_	_	٧	
Voltage,	1,9	-	10		7			7	_			
V _{IH} Min.	1.5,13.5	-	15		1	1		11	_			
Input Current, IN Max.		0,18	18	±0.1	±0.1	±1	±1	_	±10-5	±0.1	μА	

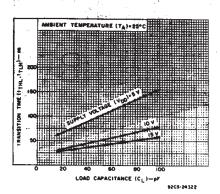


Fig.6 - Typical transition time vs. load capacitance.

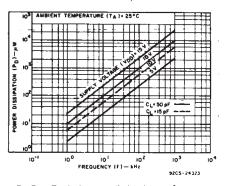


Fig.7 — Typical power dissipation vs. frequency,

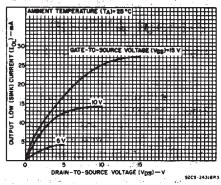


Fig. 3 — Typical output low (sink) current characteristics.

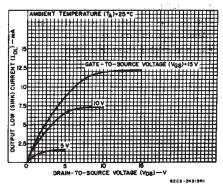


Fig. 4 — Minimum output low (sink) current characteristics.

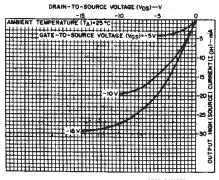


Fig.5 — Typical output high (source) current characteristics.

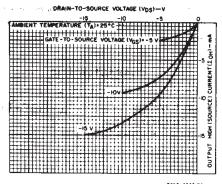
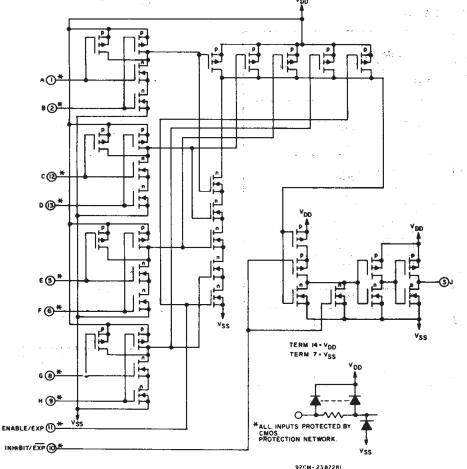


Fig.8 – Minimum output high (source) current characteristics.



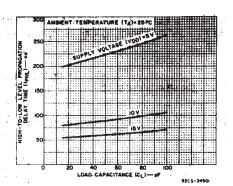


Fig. 11 — Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

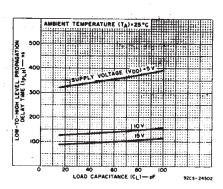
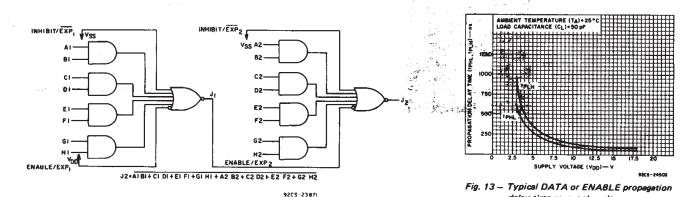


Fig. 12 — Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

delay time vs. supply voltage.

Fig. 9 - CD4086B schematic diagram.



CD4086B Types

Fig. 10 - Two CD40868's connected as an 8-wide 2-input A-O-I gate.

Fig. 10 above shows two CD4086's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086 is fed directly to the ENABLE/EXP2 line of the second CD4086. In a similar fashion, any

NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the IN-HIBIT/EXP input with the same result.

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CD4086B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r , t_f = 20 ns, C_L = 50 pF, R_L = 200 $k\Omega$

:	CONDI	TIONS	LIF	LIMITE	
CHARACTERISTIC		V _{DD} (V)	TYP.	MAX.	UNITS
Propagation Delay Time		5	225	450	
(Data):		10	90	180	ns
High-to-Low Level, tpHL		15	60	120	1
Low-to-High Level, tpLH		5	310	620	
		10	125	250	ns
	<u>L</u>	15	90	180	1
Propagation Delay Time		5	150	300	
(Inhibit): High-to-Low		10	60	120	ns
Level, tPHL(INH)		15	40	80	1
Laure de Illah I arah		5	250	500	
Low-to-High Level,		10	100	200	ns
^t PLH(INH)		15	70	140]
Transision Time		5	100	200	
Transition Time, tTHL, tTLH		10	50	100	ns
		15	40	80	1
Input Capacitance CIN	Any	Input	5	7.5	pF

TEST CIRCUITS

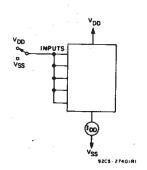


Fig. 14 - Quiescent device current.

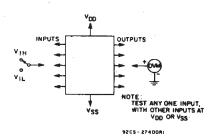
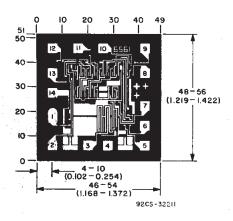


Fig. 15 - Input voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch) .

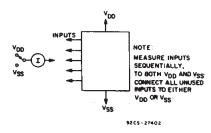


Fig. 16 - Input leakage current.

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PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4086BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4086BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4086BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
CD4086BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4086BPWE4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI
CD4086BPWG4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI
CD4086BPWRE4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI
CD4086BPWRG4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame



PACKAGE OPTION ADDENDUM

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retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4086BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4086BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4086BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4086BNSR	SO	NS	14	2000	346.0	346.0	33.0

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



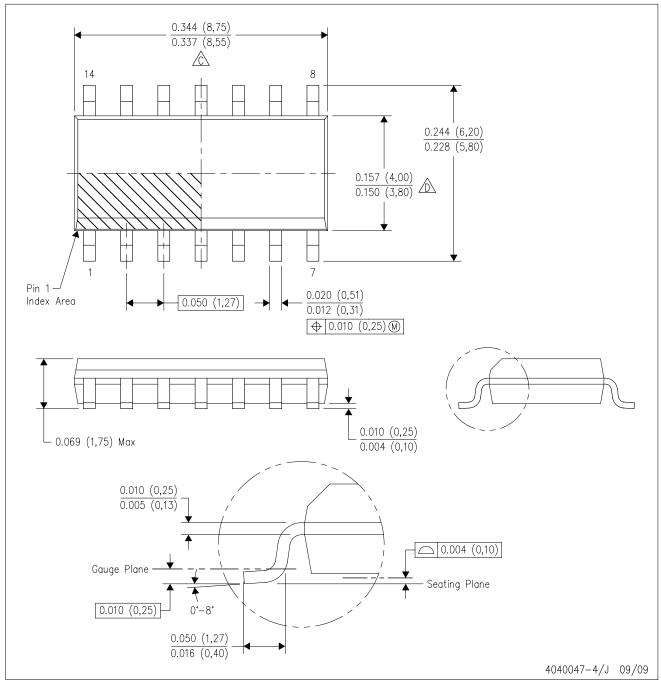
14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

