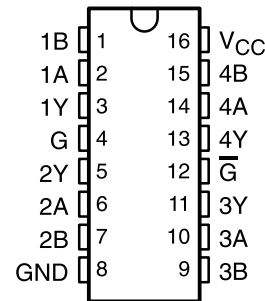


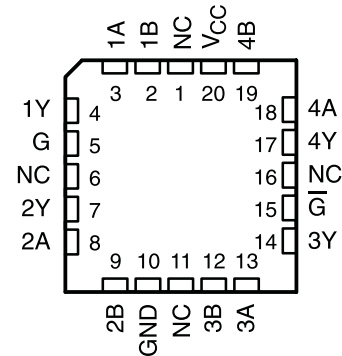
## FEATURES

- **AM26LS32A Devices Meet or Exceed the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendations V.10 and V.11**
- **AM26LS32A Devices Have  $\pm 7$ -V Common-Mode Range With  $\pm 200$ -mV Sensitivity**
- **AM26LS33A Devices Have  $\pm 15$ -V Common-Mode Range With  $\pm 500$ -mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operate From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output-Enable Inputs**
- **Input Impedance . . . 12 k $\Omega$  Minimum**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32™ and AM26LS33™**

AM26LS32AC . . . D, N, NS, OR PW PACKAGE  
AM26LS32AI, AM26LS33AC . . . D, OR N PACKAGE  
AM26LS32AM, AM26LS33AM . . . J PACKAGE  
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## DESCRIPTION

The AM26LS32A and AM26LS33A devices are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that, if the inputs are open, the outputs always are high.

Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this does not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AI is characterized for operation from –40°C to 85°C. The AM26LS32AM and AM26LS33AM are characterized for operation over the full military temperature range of –55°C to 125°C.



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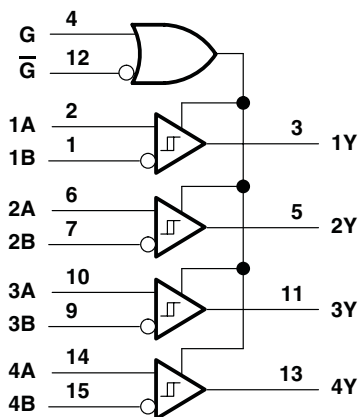
**AM26LS32AC, AM26LS32AI, AM26LS33AC  
AM26LS32AM, AM26LS33AM  
QUADRUPLE DIFFERENTIAL LINE RECEIVERS**

SLLS115E—OCTOBER 1980—REVISED OCTOBER 2007

**FUNCTION TABLE  
Each Receiver**

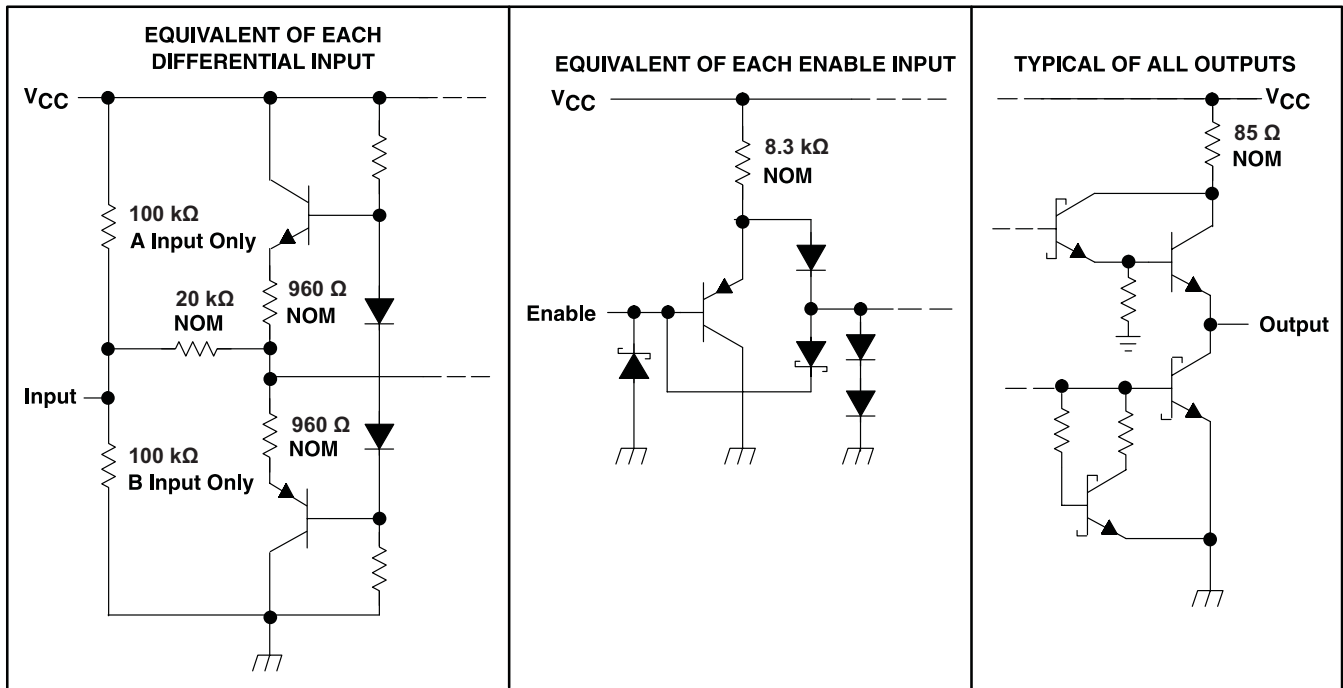
DIFFERENTIAL A-B	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers are for D, N, NS, or PW packages only.

SCHEMATICS OF INPUTS AND OUTPUTS



ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage <sup>(2)</sup>		7	V
$V_I$	Input voltage	Any differential input	$\pm 25$	V
		Other inputs	7	
$V_{ID}$	Differential input voltage <sup>(3)</sup>		$\pm 25$	V
	Continuous total power dissipation	See Dissipation Ratings Table		
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	D package	73	°C/W
		N package	67	
		NS package	64	
		PW package	108	
$T_C$	Case temperature for 60 seconds	FK package	260	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D or N package	260	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J package	300	°C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground terminal.
- (3) Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**AM26LS32AC, AM26LS32AI, AM26LS33AC  
AM26LS32AM, AM26LS33AM  
QUADRUPLE DIFFERENTIAL LINE RECEIVERS**

SLLS115E—OCTOBER 1980—REVISED OCTOBER 2007

**DISSIPATION RATINGS**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATION FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	AM26LS32AC, AM26LS32AI, AM26LS33AC			V
		4.75	5	5.25	
		AM26LS32AM, AM26LS33AM			
		4.5	5	5.5	
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>IC</sub>	Common-mode input voltage	AM26LS32A			V
				±7	
		AM26LS33A			
				±15	
I <sub>OH</sub>	High-level output current			-440	μA
I <sub>OL</sub>	Low-level output current			8	mA
T <sub>A</sub>	Operating free-air temperature	AM26LS32AC, AM26LS33AC			°C
		0		70	
		AM26LS32AI			
		-40		85	
		AM26LS32AM, AM26LS33AM			
		-55		125	

**ELECTRICAL CHARACTERISTICS**

over recommended ranges of V<sub>CC</sub>, V<sub>IC</sub>, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>O</sub> = V <sub>OHmin</sub> , I <sub>OH</sub> = -440 μA	AM26LS32A			0.2	V
			AM26LS33A			0.5	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>O</sub> = 0.45 V, I <sub>OL</sub> = 8 mA	AM26LS32A			-0.2 <sup>(2)</sup>	V
			AM26LS33A			-0.5 <sup>(2)</sup>	
V <sub>hys</sub>	Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )				50		mV
V <sub>IK</sub>	Enable-input clamp voltage	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>ID</sub> = 1 V, V <sub>I(G)</sub> = 0.8 V, I <sub>OH</sub> = -440 μA	AM26LS32AC, AM26LS33AC			2.7	V
			AM26LS32AM, AM26LS32AI, AM26LS33AM			2.5	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>ID</sub> = -1 V, V <sub>I(G)</sub> = 0.8 V	I <sub>OL</sub> = 4 mA			0.4	V
			I <sub>OL</sub> = 8 mA			0.45	
I <sub>OZ</sub>	Off-state (high-impedance state) output current	V <sub>CC</sub> = MAX	V <sub>O</sub> = 2.4 V			20	μA
			V <sub>O</sub> = 0.4 V			-20	
I <sub>I</sub>	Line input current	V <sub>I</sub> = 15 V,	Other input at -10 V to 15 V			1.2	mA
		V <sub>I</sub> = -15 V,	Other input at -15 V to 10 V			-1.7	
I <sub>I(EN)</sub>	Enable input current	V <sub>I</sub> = 5.5 V				100	μA
I <sub>H</sub>	High-level enable current	V <sub>I</sub> = 2.7 V				20	μA

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, and V<sub>IC</sub> = 0.

(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

**ELECTRICAL CHARACTERISTICS (continued)**

 over recommended ranges of  $V_{CC}$ ,  $V_{IC}$ , and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$I_L$	Low-level enable current	$V_I = 0.4\text{ V}$			–0.36	mA
$r_i$	Input resistance	$V_{IC} = -15\text{ V to }15\text{ V}$ , One input to ac ground	12	15		k $\Omega$
$I_{OS}$	Short-circuit output current <sup>(3)</sup>	$V_{CC} = \text{MAX}$	–15		–85	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ , All outputs disabled		52	70	mA

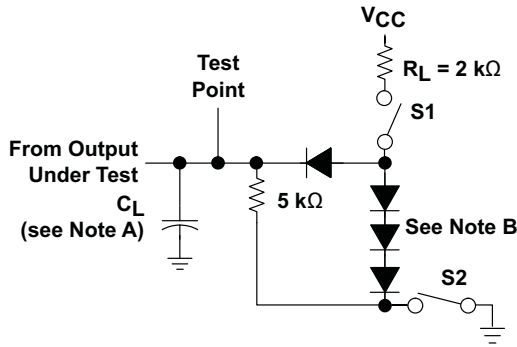
(3) Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

**SWITCHING CHARACTERISTICS**
 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

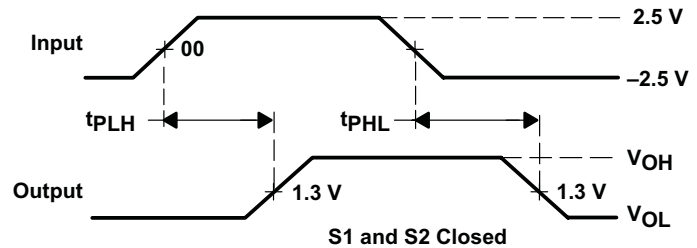
PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}$ , See <a href="#">Figure 1</a>		20	35	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output			22	35	
$t_{PZH}$	Output enable time to high level	$C_L = 15\text{ pF}$ , See <a href="#">Figure 1</a>		17	22	ns
$t_{PZL}$	Output enable time to low level			20	25	
$t_{PHZ}$	Output disable time from high level	$C_L = 15\text{ pF}$ , See <a href="#">Figure 1</a>		21	30	ns
$t_{PLZ}$	Output disable time from low level			30	40	

 (1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and  $V_{IC} = 0$ .

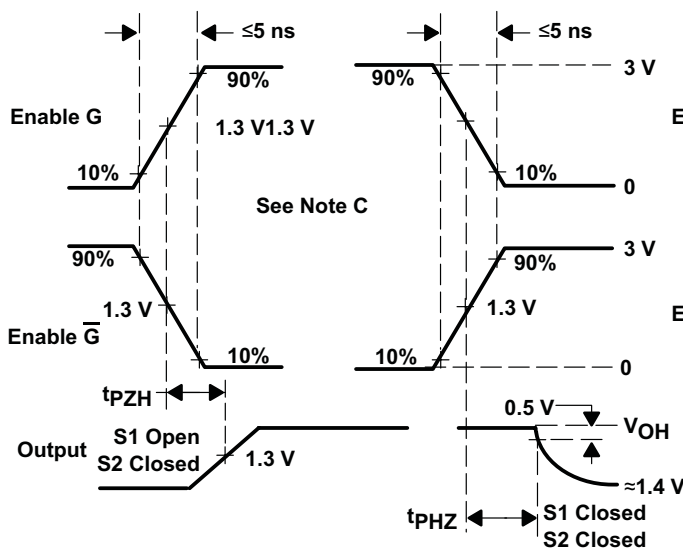
PARAMETER MEASUREMENT INFORMATION



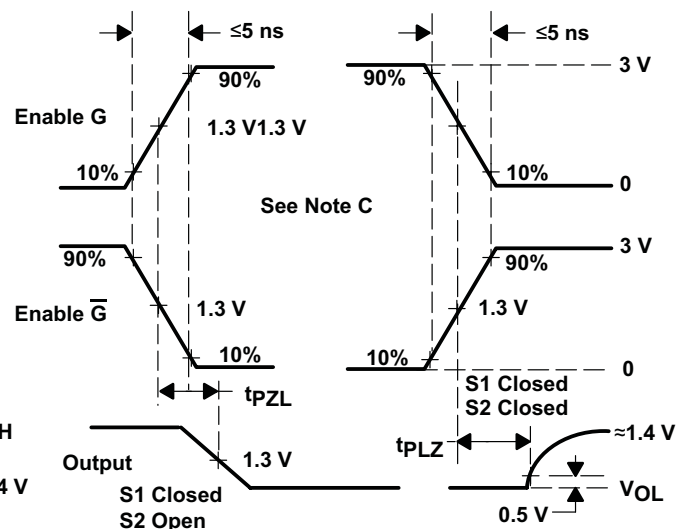
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR  $t_{PLH}$ ,  $t_{PHL}$



VOLTAGE WAVEFORMS FOR  $t_{PHZ}$ ,  $t_{PZH}$

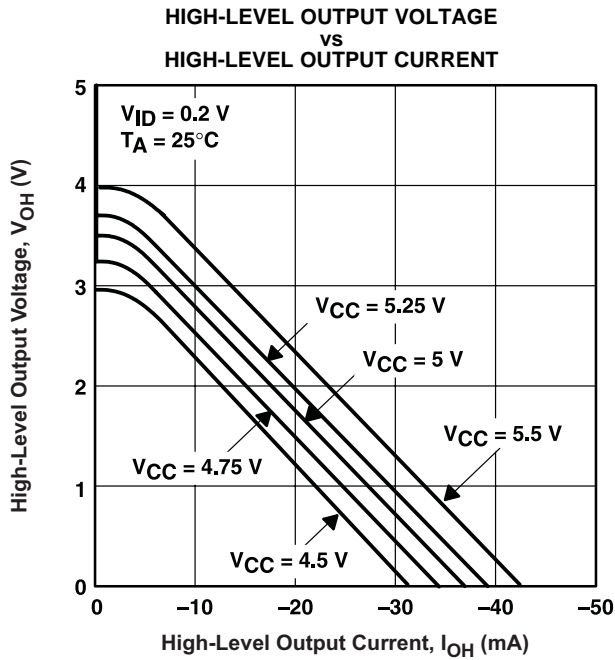


VOLTAGE WAVEFORMS FOR  $t_{PLZ}$ ,  $t_{PZL}$

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Enable G is tested with  $\bar{G}$  high;  $\bar{G}$  is tested with G low.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



†  $V_{CC} = 5.5\text{ V}$  and  $V_{CC} = 4.5\text{ V}$  applies to M-suffix devices only.

Figure 2.

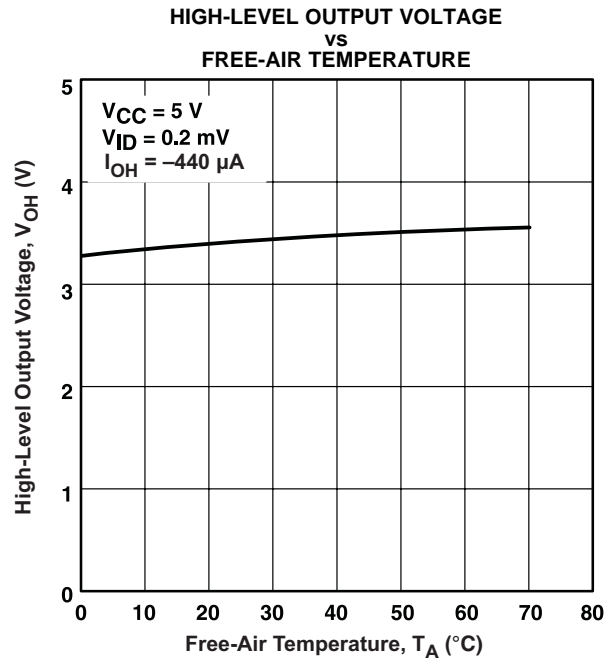


Figure 3.

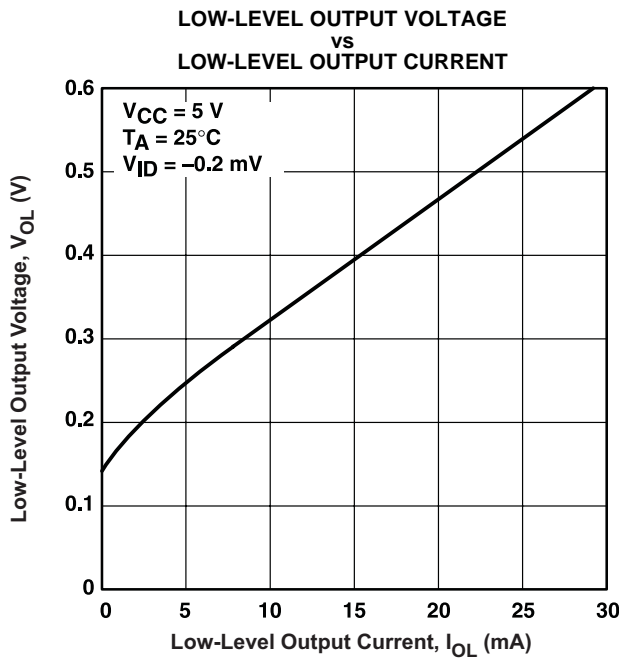


Figure 4.

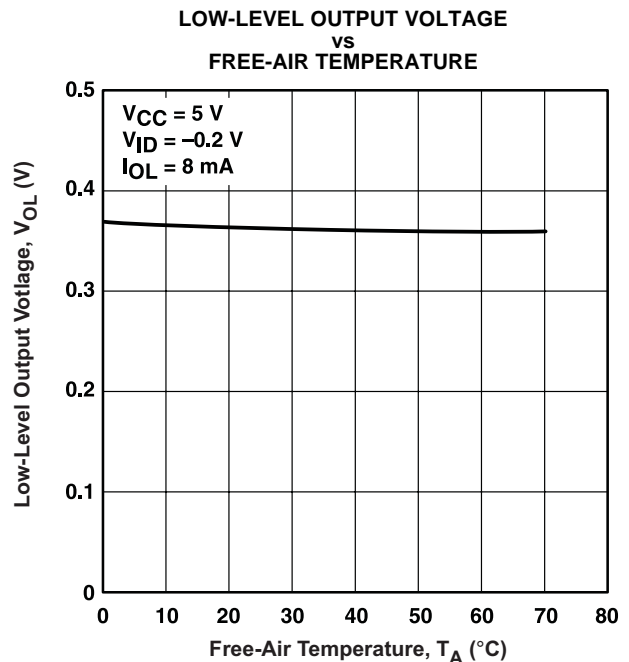


Figure 5.

TYPICAL CHARACTERISTICS (continued)

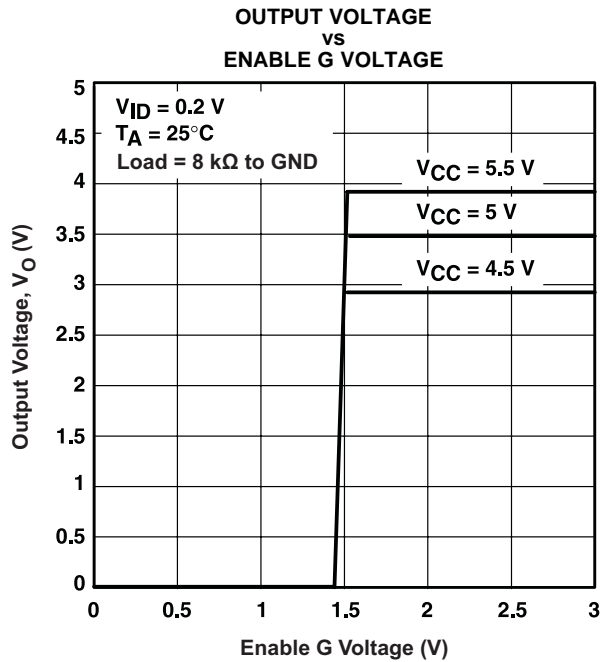


Figure 6.

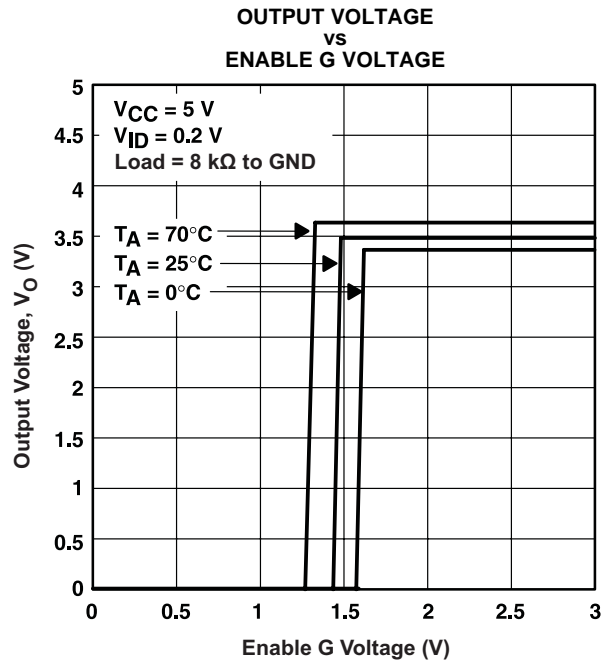


Figure 7.

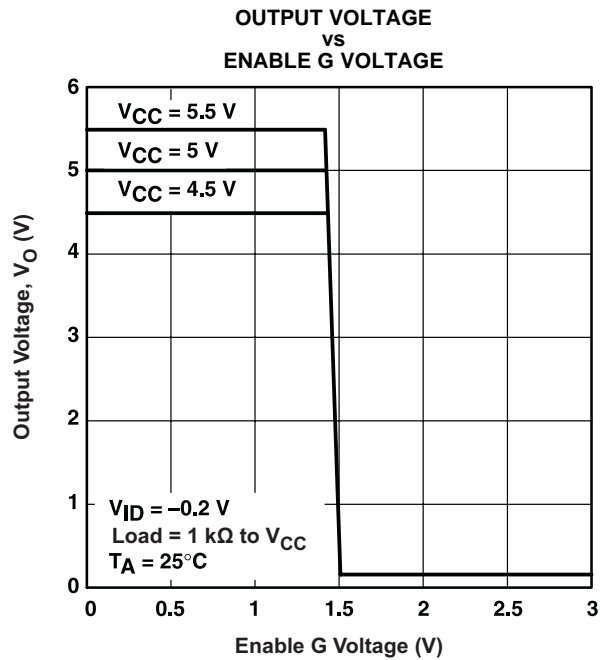


Figure 8.

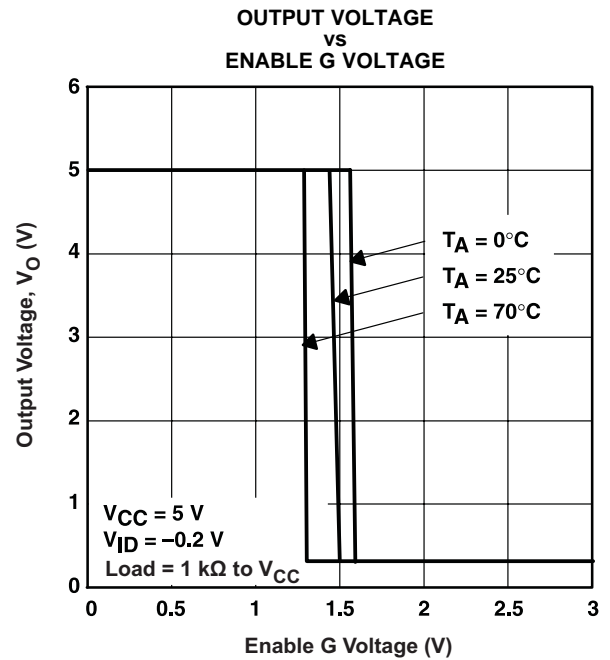


Figure 9.



**TYPICAL CHARACTERISTICS (continued)**

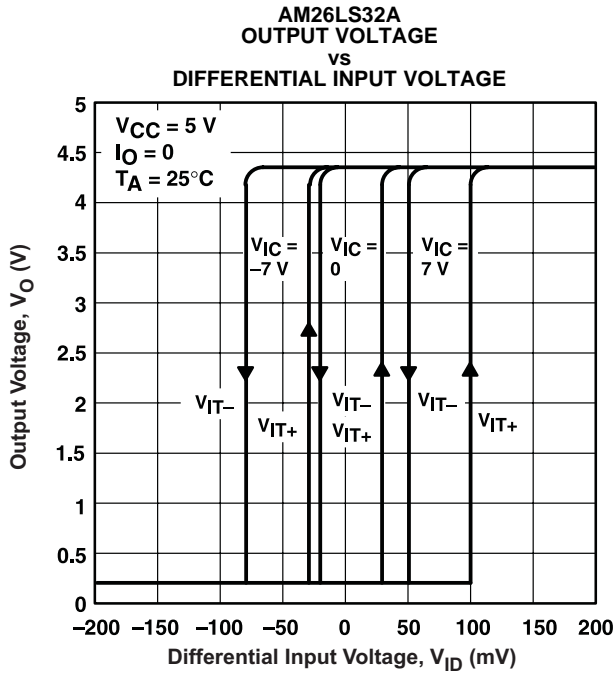


Figure 10.

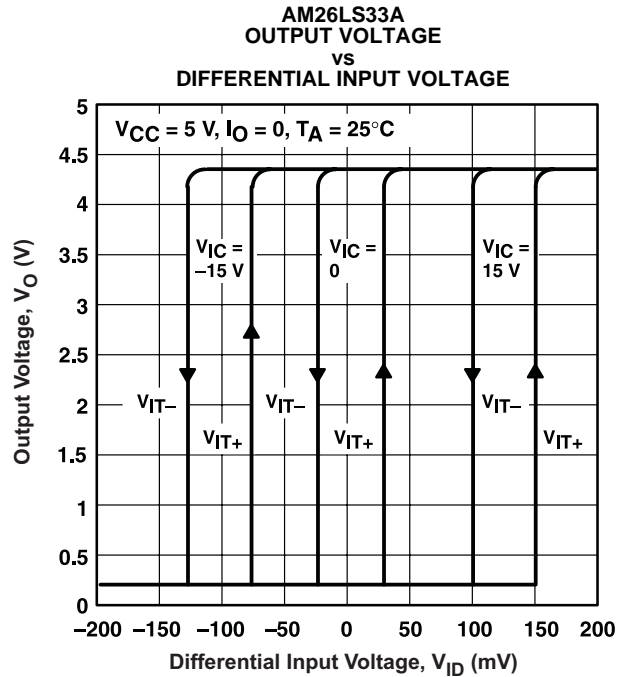
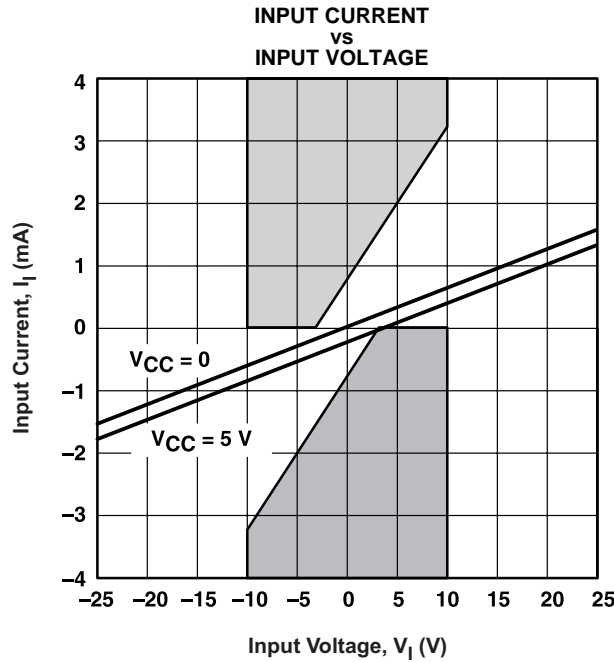


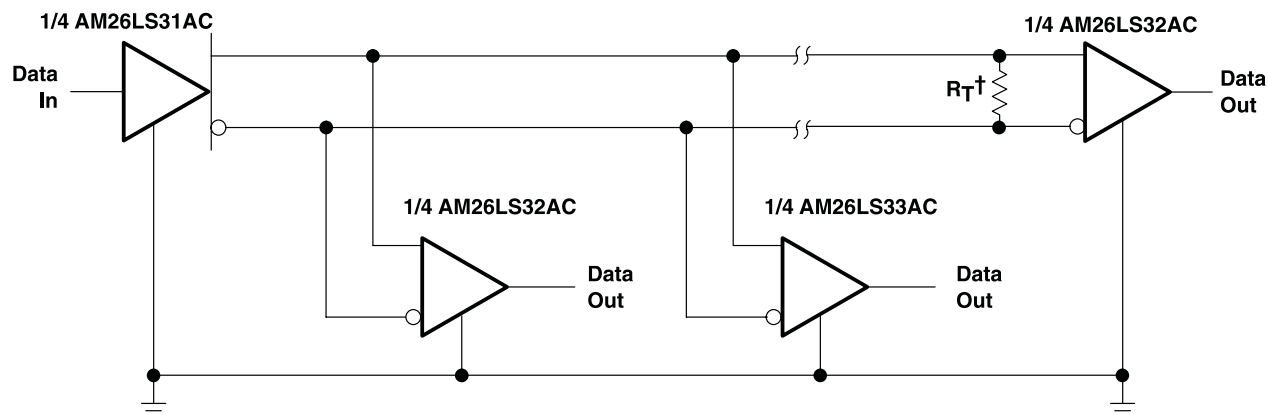
Figure 11.



The unshaded area shows requirements of paragraph 4.2.1 of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B.

Figure 12.

APPLICATION INFORMATION



†  $R_T$  equals the characteristic impedance of the line.

Figure 13. Circuit with Multiple Receivers

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-7802003M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-7802003MEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
5962-7802003MFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-7802004M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-7802004MEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
5962-7802004MFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
AM26LS32ACD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS32ACNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS32ACNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACPWG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
AM26LS32AIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS32AINE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS32AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
AM26LS32AMJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
AM26LS32AMJB	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
AM26LS32AMWB	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
AM26LS33ACD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS33ACNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS33AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
AM26LS33AMJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
AM26LS33AMJB	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
AM26LS33AMWB	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF AM26LS32A, AM26LS32AM, AM26LS33A, AM26LS33AM :**

- Enhanced Product: [AM26LS32AM-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LS32ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS32ACNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LS32ACPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LS32AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS33ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LS32ACDR	SOIC	D	16	2500	346.0	346.0	33.0
AM26LS32ACNSR	SO	NS	16	2000	346.0	346.0	33.0
AM26LS32ACPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
AM26LS32AIDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26LS33ACDR	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

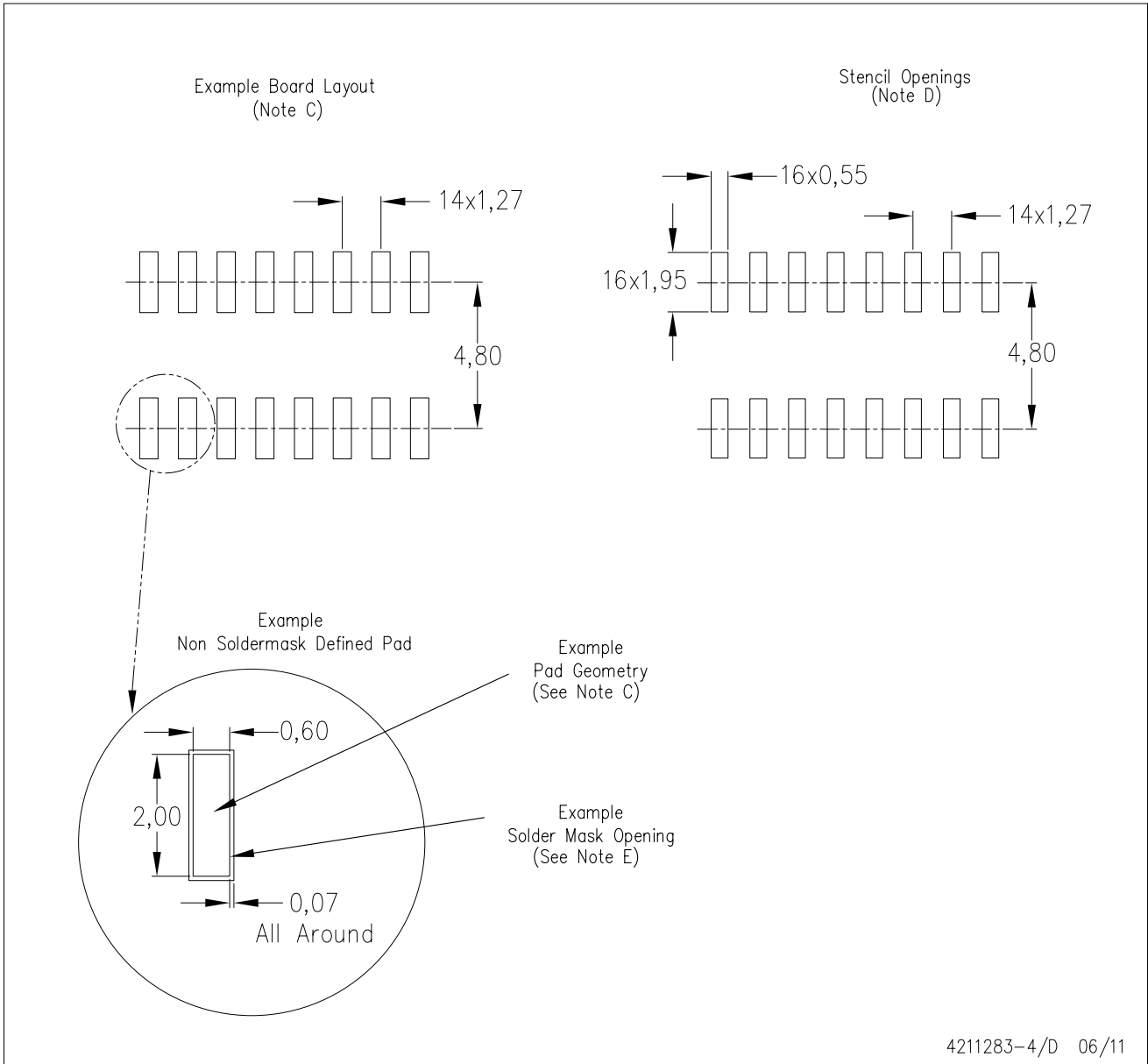
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

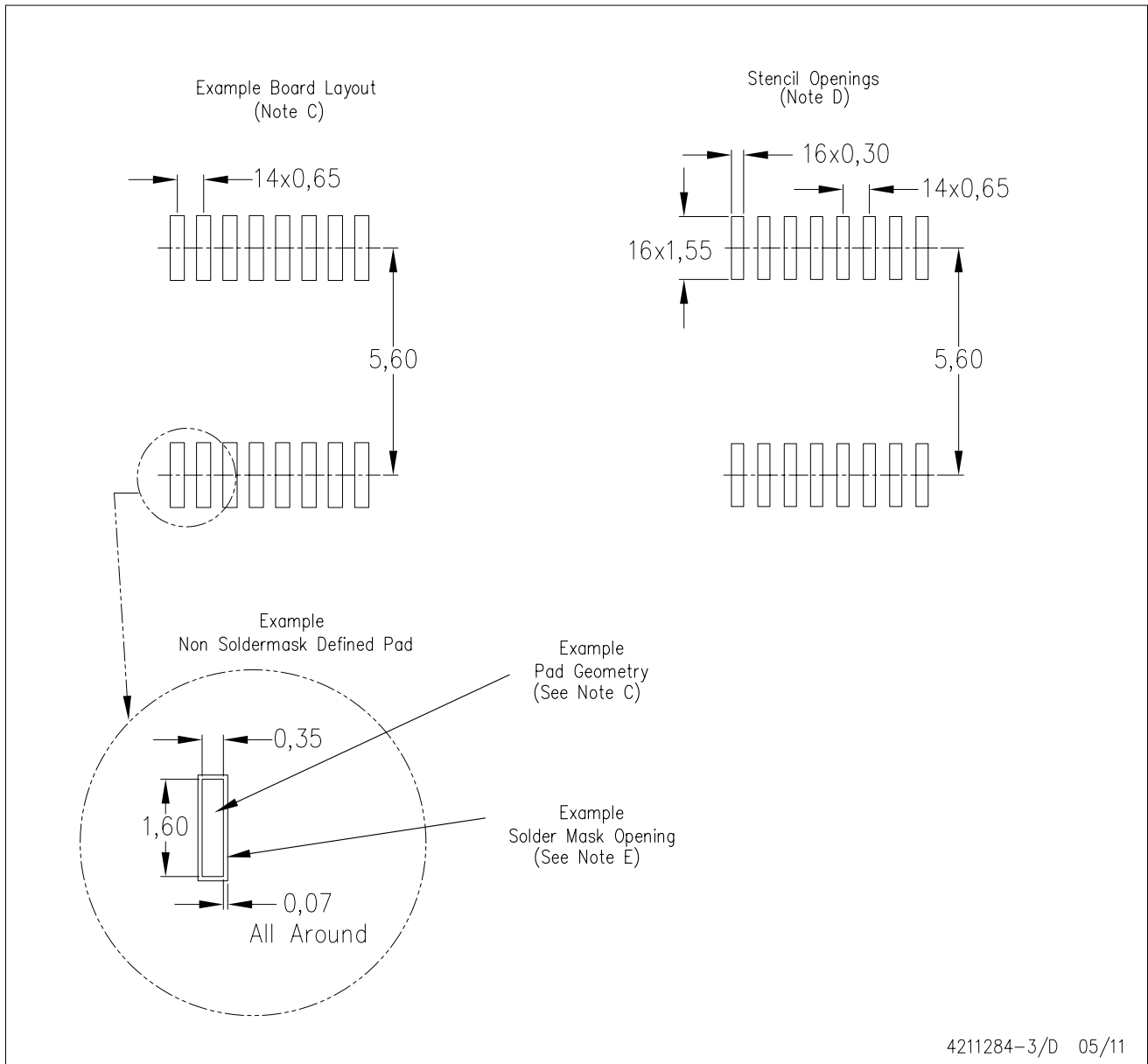


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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