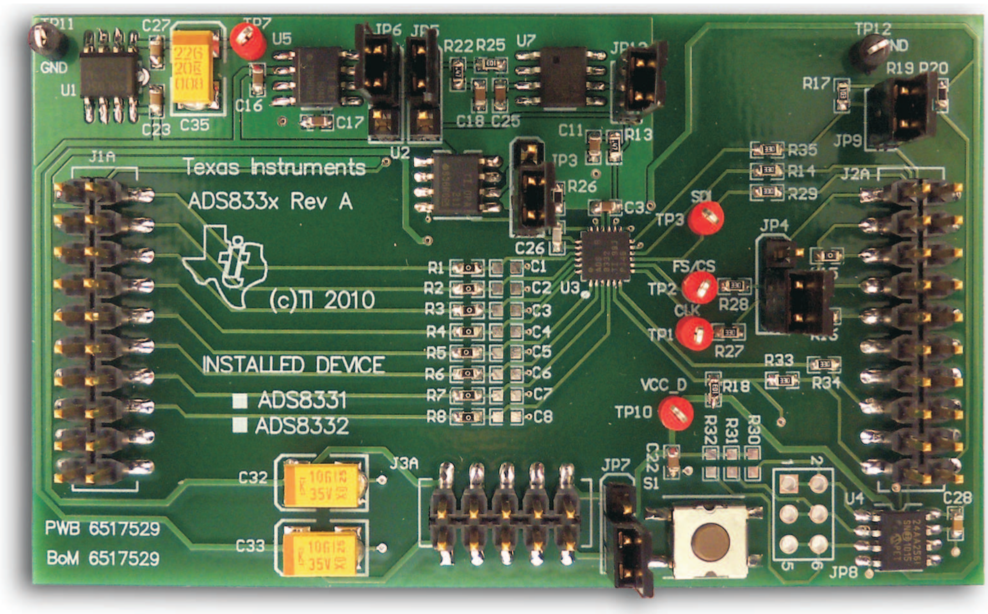
ADS833xEVM User's Guide



ADS833xEVM

This user's guide describes the characteristics, operation, and use of the ADS833xEVM. This evaluation model (EVM) is an evaluation board for the ADS8331 and the ADS8332, a high-performance, 16-bit, four- or eight-channel, successive approximation register (SAR) analog-to-digital converter (ADC). The EVM allows evaluation of all aspects of the ADS8331 and ADS8332. Complete circuit descriptions, schematic diagrams, and bills of material are included in this document.

The following related documents are available for download through the Texas Instruments web site at http://www.ti.com.

Related Documentation

Device	Literature Number
ADS8331	SBAS363
ADS8332	SBAS363
REF5040	SBOS410
OPA350	SBOS099
TL750L05	SLVS017

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Contents

List of Figures

List of Tables

1 EVM Overview

1.1 Features

ADS833xEVM:

- Contains all support circuitry needed for the ADS8331 or ADS8332
- Voltage reference options: external or onboard
- Master clock options: Internal oscillator or external clock source
- Onboard buffer circuit to drive ADC inputs
- Compatible with the TI Modular EVM System

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS833xEVM. The abbreviations *ADS833x* or *ADS8331/2* refer to the ADS8331 and ADS8332, unless otherwise indicated.

1.2 Introduction

The ADS833xEVM, shown in Figure 1, is an evaluation module built to the TI Modular EVM System specification. It can be connected to any modular EVM system interface card.

Note that the ADS833xEVM has no microprocessor and cannot run software. To connect it to a computer, some type of interface is required.

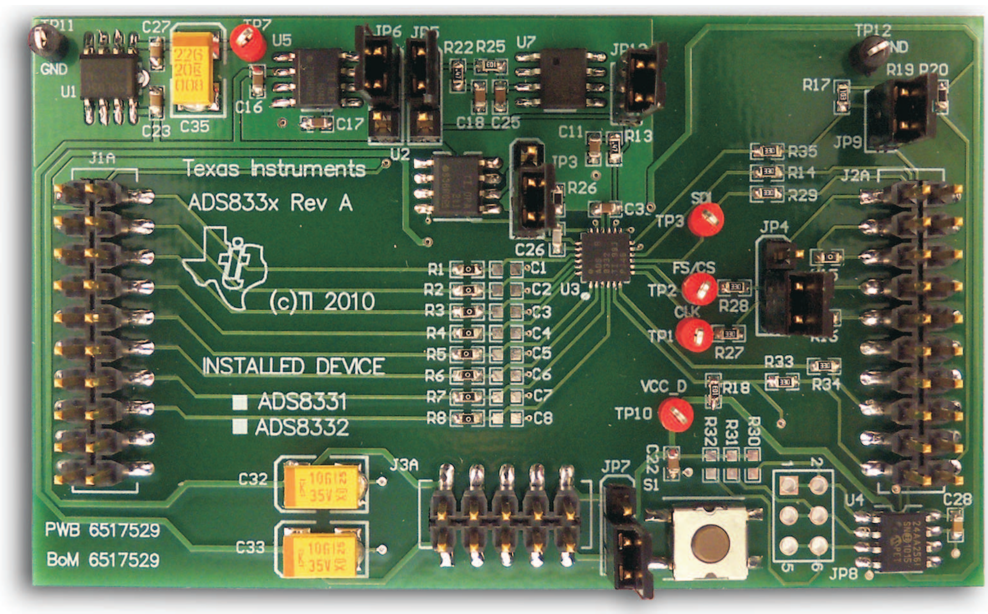


Figure 1. ADS833xEVM

2 Analog Interface

For maximum flexibility, the ADS833xEVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J1. This header/socket provides access to the analog input pins of the ADS8331/32. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

The input pins on the ADS833xEVM are directly connected to the part, with no filtering or protection. It is important that appropriate caution is taken when handling the pins. Table 1 summarizes the pinouts for analog interface J1.

Table 1. J1: Analog Interface Pinout

Pin Number	Signal	Description
J1.1 - J1.19 (odd) GND	Analog ground connections	
J1.2	IN0	IN0 analog input
J1.4	IN1	IN1 analog input
J1.6	IN2	IN2 analog input
J1.8	IN3	IN3 analog input
J1.10	NC/IN4	IN4 analog input (ADS8332 only)
J1.12	NC/IN5	IN5 analog input (ADS8332 only)
J1.14	NC/IN6	IN6 analog input (ADS8332 only)
J1.16	NC/IN7	IN7 analog input (ADS8332 only)
J1.18	GND	Analog ground connection
J1.20	REF+	External reference source input (positive)

3 Digital Interface

3.1 Serial Data Interface

The ADS833xEVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J5. This header/socket provides access to the digital control and serial data pins of the ADC. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 2 describes the J2 serial interface pins.

Table 2. J2: Serial Interface Pins

Pin No.	Pin Name	Signal Name	I/O Type	Pull-Up	Function
J2.1	CNTL	$\overline{\text{CS}}$/FS	In	None	$\overline{\text{CS}}$/FS signal (see jumper JP4)
J2.2	GPIO0	Unused	—	—	
J2.3	CLKX	SCLK	In	None	ADS833x SPI clock
J2.4	DGND	DGND	In/Out	None	Digital ground
J2.5	CLKR	SCLK	In	None	ADS833x SPI clock
J2.6	GPIO1	Unused	—	—	
J2.7	FSX	$\overline{\text{CS}}$/FS	In	None	$\overline{\text{CS}}$/FS signal (see jumper JP4)
J2.8	GPIO2	Unused	—	—	
J2.9	FSR	$\overline{\text{CS}}$/FS	In	None	$\overline{\text{CS}}$/FS signal (see jumper JP4)
J2.10	DGND	DGND	In/Out	None	Digital ground
J2.11	DX	DIN	In	None	ADS833x SPI data in
J2.12	GPIO3	Unused	—	—	
J2.13	DR	DOUT	Out	None	ADS833x SPI data out
J2.14	GPIO4	Unused	—	—	
J2.15	$\overline{\text{INT}}$	EOC/INT/CDI	In/Out	None	Status output/ Daisy-chain input
J2.16	SCL	SCL	In/Out	High	I^{2}C™ clock for EEPROM
J2.17	TOUT	$\overline{\text{CONVST}}$	In	High	Convert start signal
J2.18	DGND	DGND	In/Out	None	Digital ground
J2.19	GPIO5	$\overline{\text{RESET}}$	In	High	Reset signal, active low
J2.20	SDA	SDA	In/Out	High	I^{2}C data for EEPROM

Note that many of the pins on J2 are connected directly to the ADS8331/32. Some of the control signals on the EVM may have weak pull-up resistors to provide default settings for the pins. See the ADS8331 and ADS8332 product data sheet for complete details on these pins.

4 Power Supplies

J3 is the power-supply input connector. Table 3 lists the configuration details for J3. Analog inputs to the ADC can be applied directly to the device (see *Analog Input*). An additional bipolar supply is needed to power the bipolar amplifiers. For optimum noise performance, the external supplies (+VA and –VA) should be used.

Table 3. J3 Configuration: Power-Supply Input

Pin No.	Pin Name	Function	Required
J3.1	+VA	+10V to +15V	Yes
J3.2	–VA	–10V to –15V	Yes
J3.3	+5VA	+5V analog supply	No
J3.4	–5VA	–5V analog supply	No
J3.5	DGND	Digital ground input	Yes
J3.6	AGND	Analog ground input	Yes
J3.7	+1.8VD	1.8V digital supply	No
J3.8	VD1	Unused	No
J3.9	+3.3VD	3.3V digital supply	Yes/Optional
J3.10	+5VD	+5V	Yes/Optional

The ADS833xEVM board requires several power supplies in order to power all of the installed components. The onboard OPA211 drives the ADC input. In order to have the full common-mode input range of 0V to 4.096V, the OPA211 requires ±10V power supplies. The +10V power supply is also used to power the REF5040 and TL750L05 +5V regulator. The +5V derived from the low-dropout regulator (LDO) powers the +VA analog voltage source for the ADS833x and the OPA350, which drives the reference input.

The benefit of using a regulator to create +5V ensures that the ADC and OPA350 are powered at the same time as the input drive circuitry. Otherwise, applying power to the OPA211 and attempting to drive the ADC inputs before powering on the ADS833x could cause potential damage or cause the ADC to power up in an unknown state.

The digital voltage supply for the ADS833x is controlled by jumper JP7. By default, the jumper is in the 1-2 position, set to use the +5VD to power the ADC VBD supply. The +3.3VD supply is also an option.

5 Voltage Reference

The ADS833xEVM comes with an onboard Texas Instruments' REF5040. The reference voltage signal can either be connected directly to the ADS8331/32 or filtered through a OPA350 unity gain buffer before connection to the ADC. Jumpers JP5 and JP12 control whether the reference voltage signal is routed through the OPA350 buffer or connected directly to the ADC.

It is recommended that the power supply be turned off while setting the jumper settings to control whether or not the reference buffer is enabled. Doing so will verify that the EVM is not damaged as the OPA350 is switched in or out. If you are unable to turn off the power, care ***must*** be taken with regard to the order that JP5 and JP12 are changed when changing from the OPA350 buffer. When bypassing the OPA350, make sure that the JP12 jumper is removed first, before the JP5 jumper is moved to the 2-3 position. This procedure ensures that the reference signal is not driven from two different places.

The ADS833xEVM board is designed to either use the onboard 4.096V reference from the REF5040 or an external source that can be connected to header J1. Jumper J6 is used to select the ADC reference source.

6 Clock Source

The clock for the ADS8331/32 can come from one of two sources: the ADC internal oscillator or externally using the SCLK (SCLK/2). Pin J2.3 is used for the SCLK input.

7 EVM Operation

This section provides information on the analog input, digital control, and general operating conditions of the ADS833xEVM.

7.1 Analog Input

The four inputs from the ADS8331 (or eight inputs from the ADS8332) are routed directly from the ADC to header J1 on the EVM board. On the printed circuit board (PCB), there is the option to install a first-order RC filter on any of the channels. Each channel currently has installed 0Ω resistors in series and pads to install a capacitor (left open by default). Simply replacing the 0Ω resistor and installing a capacitor creates a low-pass filter. Note that each of these analog inputs are referenced to the analog ground of the EVM board.

The ADS833xEVM also has the option to use an onboard signal conditioning filter between the mux and ADC input. Using signal conditioning here helps to minimize the cost of a design by allowing the user to drive all eight of the analog input channels using a single op amp. In the EVM design, the OPA211 is used in a unity-gain configuration in combination with a 34.8Ω and 750pf first-order RC filter. This configuration has been tested to meet the ac specifications in the ADS8331 and ADS8332 product data sheet. See the appendix for a complete schematic of the EVM board.

7.2 Digital Control

The digital control signals can be applied directly to J6 (top or bottom side). The modular ADS833xEVM can also be connected directly to a DSP or microcontroller interface board, such as the 5-6K Interface EVM or HPA-MCU Interface boards available from Texas Instruments. For a list of compatible interface and/or accessory boards for the EVM or the ADS8331/32, see the relevant product folder on the TI web site.

7.3 Default Jumper Settings and Switch Positions

Figure 2 shows the jumpers found on the EVM and the respective factory default conditions for each.

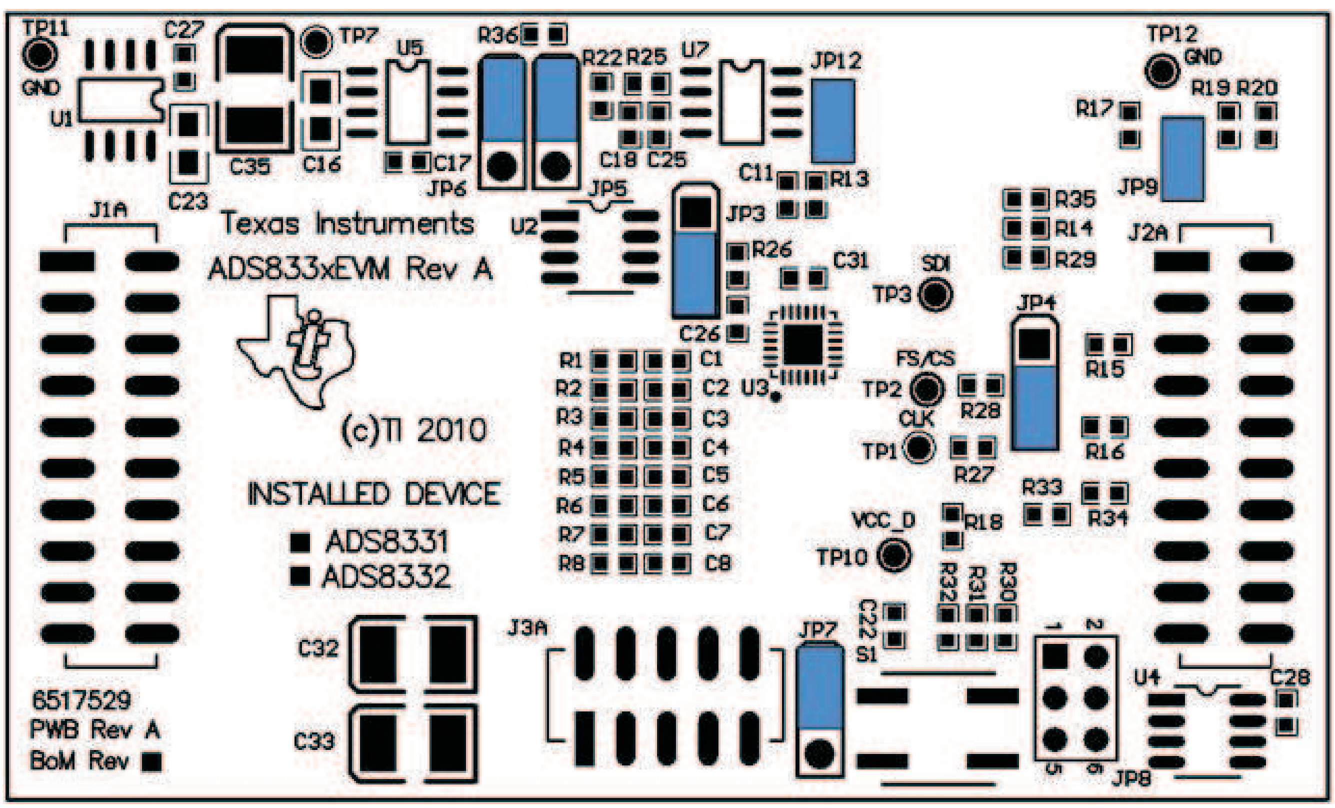


Figure 2. ADS833xEVM Default Jumper Locations

The ADS833xEVM has several hardware options to allow users to test the ADC under certain conditions. On the PCB, jumpers are used to add or remove op amps to drive the reference line and the ADC input. By default, the EVM is configured to use the REF5040 to create a 4.096V signal for the reference voltage; it is buffered through an OPA350. The analog inputs also have the option to use an onboard op amp to properly drive the ADC input. The OPA211 in a unity-gain configuration is placed between the MUX_{OUT} and ADC_{IN} pins to give an example of how to drive any of the input channels using a single op amp. All of the hardware options found on the ADS833xEVM are controlled through jumpers and switches.

Jumper JP3 controls whether the OPA211 unity-gain buffer, used to drive the analog input signals, is enabled or bypassed. By default, JP3 is in the 1-2 position to route the signal through the op amp buffer and RC filter before reaching the converter input. Moving the jumper to the 2-3 position bypasses the OPA211 and routes the input signal only through a first-order, low-pass filter.

Jumper JP4 is used to route the FS/$\overline{CS}$ signal from the ADS8331/32 to either pin J2.1 or J2.7 and J2.9. By default, the jumper is in the 2-3 position, routing the signal to J2.7 and J2.9.

As mentioned previously, the ADS833xEVM has the option to use an onboard OPA350 to drive the reference voltage. Two jumpers are used to route the reference voltage through the op amp. JP5 routes the signal through the OPA350 and JP12 connects the op amp output to the ADC reference voltage. Both jumpers must be properly placed in order to use or bypass the reference buffer. By default, JP5 is in the 1-2 position and JP12 is installed, routing the reference voltage through the OPA350 and connecting it to the ADC reference. If JP12 is removed and JP5 is in the 2-3 position, the OPA350 can be bypassed. See the *Reference Voltage* section for more information on bypassing the op amp.

JP6 selects the reference source. By default, JP6 is in the 1-2 using the REF5040 installed on the EVM. If an external reference voltage is needed, simply set JP6 to the 2-3 position. An external reference signal can then be applied to pin 20 on the J1 header.

Jumper JP7 selects between using a +3.3VD or +5VD voltage to power the +VBD signal of the ADC. By default, the jumper is in the 1-2 position to use +5VD.

JP9 allows you to use an external source to trigger the $\overline{CONVST}$. By default, the jumper is installed routing the $\overline{CONVST}$ signal to the J2 header. If the jumper is removed, the $\overline{CONVST}$ signal can be controlled via an external source to the jumper pin.

Additionally, there is one switch used to control the $\overline{RESET}$ signal of the ADC. S1 is a pushbutton switch used to perform a hardware reset of the ADC.

Table 4 lists the jumpers found on the EVM and the factory default conditions for each of the configurable jumpers.

Table 4. List of Configured Jumpers

Jumper	Default Position	Switch Description
JP3	1-2	Enable the OPA211 buffer amplifier to drive ADC inputs
JP4	2-3	Route $\overline{CS}$ signal to J2.7 and J2.9
JP5	1-2	Enable the OPA350 buffer amplifier to drive reference voltage
JP6	1-2	Use onboard REF5040 for ADC reference
JP7	1-2	+VBD to +5V
JP9	Installed	Connect $\overline{CONVST}$ signal to J2 header
JP12	Installed	Route reference signal from OPA350 to ADC
SW1	N/A	Pushbutton switch to control Reset signal

8 Schematics and Layout

The schematic for the ADS833xEVM is appended to this user's guide. The bill of materials is provided in Table 5. Figure 3 and Figure 4 illustrate the PCB layout.

8.1 Bill of Materials

Table 5. Bill of Materials

Item No.	ADS8331 Qty	ADS8332 Qty	Ref Des [(1)]	Description	Manufacturer	Part Number
1	0	0	C1, C2, C3, C4, C5, C6, C7, C8	Not installed		
2	5	5	C11, C18, C22, C25, C27	Capacitor, ceramic 10UF 6.3V X5R 20% 0603	TDK	C1608X5R0J106M
3	3	3	C16, C23, C34	Capacitor, ceramic 10UF 10V X5R 10% 0805	Murata	GRM219R61A106KE44D
4	6	6	C12, C13, C15, C24, C28, C30	Capacitor, ceramic 0.1UF 16V 10% X7R 0603	Murata	GRM188R71C104KA01D
5	2	2	C17, C31	Capacitor, ceramic 1.0UF 16V X5R 10% 0603	TDK	C1608X5R1C105K
6	1	1	C26	Capacitor, ceramic 1000PF 50V 5% C0G 0603	Murata	GRM1885C1H102JA01D
7	2	2	C32, C33	Capacitor, tantalum 10UF 35V 20% SMD	Kemet	B45196H6106M309
8	1	1	C35	Capacitor, tantalum 22UF 20V 10% SMD	Kemet	T491C226K020AT
9	2	2	J1A, J2A (Top Side)	10-pin, Dual row, SM header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
10	2	2	J1B, J2B (Bottom Side)	10-pin, Dual row, SM header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
11	1	1	J3A (Top Side)	5-pin, Dual low, SM header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
12	1	1	J3B (Bottom Side)	5-pin, Dual row, SM header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
13	5	5	JP3, JP4, JP5, JP6, JP7	Header strip, 3 pin (1x3)	Samtec	TSW-103-07-L-S
14	0	0	JP8	Not installed		
15	2	2	JP9, JP12	Header strip, 2 pin (1x2)	Samtec	TSW-102-07-L-S
16	6	6	R1, R2, R3, R4, R15, R16	Resistor, 0Ω 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEY0R00V
	0	0	R5, R6, R7, R8	Not installed		
	0	4		Resistor, 0Ω 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEY0R00V
17	2	2	R13, R22	Resistor, .47Ω 1/10W 5% 0603	Panasonic	ERJ-3RQJR47V
18	7	7	R14, R27, R28, R29, R33, R34, R35	Resistor, 33Ω 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ330V
19	4	4	R17, R18, R25, R36	Resistor, 10kΩ 1/10W 5% 0603 SMD	Yageo	RC0603JR-0710KL
20	2	2	R19, R20	Resistor, 4.99kΩ 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF4991V
21	1	1	R26	Resistor, 34.8Ω 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF34R8V
22	0	0	R30, R31, R32	Not installed		
23	1	1	S1	Switch, LT 6MM	Panasonic	EVQ-PHK03T
24	5	5	TP1, TP2, TP3, TP7, TP10	Test point - Single .025 pin, red	Keystone	5000
25	2	2	TP11, TP12	Test point - Single .025 pin, black	Keystone	5001
26	1	1	U1	IC LDO pos-volt reg 5V 8-SOIC	Texas Instruments	TL750L05CDR
27	3	3	U2	IC Op Amp GP R-R 80MHZ SGL 8SOIC	Texas Instruments	OPA211ID

(1) The following reference designators are not used:
- C9, C10, C14, C19, C20, C21, C29, R9, R10, R11, R12, R21, R23, R24, TP4, TP5, TP6, TP8, TP9, JP1, JP2, JP10, JP11, U6

Table 5. Bill of Materials (continued)

Item No.	ADS8331 Qty	ADS8332 Qty	Ref Des [(1)]	Description	Manufacturer	Part Number
28	1	0	U3	IC ADC 16-bit 500kSPS 4-Ch 24VQFN	Texas Instruments	ADS8331IBRGET
	0	1	U3	IC ADC 16-bit 500kSPS 8-Ch 24VQFN	Texas Instruments	ADS8332IBRGET
29	1	1	U4	IC EEPROM 256Kbit 400kHz 8SOIC	Microchip	24AA256-I/SN
30	1	1	U5	IC Precision V-ref 4.096V LN 8-SOIC	Texas Instruments	REF5040AID
31	1	1	U7	IC Op Amp GP R-R 38MHZ SGL 8SOIC	Texas Instruments	OPA350UA
32	7	7	N/A	0.100 Shunt - black	Samtec	SNT-100-BK-T

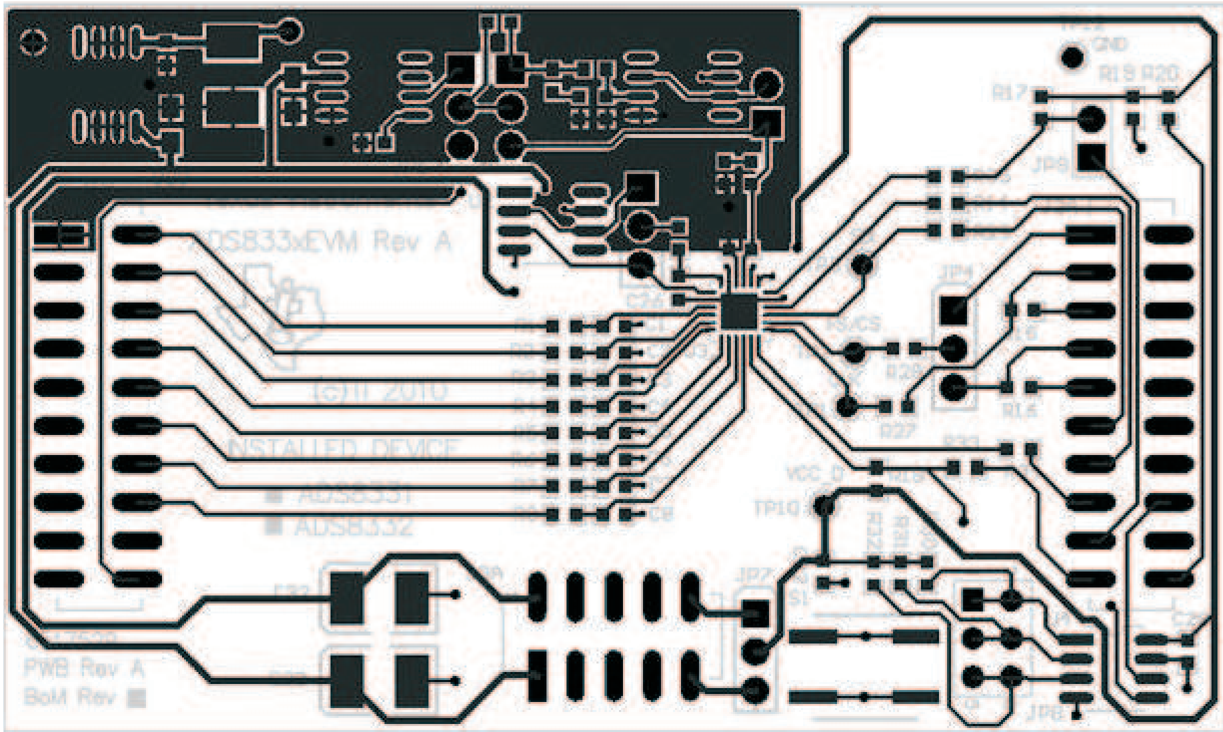


Figure 3. ADS833xEVM: Top Layer

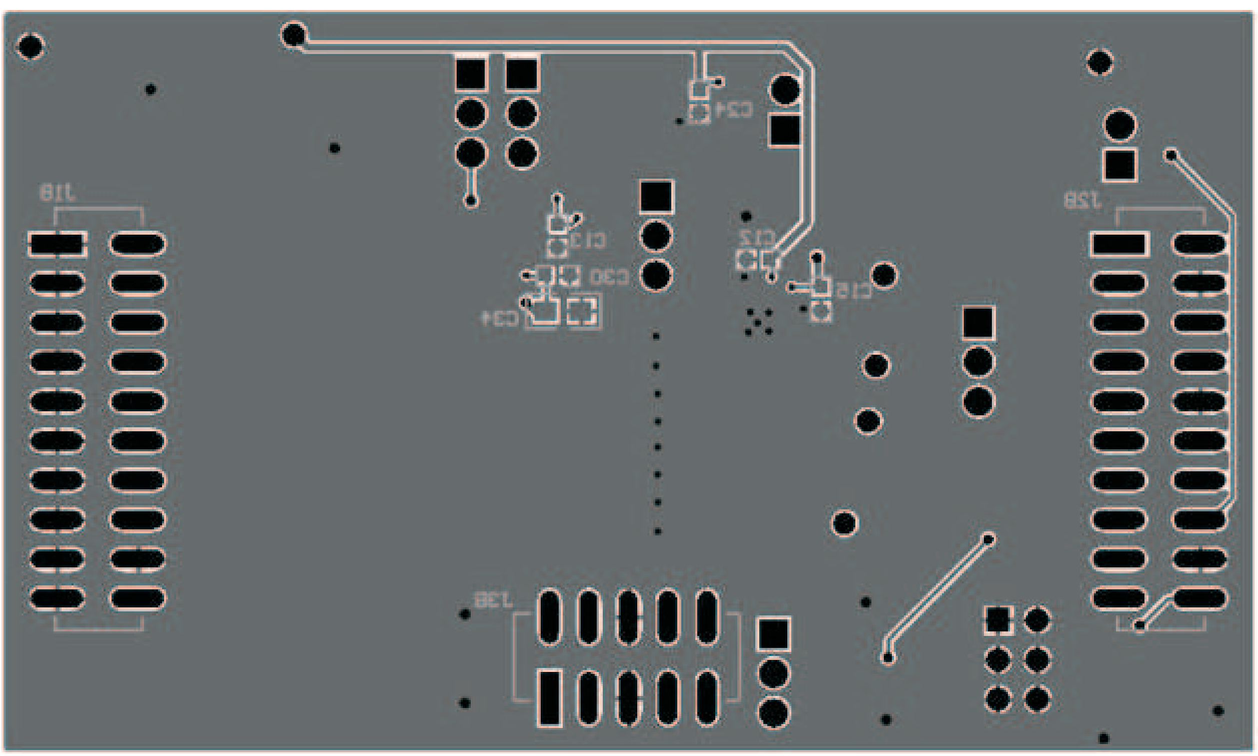
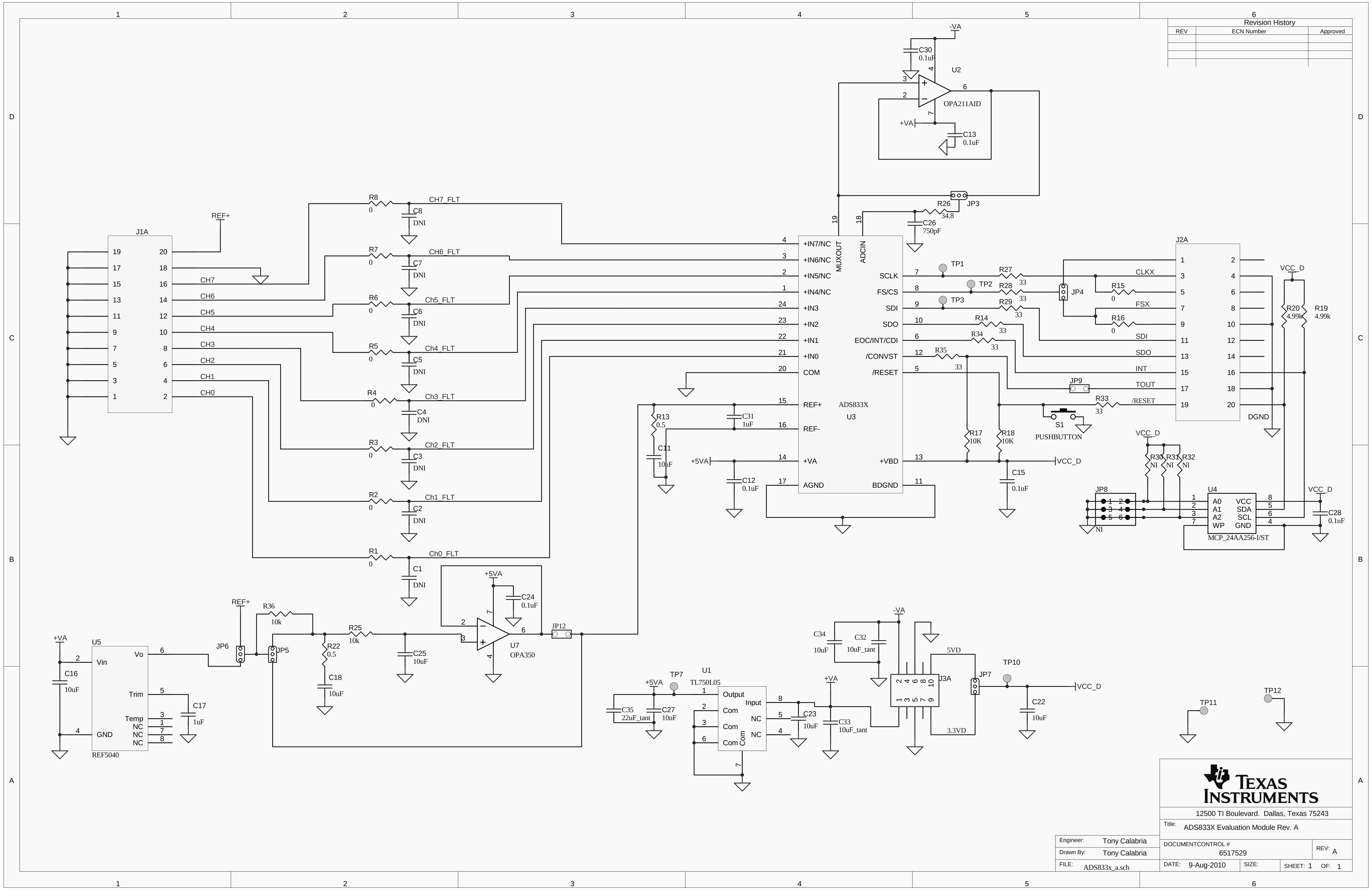


Figure 4. ADS833xEVM: Bottom Layer

Revision History

Changes from Original (August, 2010) to A Revision	Page
• Updated Table 3	5

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.


Revision History
REV
ECN Number
Approved
J1A
REF+
CH7
CH6
CH5
CH4
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CH2
CH1
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CH7_FLT
C8
DNI
R7
CH6_FLT
C7
R6
Ch5_FLT
C6
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Ch4_FLT
C5
R4
Ch3_FLT
C4
R3
Ch2_FLT
C3
R2
Ch1_FLT
C2
R1
Ch0_FLT
C1
-VA
C30
0.1uF
U2
OPA211AID
+VA
C13
0.1uF
R26
34.8
JP3
C26
750pF
MUXOUT
ADCIN
+IN7/NC
+IN6/NC
+IN5/NC
+IN4/NC
+IN3
+IN2
+IN1
+IN0
COM
REF+
REF-
+VA
AGND
SCLK
FS/CS
SDI
SDO
EOC/INT/CDI
/CONVST
/RESET
+VBD
BDGND
ADS833X
U3
TP1
TP2
TP3
R27
R28
R29
R14
R34
R35
33
JP4
R15
R16
CLKX
FSX
SDI
SDO
INT
TOUT
/RESET
JP9
R33
S1
PUSHBUTTON
R17
10K
R18
10K
C15
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VCC_D
J2A
DGND
R20
4.99k
R19
4.99k
R30
R31
R32
NI
JP8
U4
A0
A1
A2
WP
VCC
SDA
SCL
GND
MCP_24AA256-I/ST
C28
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R13
0.5
C31
1uF
C11
10uF
+5VA
C12
0.1uF
+VA
U5
Vin
Vo
Trim
Temp
NC
GND
REF5040
C16
10uF
C17
1uF
JP6
JP5
R36
10k
R22
0.5
C18
10uF
R25
10k
C25
10uF
C24
0.1uF
U7
OPA350
JP12
TP7
U1
TL750L05
Output
Input
Com
NC
C35
22uF_tant
C27
10uF
C23
10uF
C33
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TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
Title: ADS833X Evaluation Module Rev. A
Engineer: Tony Calabria
Drawn By: Tony Calabria
FILE: ADS833x_a.sch
DOCUMENTCONTROL # 6517529
REV: A
DATE: 9-Aug-2010
SIZE:
SHEET: 1 OF: 1

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0V to +4.096V and the output voltage range of 0V to 5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +35°C. The EVM is designed to operate properly with certain components above +35°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.